Application Note AN 63: Magic Eyes MP2520F to NetChip NET2272 Interface

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1 Applicability

Magic Eyes MP2520F – a super-integrated SoC (system on a chip) aimed at providing high performance multimedia functionality and low power consumption for Personal Multimedia Digital Assistants
NetChip NET2272 – USB 2.0 High-speed Programmable Peripheral Controller

2 General Description

This document assumes that the HCLK bus frequency of the MP2520F is 66 MHz. Following is a table showing the connections between the MP2520F and NET2272 (See Figure 1 for the schematic):

Signal	MP2520F	NET2272
Address	ZA[5:1]	LA[4:0]
Data	ZD[15:0]	LD[15:0]
Chip Select	nSCS2#	CS#
Read Strobe	nPOE#	IOR#
Write Strobe	nPWE#	IOW#
DMA Request	DREQ2	DREQ
DMA Acknowledge	DVAL2#	DACK
Interrupt	GPIOJ[14]	IRQ#

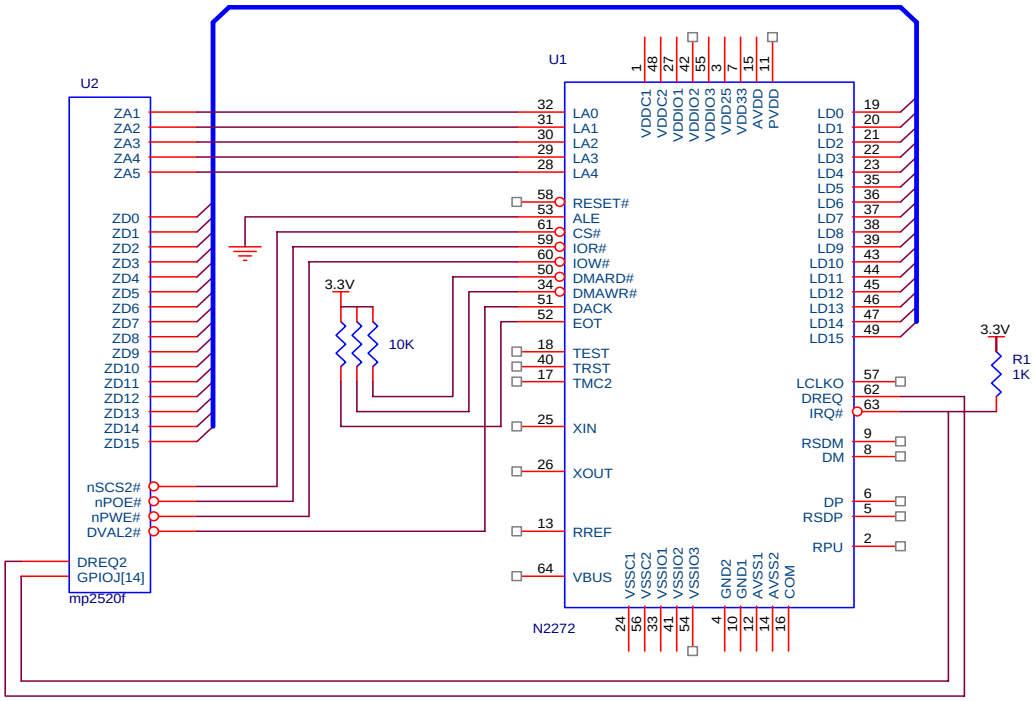

Figure 1: Magic Eyes MP2520F to NetChip NET2272 Interface

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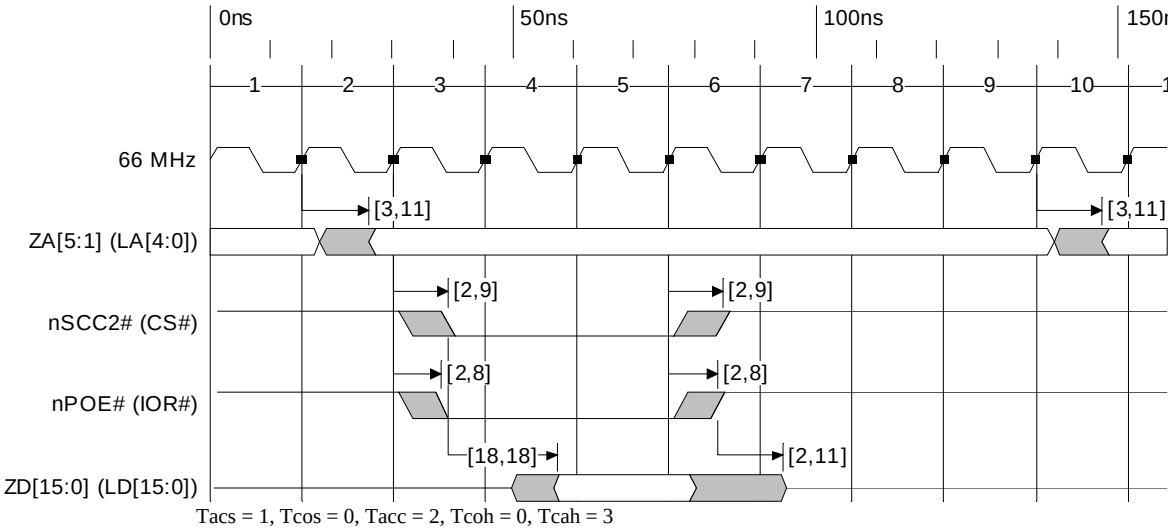
3 MP2520F Read Transaction from NET2272

The read transaction can be performed in 8 clock cycles at 66 MHz. The address setup time of -1 nsec is provided by the MP2520F, because the nPOE# signal is delayed one clock cycle from the assertion of the address. The 18 nsec data access time of the NET2272 meets the 4 nsec data setup time of the MP2520F, assuming that Tacc = 2 (Access time = 3 clocks).

When nPOE# is negated at the end of the transaction, the data is sampled by the MP2520F and the NET2272 stops driving the data bus. The -2 nsec address hold time of the NET2272 is provided by the MP2520F. The NET2272 floats its data bus within 11 nsec, which is well before any write data might be driven by the MP2520F.

By setting the Tcah parameter (Address hold time after CS# de-asserted) to 3, the MP2520F provides 5 clock cycles (75 nsec) of recovery time from the de-assertion of nPOE# until it is asserted again. The NET2272 requires 35 nsec of read recovery time, but Tcah is set to a higher value because of the 52 nsec I/O write recovery time required by the NET2272.



Tacs = 1, Tcos = 0, Tacc = 2, Tcoh = 0, Tcah = 3

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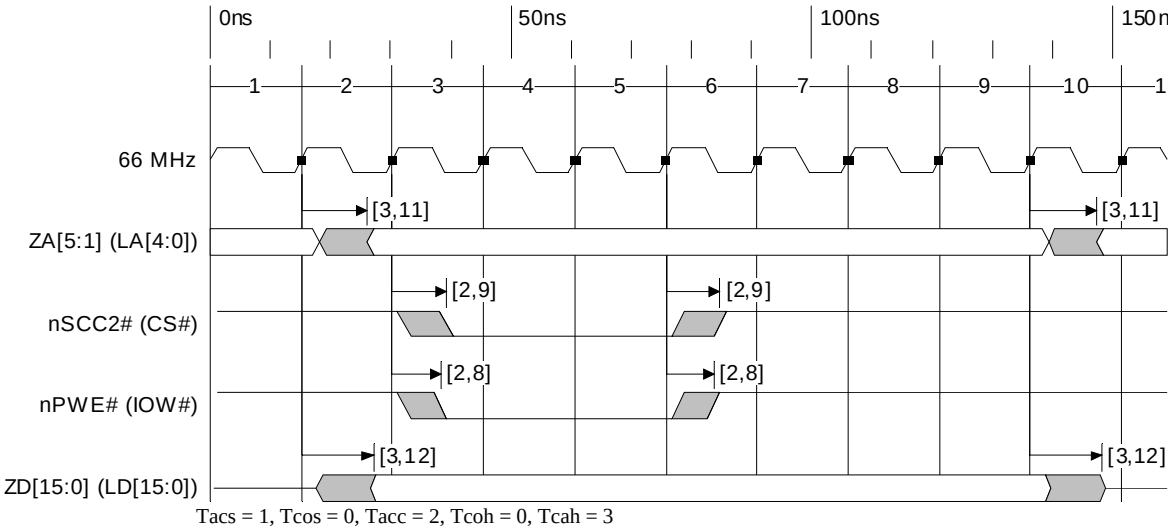
4 MP2520F Write Transaction to NET2272

The write transaction can be performed in 8 clock cycles at 66 MHz. The address/data setup time and hold times are easily met, since the address/data are presented before nPWE#, and are held until after nPWE# is de-asserted. The IOW# pulse wide requirement of 5 nsec is provided by the MP2520F, since it drives it for three full clock cycles. This transaction could be made shorter, but Tacc (access time) must be 2 for the read transactions.

By setting the Tcah parameter (Address hold time after CS# de-asserted) to 3, the MP2520F provides 5 clock cycles (75 nsec) of recovery time from the de-assertion of nPWE# until it is asserted again. The NET2272 requires 52 nsec of write recovery time.



Tacs = 1, Tcos = 0, Tacc = 2, Tcoh = 0, Tcah = 3

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5 Flow-Through Mode DMA Transaction

The MP2520F DMA flow-through mode allows data to be transferred directly between the NET2272 and system memory without CPU intervention. The MP2520F provides DREQ[3:2] for external devices to use flow-through mode, so channel 2 is used for this application note. The NET2272 can be programmed for Slow, Fast, or Burst DMA mode. The NET2272 is programmed for DMA Fast mode in this application note. It is suggested that the MP2520F and NET2272 DMA registers be programmed with the values shown, assuming that the NET2272 is the source device and that 32-bit system memory is the target device:

5.1 MP2520F DMA Command Register 0 (DMACOM0)

Bit	Bit Name	Description	Suggested Value
15:14	BURSTSIZE	Burst Operation Request Size	00 (1 Word, Not burst operation mode)
13	SRCADDRINC	Source Address Increment Setting	0 (disable)
12	FLOWSRC	When to start data transfer	1 (wait for the request signal before initiating the data transfer)
11:10	SRCMEMFMT	Source Memory Data Format	01 (LS Half-word)
9:8	SRCPERIWD	Source IO Device Data Width	01 (half-word)
7:6	RESERVED		
5	TRGADDRINC	Target Address Increment/Decrement	1 (enable)
4	FLOWTRG	When to start data transfer	0 (no wait to start)
3:2	TRGMEMFMT	Target Memory Data Format	00 (word)
1:0	TRGPERIWD	Target IO Device Data Width	00 (not used)

5.2 MP2520F DMA Control/Status Register (DMACONS)

Bit	Bit Name	Description	Suggested Value
15:11	RESERVED		
10	DMARUN	Start/End DMA	
9	ENDIRQEN	End Interrupt Enable	
8	STOPIRQEN	Enable the interrupt if the channel enters stop state	
7:5	RESERVED		
4	FLYBYS	Source Mode	0 (flow-through)
3	FLYBYT	Target Mode	0 (flow-through)
2	REQPEND	Indicates that the DMA channel has a pending request	
1	ENDINTR	Interrupt	
0	STOPINTR	Channel entering stop state due to a write to the RUN bit	

5.3 NET2272 DMA Request Control Register (DMAREQ)

Bit	Bit Name	Description	Suggested Value
7	DMA Buffer Valid	Select whether the buffer is automatically validated or not	0 (not automatically validated)
6	DMA Request	The state of DREQ output pin	
5	DMA Request Enable	Enable the NET2272 to start requesting DMA cycles	
4	DMA Control DACK	Use IOR#, IOW# during DMA?	1 (DACK# and IOR#, IOW# are used during DMA)
3	EOT Polarity	Polarity of EOT input pin	0 (active low)
2	DACK Polarity	Polarity of DACK input pin	0 (active low)
1	DREQ Polarity	Polarity of DREQ output pin	1 (active high)
0	DMA Endpoint Select	Select which endpoint is being accessed	0 (Endpoint A)

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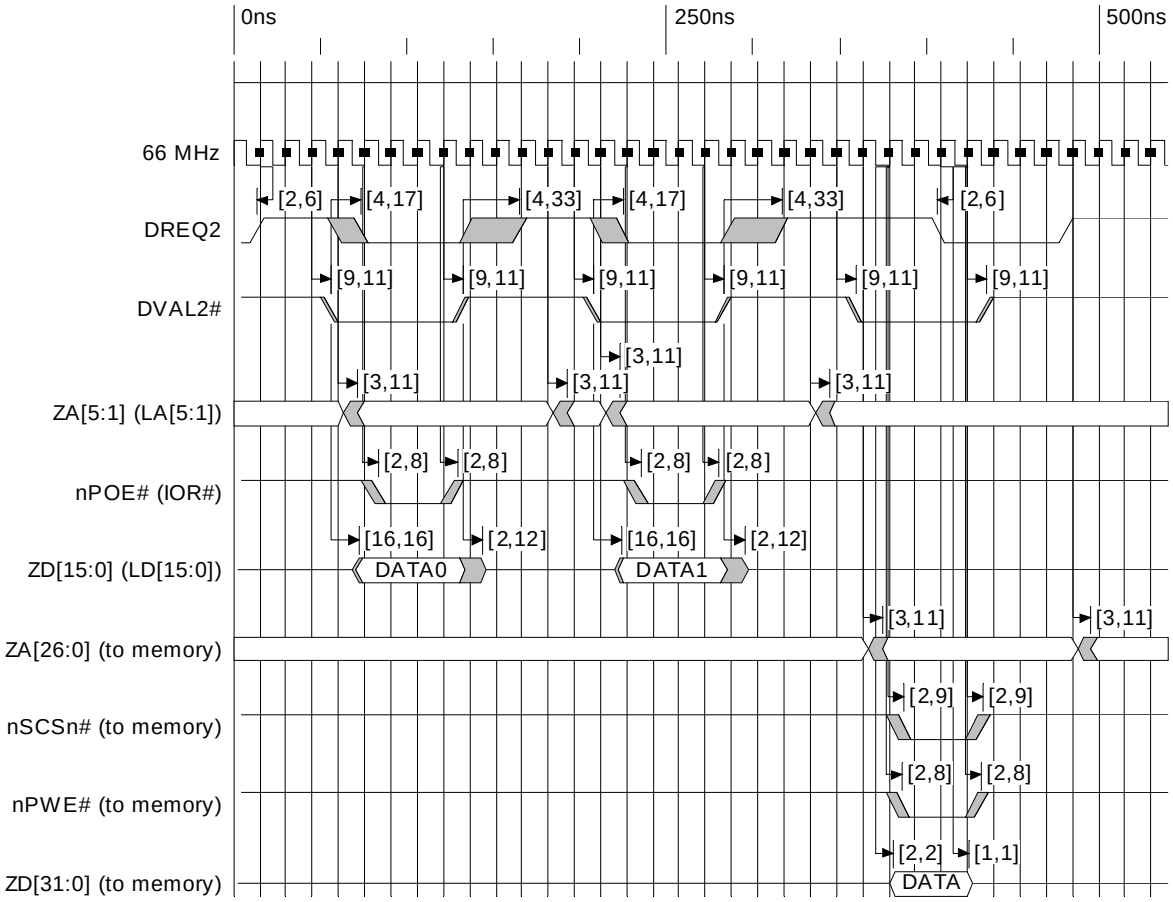
6 DMA Read from NET2272

The NET2272 starts the transaction by asserting DREQ#. The MP2520F recognizes the rising edge of DREQ# and initiates the DMA transaction. Since the NET2272 can only transfer 16-bits at a time, there will be two reads followed by one write to a 32-bit RAM.



Tacs = 1, Tcos = 0, Tacc = 2, Tcoh = 0, Tcah = 3

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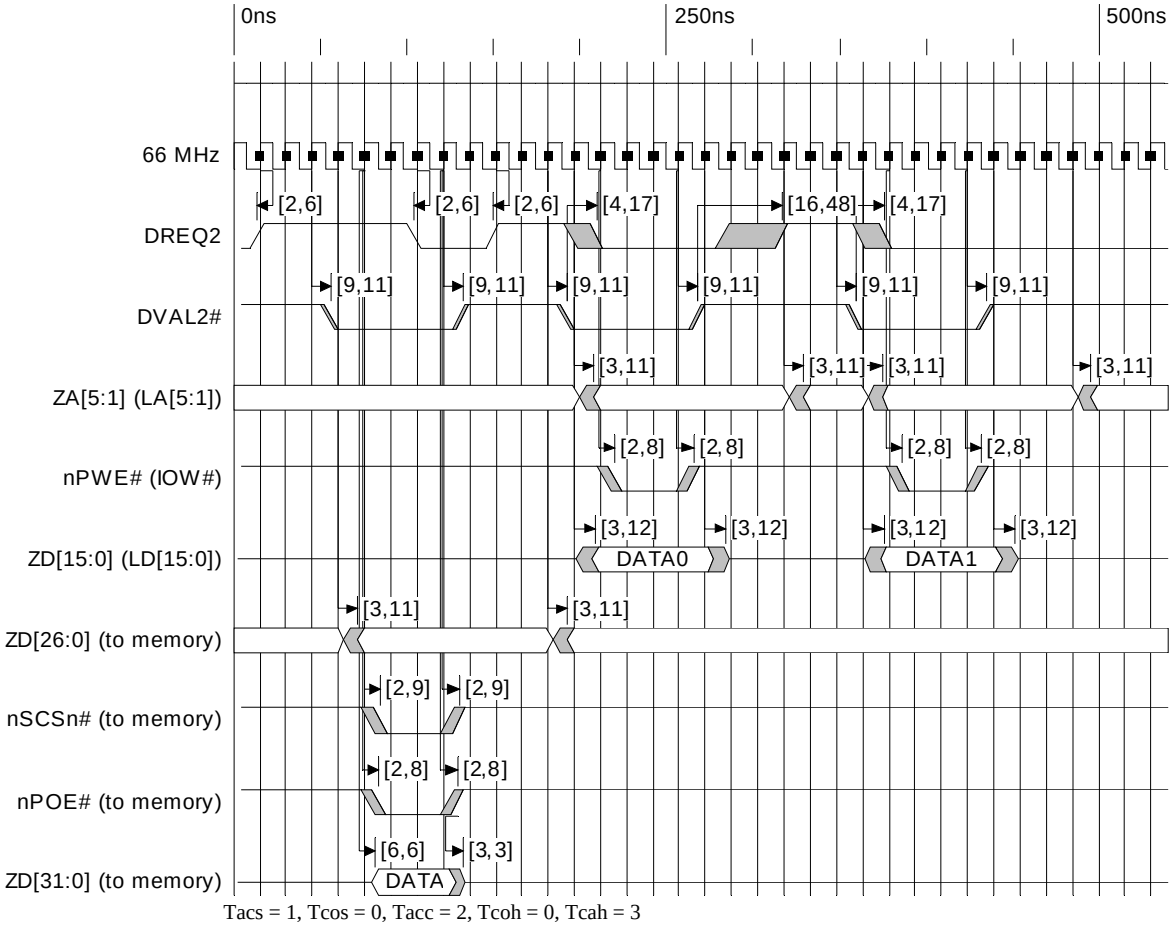
7 DMA Write to NET2272

The NET2272 starts the transaction by asserting DREQ#. The MP2520F recognizes the rising edge of DREQ# and initiates the DMA transaction. Since the NET2272 can only transfer 16-bits at a time, there will be one read to a 32-bit RAM followed by two writes.



Tacs = 1, Tcos = 0, Tacc = 2, Tcoh = 0, Tcah = 3

8 Summary

The MP2520F can be interfaced to the NET2272 with no glue logic. All timing parameters are met at a local bus frequency of 66 MHz. The data throughput between the MP2520F and the NET2272 is 16.4 Mbytes/sec (2/(8*15.2 nsec)).

The MP2520F DMA controller can also be interfaced to the NET2272 with no glue logic. The performance depends on the DMA mode, the speed of the memory that is the target of the DMA transactions, as well as the level of other DMA and CPU activity. To optimize the DMA performance, set Tcah to 0 and use software delays when performing I/O transactions. In fly-by mode, each DMA transaction takes about 32 clock cycles, resulting in a maximum 16-bit data transfer rate of 8 Mbytes/sec.

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