



MMSP™ 2
Data Sheet
MP2520F

Release Version 1.0

Document Release

2005/01/13

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CHAPTER 1

INTRODUCTION

1. INTRODUCTION

1.1 GENERAL DESCRIPTION

MP2520F is the 2nd generation MagicEyes Digital's Multimedia Signal Processor. **MP2520F** is a super-integrated SoC (system on a chip) aimed at providing high performance multimedia functionality and low power consumption for Personal Multimedia Digital Assistants.

MP2520F incorporates a Dual 32bit CPU Processor, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor and a variety of I/O peripheral components. **MP2520F** can significantly reduce system costs by eliminating not only the system control CPU, but also the Graphic IC, MPEG4 Codec IC, Camera Image Processor IC, as well as the USB Host IC. **MP2520F** helps system designers reduce engineering effort and time taken to develop a new system, by adding only memory and I/O devices such as the LCD panel, HDD, Modem module and human I/F devices.

Therefore **MP2520F** is the best solution for high-end Multimedia PDAs, multi-functional Digital Cameras, Portable Multimedia Players, Smart Phones, MoIP (Multimedia over IP) Phones, DVRs, Security Cameras over IP, and Car Infotainment.

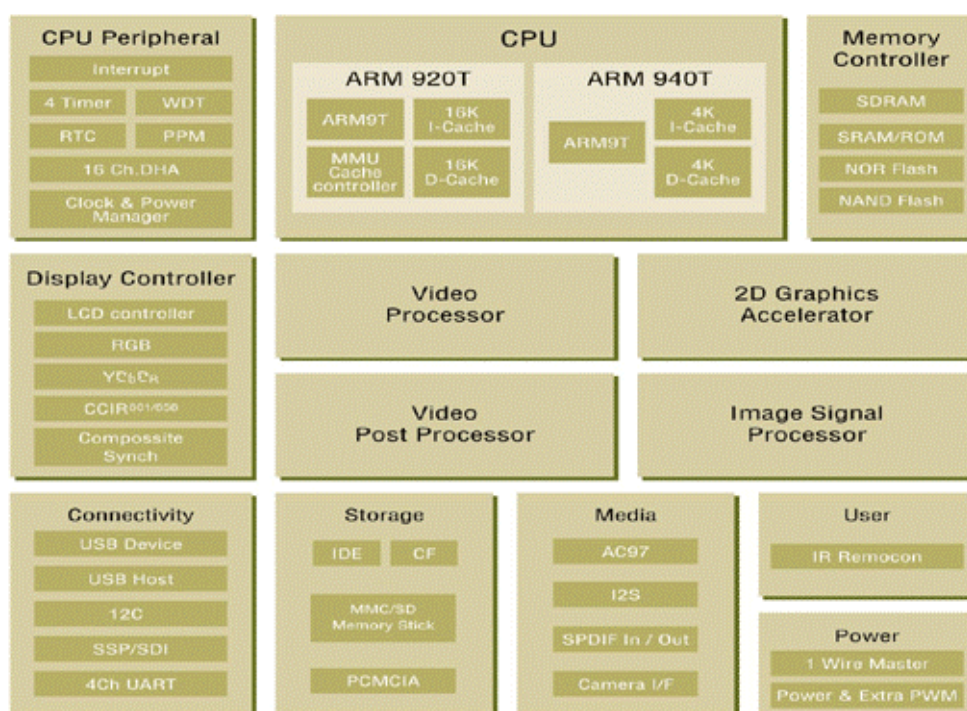


Figure 1-1. Top Level Block Diagram

1.2 KEY FEATURES

- 0.18um, 1.8V CMOS Process Technology.
- 400 pin FBGA (Fine BGA) Package, 18 x 18 mm²
- Dual 32bit CPU (Main Processor, Coprocessor) Embedded Architecture
 - Main Processor used for Operating System & System Control, Audio Processing: ARM 920T CPU (180MHz, >200MIPS), 16KB I-Cache + 16KB D-Cache + MMU
 - Coprocessor used for Video Header Parsing, Video Post Processor Control: ARM 940T CPU (180MHz, >200MIPS), 4KB I-Cache + 4KB D-Cache
- Multi Standard Video Codec including MPEG4, H.263 and JPEG/MJPEG
- Multi Functional Video Post Processor
- Win CE 3.0/4.0 Compatible 2D Graphic Accelerator
- Image Processor with Real Time Digital Zoom & Three (3) Auto Processing
- Pseudo Message Broadcasting with Command Write Buffer Memory Control Bus Architecture for High Performance Pipelined & Burst Data Operation
- USB 1.1 Host Controller, USB 1.1 Slaver, SIR, 4CH UART
- LCD Controller, 16CH.DMA, Timer, Interrupt Controller, RTC
- PCMCIA, Compact Flash, MMC, SD
- AC97 Controller, SPDIF In/Out Controller
- I²C, I²S, SSP, GPIOs, PWM, Power Manager
- Whole Chip Operating Clock 100MHz

1.3 FUNCTIONAL SPECIFICATION

Video (H/W Video Processor):

- MPEG4 ASP Decode @720 x 480, 30fps (DivX 3.11/4.x/5.x Playback)
- MPEG4 SP Encoder / Decode @VGA, 30fps (MPEG4 Camcorder, PVR, MMS)
- MPEG4 SP/H.263 L3 Codec @352 x 288, 30fps (Video Conferencing)
- JPEG Encode or Decode up to 4M pixels (DSC)
- MJPEG Encode or Decode @720 x 480, 30fps (Security Camera)

Speech & Audio (ARM920T CPU S/W):

- Need software development or porting at ARM 920T
- Support from WinCE.NET: WMA
- License from 3rd party: G.723.1
- Support from MagicEyes: PCM, MP3

High Performance 2D Graphics & LCD Controller (H/W)

- Resolution up to 1024 x 768 @ 60Hz
- Two (2) Hardware Video Overlay Surface Support

1.4 INTERNAL BUS ARCHITECTURE

MP2520F has a unique internal bus architecture, which consists of one DRAM memory bus, one Non-DRAM memory & Fast I/O bus, one I/O Peripheral bus and one local data bus. Nine memory bus masters including ARM920T™ CPU, ARM940T™ CPU, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor, LCD Controller, USB Host and DMA can access either internal DRAM memory bus or Non-DRAM memory & Fast I/O bus independently. ARM920T™ CPU, ARM940T™ CPU and DMA are the masters of the I/O Peripheral bus. DMA can read and/or write data from/to the Huffman Controller resident in the Video Post Processor directly through one local data bus.

MP2520F can handle four parallel data access operations through allowing four out of nine bus masters to access one of four internal data buses independently and concurrently. For example, MP2520F allows the ARM920T™ CPU to access I/O components through the I/O Peripheral bus, while one of the 16 DMAs to access the Huffman Controller via the local data bus, another DMA to access external I/O components via the Fast I/O bus, and the Video Processor to access external SDRAM through the DRAM memory concurrently. One local data bus consists of one data read bus and one data write bus. Therefore two out of the sixteen (16) channel DMAs can read and write data from/to the Huffman Controller simultaneously.

There is a pipelined operation between the Video Post Processor and LCD controller, which can display the decoded YUV video signal on the LCD panel directly, through multiple signal processing operations such as de-blocking, de-ring, image scaling down or up, CSC (color space converting) and color dithering. Additionally there is a pipelined operation between the Image Signal Processor and Video Processor, which can support any size of camera input image pixel resolution to be scaled down matching the LCD display pixel resolution size with the CSC operation in real time, without accessing the external video frame buffer. Those pipelined operation structures can significantly reduce external memory bandwidth requirements.

1.5 MEMORY CONTROLLER

The benefits of the super-integration of the ARM920T™ CPU, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor and LCD Controller into one chip are as follows:

- 1) Availability of a simple and unified common system memory usage
- 2) No necessity for data transfer operations between Host CPU and Video Processor, Video Post Processor, 2D Graphic Processor and Image Signal Processor. It can reduce CPU horsepower requirement and external memory bandwidth requirements as well as total power consumption at system level.

The DRAM and Non-DRAM memory bus controllers have a sixteen level individual command & data write buffer in order to enable all nine memory bus masters to access either external DRAM or Non-DRAM memory devices in burst and pipelined operation mode (without having to wait for its and/or the other memory bus masters' data to be completely written to the external memory). The DRAM memory controller can interface with various types of SDRAM memory devices. The Non-DRAM memory controller can interface with various types of Non-DRAM memory device such as SRAM, ROM, NAND/NOR Flash, PCMCIA and Compact Flash.

1.6 2D GRAPHIC PROCESSOR

MP2520F's 2D Graphic Processor accelerates the WinCE™ GDI and Direct2D™ operation without sacrificing CPU horsepower. This feature guarantees the high-resolution (up to 1024x768 pixel) display performance. Additionally it supports two hardware Video Overlay Surface acceleration, which provides two independent YUV video display windows on an RGB graphic window. It allows two different YUV video signals to be scaled down or up, to the size of each video display window, and converted simultaneously into RGB signals in real time.

1.7 IMAGE SIGNAL PROCESSOR

MP2520F's Image Signal Processor supports a CIS/CCD back-end image processing operation, which includes Auto Focus, Auto Exposure and Auto White Balance functionality. It also has Gamma Correction functionality. It can handle CCIR601 and CCIR656 video formats.

1.8 VIDEO PROCESSOR

MP2520F's Video Processor can support multiple standard video codec functionality including MPEG1/2/4, DivX 3.11/4.x/5.x, H.263 and JPEG standard. The Video Processor consists of multiple macro-functional H/W blocks including VLD/VLC, DCT/IDCT, Q/IQ, ME, MP, MC, De-Block, De-Ring and SP(stream packet processor).

1.9 VIDEO POST PROCESSOR

MP2520F's Video Post Processor consists of multiple macro-functional H/W blocks including a video signal scaling block and OSD, sub picture, hardware cursor, hue control, contrast, brightness, dithering, gamma, alpha blending, color key and CSC(color space converting) blocks. Video signal scaling can provide a high precision video signal zoom-in/out functionality to support SD-TV level video quality even during digital zoom-in or zoom-out operations. Also it enables a high resolution CCD/CIS camera image signal to be displayed on the

LCD panel, with scaling down to the LCD display panel resolution size being done in real time. Also either the original camera image or the scaled down image can be recoded selectively.

MP2520F can support up to four (4) screen split functionality with independent scaling, 90/180/270 degree rotation, and a mirror effect. MP2520F can also support a letterbox and Pan/Scan conversion functionality.

MP2520F can support three (3) staged alpha blending operations and six (6) level video mixing operations using two (2) YUV video sources, OSD, Sub Picture, RGB graphics and H/W cursor.

1.10 LCD CONTROLLER

MP2520F's LCD Controller (LCDC) generates the data and timing for active display. It has a variety of user-programmable options including display type and size, output data width, and output data type.

Display sizes up to 1024x768 pixels are supported. However, Bit per pixel (BPP) limits the maximum size screen the LCDC can drive, due to the memory bandwidth. The digital video output supports 12bit/16bit/18bit/24bit RGB, 8bit/12bit Multiplexed RGB (MRGB), and CCIR656, CCIR601, 4:4:4 YCbCr. The MRGB output mode supports the external DVI transmitter.

1.11 USB HOST CONTROLLER

MP2520F has a USB Host Controller 1.1, which makes it possible to enhance or upgrade the system easily by introducing a number of optional modules via the USB connector. Those optional modules can include a camera, portable printer, portable scanner, IC card reader etc.

1.12 NAND FLASH CONTROLLER FOR H/W BOOTLOADER

MP2520F can provide a cost effective solution for program memory, using NAND type FLASH memory instead of the expensive NOR type. It automatically loads the operating system resident in NAND type FLASH memory into the system memory (SDRAM or SRAM), before the CPU accesses the operating system when MP2520F boots up. It also supports a H/W Bootdown function that allows a PC to update the system program memory contents directly via the UART I/F port. This can eliminate the use of any kind of boot program device such as PROM or Mask ROM in the system, thus saving money as well as system board space.

1.13 IDE CONTROLLER

MP2520F has an Ultra DMA 66MHz functional block, which can access external HDD, DVD-ROM and CD-ROM devices directly without using any glue logic.

1.14 USB DEVICE

MP2520F has a USB function controller. The USB function controller is designed to provide a high performance full speed function controller solution with DMA I/F. The USB function controller allows bulk transfer with DMA, interrupt transfer and control transfer.

1.15 UART

MP2520F's UART unit provides four independent asynchronous serial I/O (SIO) ports, each of which can operate in interrupt-based or DMA-based mode. In other words, UART can generate an interrupt or DMA

request to transfer data between CPU and UART. It can support bit rates of up to 115.2K bps. Each UART channel contains two 16-byte FIFOs for receive and transmit. The MP2520F UART includes programmable baud-rates, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking. Each UART contains a baud-rate generator, transmitter, receiver and control unit. The baud-rate generator can be clocked by PCLK. The transmitter and the receiver contain 16-byte FIFOs and data shifters. Data which is to be transmitted, is written to FIFO and then copied to the transmit shifter. It is then shifted out by the transmit data pin (TxDn). The received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

1.16 I²C

MP2520F can support a multi-master I²C-bus serial interface. A dedicated serial data Line (SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices that are connected to the I²C-bus. The SDA and SCL lines are bi-directional.

1.17 AC97 CONTROLLER

The AC97 Controller Unit can support AC97 revision 2.2 features. The AC97 Controller and External codec communicate via an AC-link. AC-link is a serial interface for transferring digital audio, Mic-in, Codec register control, and status information. The AC97 Codec sends the digitized audio samples that the AC97 Controller Unit stores in memory. For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the Codec through the AC-link. The digital-to-analog converter (DAC) in the Codec then converts the audio sample to an analog audio waveform. This chapter describes the programming model for the AC97 Controller Unit. The information in this chapter requires an understanding of the AC97 revision 2.2 specification.

1.18 I²S CONTROLLER

The I²S controller provides a serial link to standard I²S CODECs for digital stereo audio. It supports both the Normal-I²S and MSB-Justified I²S formats, and provides four signals for connection to an I²S CODEC. I²S Controller signals are multiplexed with AC97 Controller pins. The controller includes FIFOs that support DMA access to memory.

1.19 SD/MMC CONTROLLER

The MMC is a universal low cost data storage and communication medium implemented as a hardware card with a simple control unit and a compact, easy-to-use interface that is designed to cover a wide variety of applications such as electronic toys, organizers, PDAs, and smart phones. MMC communication is based on an advanced 6-pin serial bus designed to operate in a low voltage range at medium speed (20 Mbps).

The SD is an evolution of the MMC with an additional 2 pins in a form factor that is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in new audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are compatible with the MMC. The SD is composed of a memory card and an I/O card. The memory card includes a copyright protection mechanism that complies with the security requirements of the Secure Digital Music

Initiative (SDMI) standard, and is faster and has a higher memory capacity. The I/O card combines high-speed data I/O with low-power consumption for mobile electronic devices.

The MMC/SD Host Controller module (MMC/SD module) integrates MMC support with SD memory and I/O functions. The copyright protection mechanism employs mutual authentication and a new cipher algorithm, and is handled in software post-processing.

1.20 DMA CONTROLLER

The DMA Controller transfers data to and from main memory in response to requests generated by internal and external peripherals. The peripherals do not directly supply addresses and commands to the memory system. The DMA Controller has 16DMA channels, 0 through 15, and every DMA request from the peripheral generates at least one memory bus cycle.

1.21 PWM CONTROLLER

MP2520F contains two pulse width modulators: PWM0 and PWM1. Each PWM is controlled by its own set of registers. The PWM unit is clocked off the 7.3728MHz oscillator output and produces a pulse width modulated output signal. Each register contains one or more fields which determine an attribute of the PWMOUTn waveform.

1.22 CLOCK & POWER MANAGER

The Clocks and Power Manager block controls the power mode and the clock frequency of each module. This block has two clock sources. One is EXTCLK and the other is XTI that is a Crystal input. One of these two clock sources is multiplexed according to **MP2520F**'s operation mode and used for the input clock of the PLL. After that, the clock frequency is divided in the CLKGEN block in accordance with the divider register value set. In addition, the divided clock is used for the input clock of the BCLKCTRL, PCLKCTRL and VCLKCTRL blocks, and these blocks divide the clock using the Control Register or cut off. The **MP2520F** power mode consists of Normal, Idle, Sleep and Deep Sleep. The CPU can execute each Power Mode by setting a PWRMODE register.

1.23 TIMER / WATCH DOG TIMER

MP2520F contains a 32-bit timer that is clocked by the 7.3728MHz oscillator. The TCOUNT register is a free running upcounter. The timer also contains four 32-bit match registers (TMATCH0, TMATCH1, TMATCH2, TMATCH3). You can read and write to each register. When the value in the TCOUNT is equal to the value within any of the match registers, and the interrupt enable bit is set, the corresponding bit in the TSTATUS is set. These bits are also routed to the interrupt controller where they can be programmed to cause an interrupt. TMATCH3 also serves as a watchdog timer enable register that resets the **MP2520F** when a match occurs, provided the TCONTROL is set. You must initialize the TCOUNT and TMATCHn registers and clear any set status bits before the FIQ and IRQ interrupts are enabled within the CPU.

1.24 INTERRUPT CONTROLLER

MP2520F has two interrupt controllers. One is the controller for ARM920T and the other is the controller for

ARM940T. Interrupt controllers in **MP2520F** receive requests from 28 interrupt sources. These interrupt sources are provided by internal peripherals such as the DMA controller, UART, IIC etc.

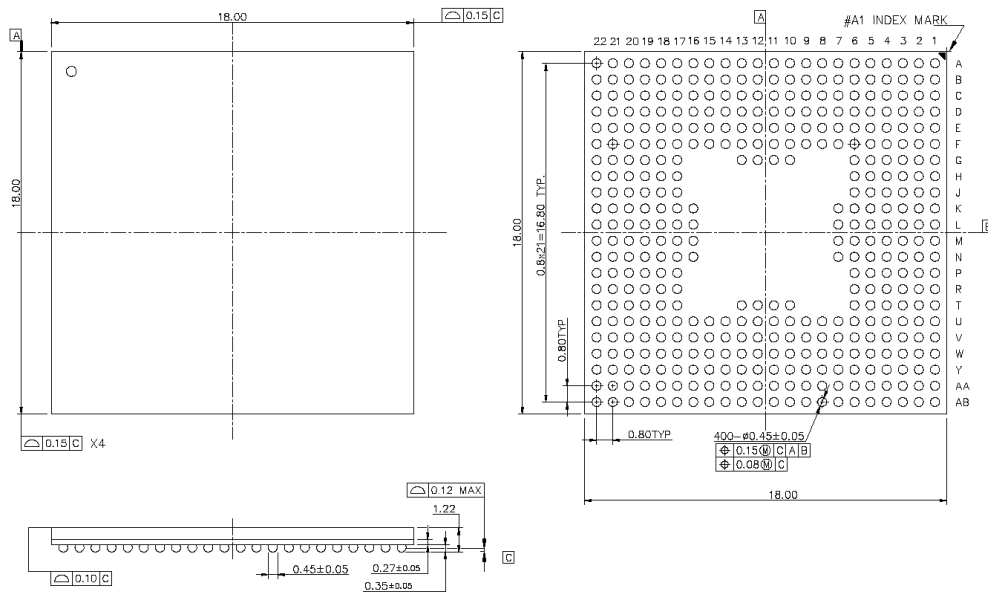
The role of the interrupt controller is to ask for the FIQ or IRQ interrupt requests to the ARM920T core after the arbitration process when there are multiple interrupt requests from internal peripherals and external interrupt request pins. The arbitration process is performed by the hardware priority logic and the result is written to the interrupt pending register.

CHAPTER 2

I/O PIN DESCRIPTIONS

2. I/O PIN DESCRIPTIONS

2.1 Mechanical Dimensions



Package Information

ITEM	DETAILS
UNIT	mm
Package Size	18.0TYP X 18.0TYP
Tolerance	±0.10
Ball Count	400 Balls
Ball Pitch	(x, y)=(0.8TYP, 0.8TYP)
Package Height	1.22TYP

Figure 2-1. MP2520F Package

2.2 MP2520F SIGNALS REFERENCE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VDD ADC	VDD OP	DP1	GPI O4	GPI O5	GPI O6	GPI O7	rRES ET	rPO RSEL	X44	X44	X44	X48	X49	X47	X45	X43	X41	X49	X47	GND	GND	A
B	VDDA PLL	AOI N1	AOI N8	AOI N4	DP0	GPI O1	GPI O8	GPI O8	GPI O10	SDC LK	X44	X44	X48	X48	X46	X44	X42	X40	X48	X46	X45	X44	B
C	XTRT C	XIO RTC	VSSA DC	AOI N0	AOI N2	DND	DP2	VDD AUV E2	VDD OP	GPI O11	rBAT TF	X44	X44	X44	X44	VDD OPA LME	GND	GND	GND	GND	X43	X42	C
D	X11	XIO	VDD LPLL	VSSA PLL	AOI N5	DND	VDD OP	GPI O8	VDD	GPI O13	EXTI ND	X44	X44	X40	X44	VDD OPA LME	GND	GND	GND	GND	X41	X40	D
E	GPI A6	GPI A4	VDD FPLL	VSSU PLL	GND	VREF	DN2	VDD	GPI O8	GPI O8	VDD	EXTI NL	VDD ALV EL	X41	X42	GND	GND	GND	GND	VDD OPA LME	X44	X44	E
F	GPI A7	GPI A11	VDD RTC	VSSR TC	VSSF PLL	GND	GND	GPI O8	GPI O4	GPI O4	VDD	rPW RSG LTO N	VDD OPA LME	GND	GND	GND	GND	GND	GND	VDD OPA LME	X47	X44	F
G	GPI A8	GPI A8	GPI A12	GPI A13	VDD OP	GPI A13	NC	NC	NC	GND	GPI O12	TEST _EN	VDD OPA LME	NC	NC	NC	GND	GND	SOX EX	VDD ALV EL	X44	X44	G
H	GPI A9	GPI A4	GPI A8	VDD	GPI A10	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	rSCS X1	rSCS X0	VDD OPA LME	X44	X44	H
J	GPI B4	GPI B13	VDD OP	GPI A9	GPI A9	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	rSW EX	rSPA SX	rSCA SX	X41	X44	J
K	GPI B8	GPI B10	GPI B13	GPI B13	GPI B13	GPI A11	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GND	SDQ M0	VDD	SDQ M0	SDQ M1	SDQ M2	K
L	GPI B7	GPI B4	GPI B8	GPI B8	GPI B8	VDD	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GND	GPI K8	GPI K11	GPI K2	GPI K3	GPI K4	L
M	GPI B2	GPI B11	GPI B11	VDD ALME 2	VDD OP	GPI B8	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPI J1	GPI J4	GPI J11	VDD OP	GPI K7	GPI K4	M
N	GPI B4	GPI B13	GPI B13	GPI B13	GPI B13	GPI B11	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPI J13	GPI J8	GPI J8	VDD	GPI J8	GPI K8	N
P	GPI B8	GPI B8	GPI B8	VDD	GPI B8	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDD	GPI J12	GPI J13	GPI J14	GPI J8	VDD ALME 2	P
R	GPI B10	GPI B4	GPI B10	GPI B10	GPI M4	VDD A820	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPI J9	GPI J8	GPI J12	GPI J8	GPI J8	R
T	GPI B10	GPI M8	GPI M1	GPI M8	VDD A820	GPI N8	NC	NC	NC	GND	GND	GND	GND	NC	NC	NC	GND	VDD A840	GPI J11	GPI J8	GPI J13	GPI J11	T
U	GPI M7	GPI M8	GPI N8	GPI N4	GPI N8	GND	GND	GND	VDD AUV E2	GND	GND	GPI B8	GPI B8	GND	GND	GND	GND	VDD OP	GPI J13	GPI J12	GPI J8	GPI J11	U
V	GPI M8	GPI M8	GPI N8	rGRE SET0	GND	GND	GPI H8	SDA	GPI C14	GPI C10	GPI C8	GPI B12	GPI B4	GPI F7	VDD A940	VDD	GPI C11	GND	GPI C8	GPI J14	GPI J8	VDD OP	V
W	GPI N7	GPI N2	GPI N1	GND	GND	GND	GPI H8	VDD A820	VDD A820	GPI C8	VDD	GPI B12	VDD	GPI B11	GPI F8	GPI C14	GPI C10	GND	GPI C8	GPI J14	GPI J8	GPI J11	W
Y	GPI N11	OW0	TD1	TDK	TMS	GPI O8	GPI H8	SCL	GPI C13	VDD OP	GPI B13	VDD OP	GPI B8	VDD AUV E2	VDD OP	GPI C14	GPI C8	GPI C8	GPI C8	GPI C8	GPI J11	GPI J8	Y
AA	TD0	VDD OP	TRST	GPI O8	GPI H8	EXTC LKIN	GPI C12	GPI C8	GPI C8	GPI C8	GPI C8	GPI B11	GPI B8	GPI F8	GPI F8	GPI F8	GPI F11	GPI F8	GPI C8	GPI C8	GPI C11	GPI C11	AA
AB	GPI C8	GPI C11	GPI H8	GPI H11	GPI C12	GPI C11	GPI C8	GPI C7	GPI C8	GPI C11	GPI B14	GPI B8	GPI B8	GPI B8	GPI F8	GPI F8	GPI F8	GPI F8	GPI F8	GPI C13	GPI C12	GPI C8	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 2-2. MP2520F Package FBGA Ball Map

Signal Name	Type	GPIO	Descriptions
Memory Controller Signals			
SDCLK_X	O	-	SDRAM clock
XA[14:0]	O	-	SDRAM address bus. This bus signals the address requested for memory accesses.
XD[15:0]	B	-	SDRAM data bus. XD[15:0] is used for 16-bit data mode.
XD[31:16]	B	-	SDRAM data bus. These data bits are used for 32-bit memory.
SCKEx	O	-	SDRAM clock enable.
nSCSx0	O	-	SDRAM CS for bank 0. This signal should be connected to the chip select (CS) pins for SDRAM.
nSCSx1	O	-	SDRAM CS for bank 1. This signal should be connected to the chip select (CS) pins for SDRAM.
NSRASx	O	-	SDRAM RAS. This signal should be connected to the row address strobe (RAS) pins for all banks of SDRAM.
NSCASx	O	-	SDRAM CAS. This signal should be connected to the column address strobe (CAS) pins for all banks of SDRAM.
NSWEx	O	-	SDRAM write enable. This signal should be connected to the write enables of SDRAM.
SDQMx[3:0]	O	-	SDRAM DQM for data bytes 0 through 3. These signals should be connected to the data output mask enables (DQM) for SDRAM
Display Controller Pins			
VD[23:8]	O	GPIOA[15:0]	Video output data (RGB, Multiplexed-RGB, YCbCr)
VD[7:0]	O	GPIOB[15:8]	Video output data (RGB, Multiplexed-RGB, YCbCr)
CLKH	O	GPIOB[7]	Pixel Clock Output
DE	O	GPIOB[6]	Data Enable
HSYNC	O	GPIOB[5]	Horizontal Sync
VSYN	O	GPIOB[4]	Vertical Sync
POL	O	GPIOB[3]	Data reverse signal of source driver
CLKV	O	GPIOB[2]	Vertical Clock output
PS	O	GPIOB[1]	Power Save
FG	O	GPIOB[0]	Clock signal of gate driver
XDOFF	O	GPIOH[6]	Gate-OFF Control signal for gate driver
VCLKIN	I	GPIOH[5]	Video Clock Input
STVD	B	GPIOK[7]	Shift clock output for Gate Driver IC
STHR	B	GPIOK[3]	Start Pulse of source Driver IC
Image Signal Processor Pins			

Signal Name	Type	GPIO	Descriptions
ID[15:0]	I	GPIOC[15:0]	Image Capture Data Input
ICKIN	I	GPIOH[4]	Image Clock In
IHSYNC	B	GPIOH[3]	Image HSYNC
IVSYNC	B	GPIOH[2]	Image VSYNC
ICKOUT	O	GPIOH[1]	Image Clock Out
UART Pins			
TX0	O	GPIOD[0]	UART0 Transmit Pin
RX0	I	GPIOD[1]	UART0 Receive Pin
nRIO	I	GPIOD[2]	UART1, UART2 Ring Indicator Pin
nDCD	I	GPIOD[3]	UART1, UART2 Data-Carrier-Detect Pin
nDSR	I	GPIOD[4]	UART1, UART2 Data-Set-Ready Pin
nDTR	O	GPIOD[5]	UART1, UART2 Data-Terminal-Ready Pin
nCTS	I	GPIOD[6]	UART1, UART2 Clear-To-Send Pin
nRTS	O	GPIOD[7]	UART1, UART2 Ready-To-Send Pin
TX1	O	GPIOD[8]	UART1 Transmit Pin
RX1	I	GPIOD[9]	UART1 Receive Pin
RX2	I	GPIOD[10]	UART2 Receive Pin
TX2	O	GPIOD[11]	UART2 Transmit Pin
RX3	I	GPIOD[12]	UART3 Receive Pin
TX3	O	GPIOD[13]	UART3 Transmit Pin
SIR Pins			
SIR RX	I	GPIOD[10]	SIR Receive Pin (SIR Mode)
SIR TX	O	GPIOD[11]	SIR Transmit Pin (SIR Mode)
PPM Pin			
PPM	I	GPION[13]	PPM Interface Pin
Non DRAM Controller Pins			
CD[15:0]	B	GPIOE[15:0]	Non DRAM Data Bus
CA[25:23](OM[3:1])	O	GPIOF[9:7]	Non DRAM Address Bus
CA[22:16]	O	GPIOF[6:0]	Non DRAM Address Bus
CA[15:1]	O	GPIOG[15:1]	Non DRAM Address Bus
CA[0](DQMz[0],BTENB0)	O	GPIOG[0]	Non DRAM Address Bus, Negative byte enable. This signal should be connected to the low byte enable for 16bit SRAM.
nPWAIT	I	GPIOI[13]	Wait Control for PCMCIA/CF/IDE/Static Memory. This signal is an input and is driven low by the PCMCIA/CF/IDE/ Static Memory to extend the length of the transfers to/from

Signal Name	Type	GPIO	Descriptions
			applications processor.
nPCS[1]	O	GPIO[7]	PCMCIA/CF Chip Select, This is used to select PCMCIA card, and enable the low byte lane.
nPCS[0]	O	GPIO[6]	PCMCIA/CF Chip Select. This is used to select PCMCIA card, and enable the High byte lane.
POE	O	GPIOJ[12]	PCMCIA/CF/SM Output Enable. This signal is an output and performs reads from memory and attribute space.
nPWE	O	GPIOJ[11]	PCMCIA/CF/SM Write Enable. This signal is an output and performs writes to memory and attribute space.
nPIOR	O	GPIOJ[10]	PCMCIA/CF/IDE I/O Read Enable. This signal is an output and performs read transactions from the PCMCIA I/O space.
nPIOW	O	GPIOJ[9]	PCMCIA/CF/IDE I/O Write Enable. This signal is an output and performs write transactions to the PCMCIA I/O space.
PSKSEL	O	GPIOJ[8]	PCMCIA/CF Socket Select. This signal is an output and is used by external steering logic to route control, address and data signals to one of the two PCMCIA sockets.
nPREG	O	GPIOJ[7]	PCMCIA/CF Register Select. This signal is an output and indicates that, on a memory transaction, the target address is attribute space. This signal has the same timing as address.
nPIOIS16	I	GPIOJ[6]	PCMCIA/CF/IDE Select 16bit Access. This signal is an input and is an acknowledgement from the PCMCIA card that the current address is a valid 16 bit wide I/O address.
RDnWR	O	GPIOJ[5]	Buffer Direction Control. Read/Write for static interface. Intended for use as a steering signal for buffering logic.
nBUFOE	O	GPIOJ[4]	Buffer Output Enable Intended for use as a buffer direction control for data bus buffering logic.
nBUFENB	O	GPIOJ[3]	Buffer Enable. Intended for use as a buffer enable for data bus buffering logic.
Static Memory Pins			
DQMz[1] (BTENB1)	O	GPIO[12]	Negative Byte Enable, This signal should be connected to the high byte enable for 16bit SRAM.
nSCS[3]	O	GPIO[11]	Static Memory Chip Select. This signal is chip selects to static memory devices such as ROM and Flash
nSCS[2]	O	GPIO[10]	Static Memory Chip Select. This signal is chip selects to static memory devices such as ROM and Flash
nSCS[1]	O	GPIO[9]	Static Memory Chip Select. This signal is chip selects to static memory devices such as ROM and Flash
nSCS[0]	O	GPIO[8]	Static Memory Chip Select. This is the chip select for the boot memory.
IDE Pins			
nICS[1]	O	GPIO[5]	IDE Chip Select. This is used to select PCMCIA card, and enable the High byte lane.
nICS[0]	O	GPIO[4]	IDE Chip Select. This is used to select PCMCIA card, and enable the low byte lane.
Nand Flash Pins			

Signal Name	Type	GPIO	Descriptions
nNFCE[3]	O	GPIO[3]	NAND Chip Select. This is chip selects to NAND Flash memory.
nNFCE[2]	O	GPIO[2]	NAND Chip Select This is chip selects to NAND Flash memory.
nNFCE[1]	O	GPIO[1]	NAND Chip Select This is chip selects to NAND Flash memory.
nNFCE[0]	O	GPIO[0]	NAND Chip Select This is chip selects to NAND Flash memory for NAND boot memory.
nPIOW/ALE	O	GPIO[9]	NAND ALE. This is address latch enable to NAND Flash memory
nPIOR/CLE	O	GPIO[10]	NAND CLE. This is command latch enable to NAND Flash memory
RnB	I	GPIO[2]	NAND Ready & Busy. This is Ready/Busy signal of NAND Flash memory.
nNFOE	O	GPIO[1]	NAND Output Enable
nNFW	O	GPIO[0]	NAND Write Enable
External DMA Pins			
DREQ[3:0]	I	GPIO[7:4]	DMA Request. This should be used as IDE DMA Request and Flyby DMA request.
DVAL[3:0]	O	GPIO[3:0]	DMA Validate. This should be used as Flyby DMA data valid strobes and IDE DMA Acknowledge signal.
PWM Pins			
PWMOUT[3:0]	O	GPIO[14:11]	Pulse Width Modulation channel
AC97 Controller Pins			
ABITCLK	I	GPIO[10]	AC97 Audio Port bit clock
ADATAIN	I	GPIO[9]	AC97 Audio Port data in
ASync	O	GPIO[8]	AC97 Audio Port sync signal
nARST	O	GPIO[7]	AC97 Audio Port reset signal
ADATOUT	O	GPIO[6]	AC97 Audio Port data out
I ² S Controller Pins			
I ² S CLK	O	GPIO[10]	I ² S Clock(QCLK_ I ² S)
I ² S DATAIN	I	GPIO[9]	I ² S SDATA IN
I ² S SYNC	O	GPIO[8]	I ² S SYNC
I ² S ACLK	O	GPIO[7]	I ² S System clock(ACLK_ I ² S)
I ² S DATAOUT	O	GPIO[6]	I ² S DATA OUT
MMC/SD Controller Pins			
SDCLK	O	GPIO[5]	MMC/SD Clock
SDCMD	B	GPIO[4]	MMC/SD Command
SDIDAT[3:0]	B	GPIO[3:0]	MMC/SD Data
656 Type Video Pins			
VD656[7:0]	B	GPIO[8:1]	656 Type Video Data

Signal Name	Type	GPIO	Descriptions
VDCLKIN	B	GPIO[0]	656 Type Video Clock
Transport Stream I/F Pins			
TSISYNC	I	GPIO[8]	MPEG I/F Sync
TSIDP	I	GPIO[7]	MPEG I/F Data Valid
TSIERR	I	GPIO[6]	MPEG I/F Error
TSIDIO	I	GPIO[5]	MPEG I/F Data bus (Serial Mode)
TSIDI[7:0]	I	GPIO[7:0]	MPEG I/F Data bus (Parallel Mode)
TSICLK	I	GPIO[4]	MPEG I/F Clock
Memory Stick Controller Pins			
MSBS	O	GPIO[3]	Memory Stick BS
MSDAT	B	GPIO[2]	Memory Stick SDAT
MSINS	I	GPIO[2]	Memory Stick INS
MSCLK	O	GPIO[1]	Memory Stick Clock
CDROM Controller Pins			
BCLK	I	GPIO[7]	CD I/F BCLK
LRCK	I	GPIO[8]	CD I/F LRCK
SDAT	I	GPIO[6]	CD I/F SDAT
SPDIF In/Out Pins			
SPDIFIN	I	GPIO[5]	SPDIF In
SPDIFOUT	O	GPIO[4]	SPDIF Out
SSP Pins			
SSPCLK	O	GPIO[3]	Synchronous Serial Port Clock
SSPFRM	O	GPIO[2]	Synchronous Serial Port Frame Signal
SSPTXD	O	GPIO[1]	Synchronous Serial Port Data
SSPRXD	I	GPIO[14]	Synchronous Serial Transmit Data
SSPEXTCLKIN	I	GPIO[12]	Synchronous Serial Port external clock input
One Wire Master Pin			
1WIRE	O	GPIO[0]	1-wire Master Output
Miscellaneous Pins			
EXTCLKO	O	GPIO[0]	External Clock Out
OM[3:0]	I	GPIO[9:7], OM0	Test Mode (External Clock selection)
TEST_EN	I	-	Test Mode Enable

Signal Name	Type	GPIO	Descriptions
nPORSEL	I	-	POWER On Reset Selection. This signal determines whether the internal POR circuit or nRESET is to be used. If nPORSEL is 0, the internal POR circuit would be used.
nRESET	I	-	Global Reset In. Active low input. nRESET is a level-sensitive input which is used to start the processor from a known address. A LOW level will cause the current instruction to terminate abnormally, and all on-chip state to be reset. When nRESET is driven HIGH, the processor will re-start from address 0.
nGRESETOut	O	-	Global Reset Out
nPWRRGLTOn	O	-	Active Low Power Control stop : 1 run : 0
EXTCLK	I	-	External Clock In
EXTIN0	I	-	Wake-up Control input #0
EXTIN1	I	-	Wake-up Control Input #1
nBATTF	I	-	Battery Fault. Active low input. Signals MP2520F that the main power source is failing (battery is low or is removed from the system.)
Crystal Pins			
XTI	I	-	7.3728Mhz Crystal In
XTO	O	-	7.3728Mhz Crystal Out
XTIRTC	I	-	32.768Khz RTC Crystal input
XTORTC	O	-	32.768Khz RTC Crystal output
JTAG Pins			
TCK	I	-	Clock input for the JTAG Logic
nTRST	I	-	Reset input for the JTAG Logic
TDO	O	-	Serial output for test instructions and data for JTAG
TMS	I	-	TMS controls the sequence of the TAP controller's state
TDI	I	-	Serial Data input for JTAG
Dedicated GPIO			
GPIOI[15]	B		GPIO : Dedicated GPIO(CBBUSREQ) ALT2 : 656IN[7]
GPIOI[14]	B		GPIO : Dedicated GPIO(CBBUSGNT) ALT2 : 656IN[6]
GPIOJ[15]	B		GPIO : Dedicated GPIO(CBREQ) ALT2 : 656IN[2]
GPIOJ[14]	B		GPIO : Dedicated GPIO(CBACK) ALT2 : 656IN[1]
GPIOJ[13]	B		GPIO : Dedicated GPIO(CBRDY) ALT2 : 656IN[0]
Power and Ground Pins			
VDDA920	SUP		ARM920T power supply
VDDA940	SUP		ARM940T power supply
VDDADC	SUP		ADC power supply
VDDALIVE1	SUP		Alive1 block power supply

Signal Name	Type	GPIO	Descriptions
VDDALIVE2	SUP		Alive2 block power supply
VDDAPLL	SUP		APLL power supply
VDDFPLL	SUP		FPLL power supply
VDDUPLL	SUP		UPLL power supply
VDDI	SUP		Internal logic power supply
VDDOP	SUP		I/O power supply
VDDOPALIVE	SUP		SDRAM I/O power supply
VDDRTC	SUP		RTC power supply
VSSADC	SUP		ADC ground
VSSAPLL	SUP		APLL ground
VSSFPLL	SUP		FPLL ground
VSSUPLL	SUP		UPLL ground
VSSRTC	SUP		RTC ground

TABLE 2-1. SIGNAL DESCRIPTIONS FOR MP2520F

GPIO Pins	Alternate Function1/Function2
GPIOA[15:0]	VD[23:8]
GPIOB[15:8]	VD[7:0]
GPIOB[7]	CLKH
GPIOB[6]	DE
GPIOB[5]	HSYNC
GPIOB[4]	VSYN
GPIOB[3]	POL
GPIOB[2]	CLKV
GPIOB[1]	PS
GPIOB[0]	FG
GPIOC[15:0]	ID[15:0]
GPIOD[0]	TX0
GPIOD[1]	RX0
GPIOD[2]	nRIO
GPIOD[3]	nDCD
GPIOD[4]	nDSR
GPIOD[5]	nDTR
GPIOD[6]	nCTS

GPIO Pins	Alternate Function1/Function2
GPIO[7]	nRTS
GPIO[8]	TX1
GPIO[9]	RX1
GPIO[10]	RX2
GPIO[11]	TX2
GPIO[12]	RX3/SSPEXTCLKIN
GPIO[13]	TX3
GPIOE[15:0]	CD[15:0]
GPIOF[9:7]	CA[25:23](OM[3:1])
GPIOF[6:0]	CA[22:16]
GPIOG[15:1]	CA[15:1]
GPIOG[0]	CA[0](DQMz[0], BTENB0)
GPIOH[6]	XDOFF
GPIOH[5]	VCLKIN
GPIOH[4]	ICLKIN
GPIOH[3]	IHSYNC
GPIOH[2]	IVSYNC
GPIOH[1]	ICLKOUT
GPIOH[0]	EXTCKLO
GPIOI[15]	Dedicated GPIO(CBBUSREQ)/ /656IN[7]
GPIOI[14]	Dedicated GPIO(CBBUSGNT)/ /656IN[6]
GPIOI[13]	nPWAIT
GPIOI[12]	DQMz[1] (BTENB1)
GPIOI[11]	nSCS[3]
GPIOI[10]	nSCS[2]
GPIOI[9]	nSCS[1]
GPIOI[8]	nSCS[0]
GPIOI[7]	nPCS[1]
GPIOI[6]	nPCS[0]
GPIOI[5]	nICS[1]
GPIOI[4]	nICS[0]
GPIOI[3]	nNFCE[3]/656IN[5]
GPIOI[2]	nNFCE[2]/656IN[4]
GPIOI[1]	nNFCE[1]/656IN[3]
GPIOI[0]	nNFCE[0]
GPIOJ[15]	Dedicated GPIO (CBREQ)/ /656IN[2]
GPIOJ[14]	Dedicated GPIO (CBACK)/ /656IN[1]
GPIOJ[13]	Dedicated GPIO (CBRDY)/ /656IN[0]
GPIOJ[12]	NPOE
GPIOJ[11]	NPWE
GPIOJ[10]	NPIOR

GPIO Pins	Alternate Function1/Function2
GPIOJ[9]	NPIOW
GPIOJ[8]	PSKSEL
GPIOJ[7]	NPREG
GPIOJ[6]	nPIOIS16
GPIOJ[5]	RDnWR
GPIOJ[4]	NBUFOE
GPIOJ[3]	nBUFENB
GPIOJ[2]	RnB
GPIOJ[1]	NNFOE
GPIOJ[0]	NNFWE
GPIOK[7]	DREQ3/STVD
GPIOK[6]	DREQ2
GPIOK[5]	DREQ1
GPIOK[4]	DREQ0
GPIOK[3]	DVAL3/STHR
GPIOK[2]	DVAL2/V656CLK
GPIOK[1]	DVAL1
GPIOK[0]	DVAL0
GPION[14]	PWMOUT3/SSPRXD
GPION[13]	PWMOUT2/PPM
GPION[12]	PWMOUT1
GPION[11]	PWMOUT0
GPION[10]	ABITCLK/ I ² S CLK
GPION[9]	ADATAIN/ I ² S DATAIN
GPION[8]	ASYNC/ I ² S SYNC
GPION[7]	nARST/ I ² S ACLK
GPION[6]	ADATOUT/ I ² S DATAOUT
GPION[5]	SDICLK
GPION[4]	SDICMD
GPION[3]	SDIDAT[3]/MSBS
GPION[2]	SDIDAT[2]/MSDAT
GPION[1]	SDIDAT[1]
GPION[0]	SDIDAT[0]
GPION[8]	VD656[7]/TSISYNC (LRCK)
GPION[7]	VD656[6]/TSIDP (BCLK)
GPION[6]	VD656[5]/TSIERR (SDAT)
GPION[5]	VD656[4]/TSIDIO
GPION[4]	VD656[3]/TSICLK
GPION[3]	VD656[2]
GPION[2]	VD656[1]

GPIO Pins	Alternate Function1/Function2
GPION[1]	VD656[0]
GPION[0]	VDCLKIN
GPION[7]	TSID[7]/TSISYNC
GPION[6]	TSID[6]/TSIDP
GPION[5]	TSID[5]/TSIERR (LRCK)
GPION[4]	TSID[4]/TSIDIO (BCK)
GPION[3]	TSID[3]/TSICLK (SDAT)
GPION[2]	TSID[2]/MSINS
GPION[1]	TSID[1]/MSCLK
GPION[0]	TSID[0]
GPIOO[5]	SPDIFIN
GPIOO[4]	SPDIFOUT
GPIOO[3]	SSPCLK
GPIOO[2]	SSPFRM
GPIOO[1]	SSPTXD
GPIOO[0]	1WIRE

TABLE 2-2. MP2520F GPIO PIN MAP

2.3 MP2520F I/O PIN LISTING

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
A1	VDDADC	SUP				
A2	VDDOP	SUP				
A3	DP1	IAOA	DP1	DP1	-	-
A4	GPIOO[4]/SPDIFOUT	ISOSZP	GPIOO[4]	GPIOO[4]	SPDIFOUT	-
A5	GPIOO[5]/SPDIFIN	ISOSZP	GPIOO[5]	GPIOO[5]	SPDIFIN	
A6	GPIOD[5]/nDTR	ISOSZP	GPIOD[5]	GPIOD[5]	nDTR	-
A7	GPIOD[7]/nRTS	ISOSZP	GPIOD[7]	GPIOD[7]	nRTS	-
A8	nRESET	IS	nRESET	nRESET	-	-
A9	nPORSEL	IS	nPORSEL	nPORSEL	-	-
A10	XA[1]	OS	XA[1]	XA[1]	-	-
A11	XA[4]	OS	XA[4]	XA[4]	-	-
A12	XA[9]	OS	XA[9]	XA[9]	-	-
A13	XD[31]	ISOS	XD[31]	XD[31]	-	-
A14	XD[29]	ISOS	XD[29]	XD[29]	-	-
A15	XD[27]	ISOS	XD[27]	XD[27]	-	-
A16	XD[25]	ISOS	XD[25]	XD[25]	-	-
A17	XD[23]	ISOS	XD[23]	XD[23]	-	-
A18	XD[21]	ISOS	XD[21]	XD[21]	-	-
A19	XD[19]	ISOS	XD[19]	XD[19]	-	-
A20	XD[17]	ISOS	XD[17]	XD[17]	-	-
A21	GND	SUP				
A22	GND	SUP				
B1	VDDAPLL	SUP				
B2	ADCIN1	IA	ADCIN1	ADCIN1	-	-
B3	ADCIN3	IA	ADCIN3	ADCIN3	-	-
B4	ADCIN4	IA	ADCIN4	ADCIN4	-	-
B5	DP0	IAOA	DP0	DP0	-	-
B6	GPIOD[1]/RX0	ISOSZP	GPIOD[1]	GPIOD[1]	RX0	-
B7	GPIOD[6]/nCTS	ISOSZP	GPIOD[6]	GPIOD[6]	nCTS	-
B8	GPIOD[9]/RX1	ISOSZP	GPIOD[9]	GPIOD[9]	RX1	-
B9	GPIOD[10]/RX2	ISOSZP	GPIOD[10]	GPIOD[10]	RX2	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
B10	SDCLK	OS	SDCLK	SDCLK	-	-
B11	XA[0]	OS	XA[0]	XA[0]	-	-
B12	XA[5]	OS	XA[5]	XA[5]	-	-
B13	XD[30]	ISOS	XD[30]	XD[30]	-	-
B14	XD[28]	ISOS	XD[28]	XD[28]	-	-
B15	XD[26]	ISOS	XD[26]	XD[26]	-	-
B16	XD[24]	ISOS	XD[24]	XD[24]	-	-
B17	XD[22]	ISOS	XD[22]	XD[22]	-	-
B18	XD[20]	ISOS	XD[20]	XD[20]	-	-
B19	XD[18]	ISOS	XD[18]	XD[18]	-	-
B20	XD[16]	ISOS	XD[16]	XD[16]	-	-
B21	XD[15]	ISOS	XD[15]	XD[15]	-	-
B22	XD[14]	ISOS	XD[14]	XD[14]	-	-
C1	XTIRTC	IS	XTIRTC	XTIRTC	-	-
C2	XTORTC	OS	XTORTC	XTORTC	-	-
C3	VSSADC	SUP				
C4	ADCIN0	IA	ADCIN0	ADCIN0	-	-
C5	ADCIN2	IA	ADCIN2	ADCIN2	-	-
C6	DN0	IAQA	DN0	DN0	-	-
C7	DP2	IAQA	DP2	DP2	-	-
C8	VDDALIVE2	SUP				
C9	VDDOP	SUP				
C10	GPIOD[11]/TX2	ISOSZP	GPIOD[11]	GPIOD[11]	TX2	-
C11	nBATTF	IS	nBATTF	nBATTF	-	-
C12	XA[2]	OS	XA[2]	XA[2]	-	-
C13	XA[6]	OS	XA[6]	XA[6]	-	-
C14	XA[8]	OS	XA[8]	XA[8]	-	-
C15	XBA[1]	OS	XBA[1]	XBA[1]	-	-
C16	VDDOPALIVE	SUP				
C17	GND	SUP				
C18	GND	SUP				
C19	GND	SUP				
C20	GND	SUP				
C21	XD[13]	ISOS	XD[13]	XD[13]	-	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
C22	XD[12]	ISOS	XD[12]	XD[12]	-	-
D1	XTI	IS	XTI	XTI	-	-
D2	XTO	OS	XTO	XTO	-	-
D3	VDDUPLL	SUP				
D4	VSSAPLL					
D5	ADCIN5	IA	ADCIN5	ADCIN5	-	-
D6	DN1	IAOA	DN1	DN1	-	-
D7	VDDOP	SUP				
D8	GPIOD[2]/nRIO	ISOSZP	GPIOD[2]	GPIOD[2]	nRIO	-
D9	VDDI	SUP				
D10	GPIOD[13]/TX3	ISOSZP	GPIOD[13]	GPIOD[13]	TX3	-
D11	EXTIN0	IS	EXTIN0	EXTIN0	-	-
D12	XA[3]	OS	XA[3]	XA[3]	-	-
D13	XA[7]	OS	XA[7]	XA[7]	-	-
D14	XA[10]	OS	XA[10]	XA[10]	-	-
D15	XBA[0]	OS	XBA[0]	XBA[0]	-	-
D16	VDDOPALIVE	SUP				
D17	GND	SUP				
D18	GND	SUP				
D19	GND	SUP				
D20	GND	SUP				
D21	XD[11]	ISOS	XD[11]	XD[11]	-	-
D22	XD[10]	ISOS	XD[10]	XD[10]	-	-
E1	GPIOA[9]/VD[17]	ISOSZP	GPIOA[9]	GPIOA[9]	VD[17]	-
E2	GPIOA[14]/VD[22]	ISOSZP	GPIOA[14]	GPIOA[14]	VD[17]	-
E3	VDDFPLL	SUP				
E4	VSSUPLL	SUP				
E5	GND	SUP				
E6	VREF	IA	VREF	VREF	-	-
E7	DN2	IAOA	DN2	DN2	-	-
E8	VDDI	SUP				
E9	GPIOD[3]/nDCD	ISOSZP	GPIOD[3]	GPIOD[3]	nDCD	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
E10	GPIOD[8]/TX1	ISOSZP	GPIOD[8]	GPIOD[8]	TX1	-
E11	VDDI	SUP				
E12	EXTIN1	IS	EXTIN1	EXTIN1	-	-
E13	VDDALIVE1	SUP				
E14	XA[11]	OS	XA[11]	XA[11]	-	-
E15	XA[12]	OS	XA[12]	XA[12]	-	-
E16	GND	SUP				
E17	GND	SUP				
E18	GND	SUP				
E19	GND	SUP				
E20	VDDOPALIVE	SUP				
E21	XD[9]	ISOS	XD[9]	XD[9]	-	-
E22	XD[8]	ISOS	XD[8]	XD[8]	-	-
F1	GPIOA[7]/VD[15]	ISOSZP	GPIOA[7]	GPIOA[7]	VD[15]	-
F2	GPIOA[11]/VD[19]	ISOSZP	GPIOA[11]	GPIOA[11]	VD[19]	-
F3	VDDRTC	SUP				
F4	VSSRTC					
F5	VSSFPLL	SUP				
F6	GND	SUP				
F7	GND	SUP				
F8	GPIOD[0]/TX0	ISOSZP	GPIOD[0]	GPIOD[0]	TX0	-
F9	GPIOD[4]/nDSR	ISOSZP	GPIOD[4]	GPIOD[4]	nDSR	-
F10	GPIOH[0]/EXTCLKO	ISOSZP	GPIOH[0]	GPIOH[0]	EXTCLKO	-
F11	VDDI	SUP				
F12	nPWRRGLTON	OS	nPWRRGLT On	nPWRRGLTO n	-	-
F13	VDDOPALIVE	SUP				
F14	GND	SUP				
F15	GND	SUP				
F16	GND	SUP				
F17	GND	SUP				
F18	GND	SUP				
F19	GND	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
F20	VDDOPALIVE	SUP				
F21	XD[7]	ISOS	XD[7]	XD[7]	-	-
F22	XD[6]	ISOS	XD[6]	XD[6]	-	-
G1	GPIOA[3]/VD[11]	ISOSZP	GPIOA[3]	GPIOA[3]	VD[11]	-
G2	GPIOA[8]/VD[16]	ISOSZP	GPIOA[8]	GPIOA[8]	VD[16]	-
G3	GPIOA[12]/VD[20]	ISOSZP	GPIOA[12]	GPIOA[12]	VD[20]	-
G4	GPIOA[13]/VD[21]	ISOSZP	GPIOA[13]	GPIOA[13]	VD[21]	-
G5	VDDOP	SUP				
G6	GPIOA[15]/VD[23]	ISOSZP	GPIOA[15]	GPIOA[15]	VD[23]	-
G10	GND	SUP				
G11	GPIOD[12]/RX3/SSPEXTCLKIN	ISOSZP	GPIOD[12]	GPIOD[12]	RX3	SSPEXT CLKIN
G12	TEST_EN	IS	TEST_EN	TEST_EN	-	-
G13	VDDOPALIVE	SUP				
G17	GND	SUP				
G18	GND	SUP				
G19	SCKEX	OS	SCKEx	SCKEx	-	-
G20	VDDALIVE1	SUP				
G21	XD[5]	ISOS	XD[5]	XD[5]	-	-
G22	XD[4]	ISOS	XD[4]	XD[4]	-	-
H1	GPIOA[0]/VD[8]	ISOSZP	GPIOA[0]	GPIOA[0]	VD[8]	-
H2	GPIOA[4]/VD[12]	ISOSZP	GPIOA[4]	GPIOA[4]	VD[12]	-
H3	GPIOA[6]/VD[14]	ISOSZP	GPIOA[6]	GPIOA[6]	VD[14]	-
H4	VDDI	SUP				
H5	GPIOA[10]/VD[18]	ISOSZP	GPIOA[10]	GPIOA[10]	VD[18]	-
H6	GND	SUP				
H17	GND	SUP				
H18	nSCSX1	OS	nSCSX1	nSCSX1	-	-
H19	nSCSX0	OS	nSCSX0	nSCSX0	-	-
H20	VDDOPALIVE	SUP				
H21	XD[3]	ISOS	XD[3]	XD[3]	-	-
H22	XD[2]	ISOS	XD[2]	XD[2]	-	-
J1	GPIOB[14]/VD[6]	ISOSZP	GPIOB[14]	GPIOB[14]	VD[6]	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
J2	GPIOB[15]/VD[7]	ISOSZP	GPIOB[15]	GPIOB[15]	VD[7]	-
J3	VDDOP	SUP				
J4	GPIOA[2]/VD[10]	ISOSZP	GPIOA[2]	GPIOA[2]	VD[10]	-
J5	GPIOA[5]/VD[13]	ISOSZP	GPIOA[5]	GPIOA[5]	VD[13]	-
J6	GND	SUP				
J17	GND	SUP				
J18	nSWEX	OS	nSWEx	nSWEx	-	-
J19	nSRASX	OS	nSRASx	nSRASx	-	-
J20	nSCASX	OS	nSCASx	nSCASx	-	-
J21	XD[1]	ISOS	XD[1]	XD[1]	-	-
J22	XD[0]	ISOS	XD[0]	XD[0]	-	-
K1	GPIOB[8]/VD[0]	ISOSZP	GPIOB[8]	GPIOB[8]	VD[0]	-
K2	GPIOB[11]/VD[3]	ISOSZP	GPIOB[11]	GPIOB[11]	VD[3]	-
K3	GPIOB[12]/VD[4]	ISOSZP	GPIOB[12]	GPIOB[12]	VD[4]	-
K4	GPIOB[13]/VD[5]	ISOSZP	GPIOB[13]	GPIOB[13]	VD[5]	-
K5	GPIOB[10]/VD[2]	ISOSZP	GPIOB[10]	GPIOB[10]	VD[2]	-
K6	GPIOA[1]/VD[9]	ISOSZP	GPIOA[1]	GPIOA[1]	VD[9]	-
K7	GND	SUP				
K16	GND	SUP				
K17	GND	SUP				
K18	SDQMx0	OS	SDQMx0	SDQMx0	-	-
K19	VDDI	SUP				
K20	SDQMx3	OS	SDQMx3	SDQMx3	-	-
K21	SDQMx1	OS	SDQMx1	SDQMx1	-	-
K22	SDQMx2	OS	SDQMx2	SDQMx2	-	-
L1	GPIOB[7]/CLKH	ISOSZP	GPIOB[7]	GPIOB[7]	CLKH	-
L2	GPIOB[4]/VSYNC	ISOSZP	GPIOB[4]	GPIOB[4]	VSYNC	-
L3	GPIOB[6]/DE	ISOSZP	GPIOB[6]	GPIOB[6]	DE	-
L4	GPIOB[5]/HSYNC	ISOSZP	GPIOB[5]	GPIOB[5]	HSYNC	-
L5	GPIOB[9]/VD[1]	ISOSZP	GPIOB[9]	GPIOB[9]	VD[1]	-
L6	VDDI	SUP				
L7	GND	SUP				
L16	GND	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
L17	GND	SUP				
L18	GPIOK[5]/DREQ1	ISOSZP	GPIOK[5]	GPIOK[5]	DREQ1	-
L19	GPIOK[1]/DVAL1	ISOSZP	GPIOK[1]	GPIOK[1]	DVAL1	-
L20	GPIOK[2]/DVAL2/V656CLK	ISOSZP	GPIOK[2]	GPIOK[2]	DVAL2	V656CLK
L21	GPIOK[3]/DVAL3/STHR	ISOSZP	GPIOK[3]	GPIOK[3]	DVAL3	STHR
L22	GPIOK[0]/DVAL0	ISOSZP	GPIOK[0]	GPIOK[0]	DVAL0	-
M1	GPIOB[2]/CLKV	ISOSZP	GPIOB[2]	GPIOB[2]	CLKV	-
M2	GPIOB[0]/FG	ISOSZP	GPIOB[0]	GPIOB[0]	FG	-
M3	GPIOB[1]/PS	ISOSZP	GPIOB[1]	GPIOB[1]	PS	-
M4	VDDALIVE2	SUP				
M5	VDDOP	SUP				
M6	GPIOB[3]/POL	ISOSZP	GPIOB[3]	GPIOB[3]	POL	-
M7	GND	SUP				
M16	GND	SUP				
M17	GPIOJ[0]/nNFWE	ISOSZP	GPIOJ[0]	GPIOJ[0]	nNFWE	-
M18	GPIOJ[4]/nBUFOE	ISOSZP	GPIOJ[4]	GPIOJ[4]	nBUFOE	-
M19	GPIOJ[1]/nNFOE	ISOSZP	GPIOJ[1]	GPIOJ[1]	nNFOE	-
M20	VDDOP	SUP				
M21	GPIOK[7]/DREQ3/STVD	ISOSZP	GPIOK[7]	GPIOK[7]	DREQ3	STVD
M22	GPIOK[4]/DREQ0	ISOSZP	GPIOK[4]	GPIOK[4]	DREQ0	-
N1	GPIO_L[14]/PWMOUT3/SSPRXD	ISOSZP	GPIO_L[14]	GPIO_L[14]	PWMOUT3	SSPRXD
N2	GPIO_L[13]/PWMOUT2/PPM	ISOSZP	GPIO_L[13]	GPIO_L[13]	PWMOUT2	PPM
N3	GPIO_L[10]/ABITCLK/I ² S CLK	ISOSZP	GPIO_L[10]	GPIO_L[10]	ABITCLK	-
N4	GPIO_L[11]/PWMOUT0	ISOSZP	GPIO_L[11]	GPIO_L[11]	PWMOUT0	-
N5	GPIO_L[12]/PWMOUT1	ISOSZP	GPIO_L[12]	GPIO_L[12]	PWMOUT1	-
N6	GPIO_L[7]/nARST/I ² S ACLK	ISOSZP	GPIO_L[7]	GPIO_L[7]	nARST	-
N7	GND	SUP				
N16	GND	SUP				
N17	GPIOJ[10]/nPJOR	ISOSZP	GPIOJ[10]	GPIOJ[10]	nPJOR	-
N18	GPIOJ[8]/PSKSEL	ISOSZP	GPIOJ[8]	GPIOJ[8]	PSKSEL	-
N19	GPIOJ[5]/RDNWR	ISOSZP	GPIOJ[5]	GPIOJ[5]	RDNWR	-
N20	VDDI	SU				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
N21	GPIOJ[2]/RNB	ISOSZP	GPIOJ[2]	GPIOJ[2]	RnB	-
N22	GPIOK[6]/DREQ2	ISOSZP	GPIOK[6]	GPIOK[6]	DREQ2	-
P1	GPIOI[9]/ADATAIN/ I ² S DATAIN	ISOSZP	GPIOI[9]	GPIOI[9]	ADATAIN	-
P2	GPIOI[8]/ASYNC/ I ² S SYNC	ISOSZP	GPIOI[8]	GPIOI[8]	ASYNC	-
P3	GPIOI[5]/SDICLK	ISOSZP	GPIOI[5]	GPIOI[5]	SDICLK	-
P4	VDDI	SUP				
P5	GPIOI[3]/SDIDAT[3]/MSBS	ISOSZP	GPIOI[3]	GPIOI[3]	SDIDAT[3]	MSBS
P6	GND	SUP				
P17	VDDI	SUP				
P18	GPIOJ[12]/nPOE	ISOSZP	GPIOJ[12]	GPIOJ[12]	nPOE	-
P19	GPIOJ[13](CBRDY)/ 656IN[0]	ISOSZP	GPIOJ[13]	GPIOJ[13] (CBRDY)		656IN[0]
P20	GPIOJ[14](CBACK)/ 656IN[1]	ISOSZP	GPIOJ[14]	GPIOJ[14] (CBACK)		656IN[1]
P21	GPIOJ[3]/nBUFENB	ISOSZP	GPIOJ[3]	GPIOJ[3]	nBUFENB	-
P22	VDDALIE2	SUP				
R1	GPIOI[6]/ADATOUT/ I ² S DATAOUT	ISOSZP	GPIOI[6]	GPIOI[6]	ADATOUT	-
R2	GPIOI[4]/SDICMD	ISOSZP	GPIOI[4]	GPIOI[4]	SDICMD	-
R3	GPIOI[0]/SDIDAT[0]	ISOSZP	GPIOI[0]	GPIOI[0]	SDIDAT[0]	-
R4	GPIOI[1]/SDIDAT[1]	ISOSZP	GPIOI[1]	GPIOI[1]	SDIDAT[1]	-
R5	GPIOI[4]/VD656[3]/TSICLK	ISOSZP	GPIOI[4]	GPIOI[4]	VD656[3]	TSICLK
R6	VDDA920	SUP				
R17	GND	SUP				
R18	GPIOI[4]/nICS[0]	ISOSZP	GPIOI[4]	GPIOI[4]	nICS[0]	-
R19	GPIOI[5]/nICS[1]	ISOSZP	GPIOI[5]	GPIOI[5]	nICS[1]	-
R20	GPIOI[2]/nNFCE[2]/656IN[4]	ISOSZP	GPIOI[2]	GPIOI[2]	nNFCE[2]	656IN[4]
R21	GPIOJ[9]/nPLOW	ISOSZP	GPIOJ[9]	GPIOJ[9]	nPLOW	-
R22	GPIOJ[6]/nPLOIS16	ISOSZP	GPIOJ[6]	GPIOJ[6]	nPLOIS16	-
T1	GPIOI[2]/SDIDAT[2]/MSDAT	ISOSZP	GPIOI[2]	GPIOI[2]	SDIDAT[2]	MSDAT
T2	GPIOI[8]/VD656[7]/TSISYNC(LRCK)	ISOSZP	GPIOI[8]	GPIOI[8]	VD656[7]	TSISYNC (LRCK)
T3	GPIOI[1]/VD656[0]	ISOSZP	GPIOI[1]	GPIOI[1]	VD656[0]	-
T4	GPIOI[2]/VD656[1]	ISOSZP	GPIOI[2]	GPIOI[2]	VD656[1]	-
T5	VDDA920	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
T6	GPIO[M6]/VD656[5]/TSIERR(SDAT)	ISOSZP	GPIO[M6]	GPIO[M6]	VD656[5]	TSIERR (SDAT)
T10	GND	SUP				
T11	GND	SUP				
T12	GND	SUP				
T13	GND	SUP				
T17	GND	SUP				
T18	VDDA940	SUP				
T19	GPIO[L7]/nPCS[1]	ISOSZP	GPIO[L7]	GPIO[L7]	nPCS[1]	-
T20	GPIO[L6]/nPCS[0]	ISOSZP	GPIO[L6]	GPIO[L6]	nPCS[0]	-
T21	GPIO[J15] (CBREQ) / 656IN[2]	ISOSZP	GPIO[J15]	GPIO[J15] (CBREQ)		656IN[2]
T22	GPIO[J7]/nPREG	ISOSZP	GPIO[J7]	GPIO[J7]	nPREG	-
U1	GPIO[M7]/VD656[6]/TSIDP (BCLK)	ISOSZP	GPIO[M7]	GPIO[M7]	VD656[6]	TSIDP (BCLK)
U2	GPIO[M5]/VD656[4]/TSID0	ISOSZP	GPIO[M5]	GPIO[M5]	VD656[4]	TSID0
U3	GPION[6]/TSID[6]/TSIDP	ISOSZP	GPION[6]	GPION[6]	TSID[6]	TSIDP
U4	GPION[4]/TSID[4]/TSID0 (BCLK)	ISOSZP	GPION[4]	GPION[4]	TSID[4]	TSID0 (BCLK)
U5	GPION[5]/TSID[5]/TSIERR (LRCK)	ISOSZP	GPION[5]	GPION[5]	TSID[5]	TSIERR (LRCK)
U6	GND	SUP				
U7	GND	SUP				
U8	GND	SUP				
U9	VDDALIVE2	SUP				
U10	GND	SUP				
U11	GND	SUP				
U12	GPIO[E8]/ZD[8]	ISOSZP	GPIO[E8]	GPIO[E8]	CD[8]	-
U13	GPIO[E0]/ZD[0]	ISOSZP	GPIO[E0]	GPIO[E0]	CD[0]	-
U14	GND	SUP				
U15	GND	SUP				
U16	GND	SUP				
U17	GND	SUP				
U18	VDDOP	SUP				

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Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
U19	GPIO[13]/nPWAIT	ISOSZP	GPIO[13]	GPIO[13]	nPWAIT	-
U20	GPIO[12]/DQMZ1(BTENB1)	ISOSZP	GPIO[12]	GPIO[12]	DQMZ1 (BTENB1)	-
U21	GPIO[0]/nNFCE[0]	ISOSZP	GPIO[0]	GPIO[0]	nNFCE[0]	-
U22	GPIOJ[11]/nPWE	ISOSZP	GPIOJ[11]	GPIOJ[11]	nPWE	-
V1	GPION[3]/VD656[2]	ISOSZP	GPION[3]	GPION[3]	VD656[2]	-
V2	GPION[0]/VDCLKIN	ISOSZP	GPION[0]	GPION[0]	VDCLKIN	-
V3	GPION[3]/TSID[3]/TSICLK (SDAT)	ISOSZP	GPION[3]	GPION[3]	TSID[3]	TSICLK (SDAT)
V4	nGRESETOut	OS	nGRESETOut	nGRESETOut	-	-
V5	GND	SUP				
V6	GND	SUP				
V18	GND	SUP				
V7	GPIOH[3]/IHSYNC	ISOSZP	GPIOH[3]	GPIOH[3]	IHSYNC	-
V8	SDA	OD	SDA	SDA	-	-
V9	GPIOC[14]/ID[14]	ISOSZP	GPIOC[14]	GPIOC[14]	ID[14]	-
V10	GPIOC[10]/ID[10]	ISOSZP	GPIOC[10]	GPIOC[10]	ID[10]	-
V11	GPIOC[2]/ID[2]	ISOSZP	GPIOC[2]	GPIOC[2]	ID[2]	-
V12	GPIOE[12]/ZD[12]	ISOSZP	GPIOE[12]	GPIOE[12]	CD[12]	-
V13	GPIOE[4]/ZD[4]	ISOSZP	GPIOE[4]	GPIOE[4]	CD[4]	-
V14	GPIOF[7]/ZA[23]/OM[1]	ISOSZP	GPIOF[7]	GPIOF[7]	CA[23]	OM[1]
V15	VDDA940	SUP				
V16	VDDI	SUP				
V17	GPIOG[11]/ZA[11]	ISOSZP	GPIOG[11]	GPIOG[11]	CA[11]	-
V19	GPIOG[2]/ZA[2]	ISOSZP	GPIOG[2]	GPIOG[2]	CA[2]	-
V20	GPIO[15](CBBUSREQ)/ 656IN[7]	ISOSZP	GPIO[15]	GPIO[15] (CBBUSREQ)		656IN[7]
V21	GPIO[3]/nNFCE[3]/656IN[5]	ISOSZP	GPIO[3]	GPIO[3]	nNFCE[3]	656IN[5]
V22	VDDOP	SUP				
W1	GPION[7]/TSID[7]/TSISYNC	ISOSZP	GPION[7]	GPION[7]	TSID[7]	TSISYNC
W2	GPION[2]/TSID[2]/MSINS	ISOSZP	GPION[2]	GPION[2]	TSID[2]	MSINS
W3	GPION[0]/TSID[0]	ISOSZP	GPION[0]	GPION[0]	TSID[0]	-
W4	GND	SUP				
W5	GND	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
W6	GND	SUP				
W7	GPIOH[5]/VCLKIN	ISOSZP	GPIOH[5]	GPIOH[5]	VCLKIN	-
W8	VDDA920	SUP				
W9	VDDA920	SUP				
W10	GPIOC[5]/ID[5]	ISOSZP	GPIOC[5]	GPIOC[5]	ID[5]	-
W11	VDDI	SUP				
W12	GPIOE[13]/ZD[13]	ISOSZP	GPIOE[13]	GPIOE[13]	CD[13]	-
W13	VDDI	SUP				
W14	GPIOE[1]/ZD[1]	ISOSZP	GPIOE[1]	GPIOE[1]	CD[1]	-
W15	GPIOF[5]/ZA[21]	ISOSZP	GPIOF[5]	GPIOF[5]	CA[21]	-
W16	GPIOG[14]/ZA[14]	ISOSZP	GPIOG[14]	GPIOG[14]	CA[14]	-
W17	GPIOG[10]/ZA[10]	ISOSZP	GPIOG[10]	GPIOG[10]	CA[10]	-
W18	GND	SUP				
W19	GPIOG[5]/ZA[5]	ISOSZP	GPIOG[5]	GPIOG[5]	CA[5]	-
W20	GPIOI[14] (CBBUSGNT) / 656IN[6]	ISOSZP	GPIOI[14]	GPIOI[14] (CBBUSGNT)		656IN[6]
W21	GPIOI[8]/nSCS[0]	ISOSZP	GPIOI[8]	GPIOI[8]	nSCS[0]	-
W22	GPIOI[1]/nNFCE[1]/656IN[3]	ISOSZP	GPIOI[1]	GPIOI[1]	nNFCE[1]	656IN[3]
Y1	GPION[1]/TSID[1]/MSCLK	ISOSZP	GPION[1]	GPION[1]	TSID[1]	MSCLK
Y2	OM0	OS	OM0	OM0	-	-
Y3	TDI	IS	TDI	TDI	-	-
Y4	TCK	IS	TCK	TCK	-	-
Y5	TMS	IS	TMS	TMS	-	-
Y6	GPIOO[2]/SSPFRM	ISOSZP	GPIOO[2]	GPIOO[2]	SSPFRM	-
Y7	GPIOH[4]/ICLKIN	ISOSZP	GPIOH[4]	GPIOH[4]	ICLKIN	
Y8	SCL	OD	SCL	SCL	-	-
Y9	GPIOC[13]/ID[13]	ISOSZP	GPIOC[13]	GPIOC[13]	ID[13]	-
Y10	VDDOP	SUP				
Y11	GPIOE[15]/ZD[15]	ISOSZP	GPIOE[15]	GPIOE[15]	CD[15]	-
Y12	VDDOP	SUP				
Y13	GPIOE[6]/ZD[6]	ISOSZP	GPIOE[6]	GPIOE[6]	CD[6]	-
Y14	VDDALIVE2	SUP				
Y15	VDDOP	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
Y16	GPIOG[15]/ZA[15]	ISOSZP	GPIOG[15]	GPIOG[15]	CA[15]	-
Y17	GPIOG[9]/ZA[9]	ISOSZP	GPIOG[9]	GPIOG[9]	CA[9]	-
Y18	GPIOG[8]/ZA[8]	ISOSZP	GPIOG[8]	GPIOG[8]	CA[8]	-
Y19	GPIOG[4]/ZA[4]	ISOSZP	GPIOG[4]	GPIOG[4]	CA[4]	-
Y20	GPIOG[3]/ZA[3]	ISOSZP	GPIOG[3]	GPIOG[3]	CA[3]	-
Y21	GPIOI[11]/nSCS[3]	ISOSZP	GPIOI[11]	GPIOI[11]	nSCS[3]	-
Y22	GPIOI[9]/nSCS[1]	ISOSZP	GPIOI[9]	GPIOI[9]	nSCS[1]	-
AA1	TDO	OSZ	TDO	TDO	-	-
AA2	VDDOP	SUP				
AA3	NTRST	IS	nTRST	nTRST	-	-
AA4	GPIOO[0]/1WIRE	OD	GPIOO[0]	GPIOO[0]	1WIRE	-
AA5	GPIOH[2]/IVSYNC	ISOSZP	GPIOH[2]	GPIOH[2]	IVSYNC	-
AA6	EXTCLKIN	IS	EXTCLKIN	EXTCLKIN		-
AA7	GPIOC[12]/ID[12]	ISOSZP	GPIOC[12]	GPIOC[12]	ID[12]	-
AA8	GPIOC[9]/ID[9]	ISOSZP	GPIOC[9]	GPIOC[9]	ID[9]	-
AA9	GPIOC[6]/ID[6]	ISOSZP	GPIOC[6]	GPIOC[6]	ID[6]	-
AA10	GPIOC[4]/ID[4]	ISOSZP	GPIOC[4]	GPIOC[4]	ID[4]	-
AA11	GPIOC[0]/ID[0]	ISOSZP	GPIOC[0]	GPIOC[0]	ID[0]	-
AA12	GPIOE[10]/ZD[10]	ISOSZP	GPIOE[10]	GPIOE[10]	CD[10]	-
AA13	GPIOE[7]/ZD[7]	ISOSZP	GPIOE[7]	GPIOE[7]	CD[7]	-
AA14	GPIOE[3]/ZD[3]	ISOSZP	GPIOE[3]	GPIOE[3]	CD[3]	-
AA15	GPIOF[9]/ZA[25]/OM[3]	ISOSZP	GPIOF[9]	GPIOF[9]	CA[25]	OM[3]
AA16	GPIOF[4]/ZA[20]	ISOSZP	GPIOF[4]	GPIOF[4]	CA[20]	-
AA17	GPIOF[1]/ZA[17]	ISOSZP	GPIOF[1]	GPIOF[1]	CA[17]	-
AA18	GPIOF[0]/ZA[16]	ISOSZP	GPIOF[0]	GPIOF[0]	CA[16]	-
AA19	GPIOG[7]/ZA[7]	ISOSZP	GPIOG[7]	GPIOG[7]	CA[7]	-
AA20	GPIOG[6]/ZA[6]	ISOSZP	GPIOG[6]	GPIOG[6]	CA[6]	-
AA21	GPIOG[1]/ZA[1]	ISOSZP	GPIOG[1]	GPIOG[1]	CA[1]	-
AA22	GPIOI[10]/nSCS[2]	ISOSZP	GPIOI[10]	GPIOI[10]	nSCS[2]	-
AB1	GPIOO[3]/SSPCLK	ISOSZP	GPIOO[3]	GPIOO[3]	SSPCLK	-
AB2	GPIOO[1]/SSPTXD	ISOSZP	GPIOO[1]	GPIOO[1]	SSPTXD	-
AB3	GPIOH[6]/XDOFF	ISOSZP	GPIOH[6]	GPIOH[6]	XDOFF	-
AB4	GPIOH[1]/ICLKOUT	ISOSZP	GPIOH[1]	GPIOH[1]	ICLKOUT	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
AB5	GPIOC[15]/ID[15]	ISOSZP	GPIOC[15]	GPIOC[15]	ID[15]	-
AB6	GPIOC[11]/ID[11]	ISOSZP	GPIOC[11]	GPIOC[11]	ID[11]	-
AB7	GPIOC[8]/ID[8]	ISOSZP	GPIOC[8]	GPIOC[8]	ID[8]	-
AB8	GPIOC[7]/ID[7]	ISOSZP	GPIOC[7]	GPIOC[7]	ID[7]	-
AB9	GPIOC[3]/ID[3]	ISOSZP	GPIOC[3]	GPIOC[3]	ID[3]	-
AB10	GPIOC[1]/ID[1]	ISOSZP	GPIOC[1]	GPIOC[1]	ID[1]	-
AB11	GPIOE[14]/ZD[14]	ISOSZP	GPIOE[14]	GPIOE[14]	CD[14]	-
AB12	GPIOE[11]/ZD[11]	ISOSZP	GPIOE[11]	GPIOE[11]	CD[11]	-
AB13	GPIOE[9]/ZD[9]	ISOSZP	GPIOE[9]	GPIOE[9]	CD[9]	-
AB14	GPIOE[5]/ZD[5]	ISOSZP	GPIOE[5]	GPIOE[5]	CD[5]	-
AB15	GPIOE[2]/ZD[2]	ISOSZP	GPIOE[2]	GPIOE[2]	CA[24]	-
AB16	GPIOF[8]/ZA[24]/OM[2]	ISOSZP	GPIOF[8]	GPIOF[8]	CA[24]	OM[2]
AB17	GPIOF[6]/ZA[22]	ISOSZP	GPIOF[6]	GPIOF[6]	CA[22]	-
AB18	GPIOF[3]/ZA[19]	ISOSZP	GPIOF[3]	GPIOF[3]	CA[19]	-
AB19	GPIOF[2]/ZA[18]	ISOSZP	GPIOF[2]	GPIOF[2]	CA[18]	-
AB20	GPIOG[13]/ZA[13]	ISOSZP	GPIOG[13]	GPIOG[13]	CA[13]	-
AB21	GPIOG[12]/ZA[12]	ISOSZP	GPIOG[12]	GPIOG[12]	CA[12]	-
AB22	GPIOG[0]/ZA[0] (DQMz[0], BTENB0)	ISOSZP	GPIOG[0]	GPIOG[0]	CA[0] (DQMz[0], BTE NB0)	-

TABLE 2-3. MP2520F PIN OUT – BALLPAD NUMBER ORDER

- IA : Analog Input
- OA : Analog Output
- IAOA : Analog Input/Output
- IS : Schmitt trigger Input
- OS : Schmitt trigger Output
- ISOS : Schmitt trigger Input/Output
- ISOSZP : Schmitt trigger Input/Output Tri-state Pull-up enable
- OD : Open Drain
- SUP : Supply

2.4 SYSTEM CONFIGURATION

Pin Name	Ball	Function Name	Description
GPIOA[14]/VD[22]	E2	RstCfgNFBoot	Nand Boot Enable
GPIOA[13]/VD[21]	G4	RstCfgNFBSize	Nand Boot Size : 0 : 2048byte, 1 : 4096byte
GPIOA[12]/VD[20]	G3	RstCfgNFBUSWidth	Nand flash Bus Width : 0 : 8bit, 1 : 16bit
GPIOA[11]/VD[19]	F2	RstCfgNFType	Nand flash Type : 0 : 3 Address, 1 : 4 Address
GPIOA[10]/VD[18]	H5	RstCfgSR0BUSWidth	SRAM Bus Width : 0 : 8bit, 1 : 16 bit
GPIOA[9]/VD[17]	E1	RstCfgSDRTYPE	SDRAM Type 0 : Full up / Full Down
GPIOA[8]/VD[16]	G2	RstCfgBUSCBW	SDRAM Total Bus Width 0 : 16 bit 1 : 32 bit
GPIOA[7]/VD[15]	F1	RstCfgSDRBW[1]	SDRAM Bus Width 00 : 4bit, 01 : 8bit, 10 : 16bit
GPIOA[6]/VD[14]	H3	RstCfgSDRBW[0]	
GPIOA[5]/VD[13]	J5	RstCfgSDRCAP[1]	SDRAM Capacity 00 : 64Mbit, 01 : 128Mbit, 10 : 256 Mbit, 11 : 512 Mbit
GPIOA[4]/VD[12]	H2	RstCfgSDRCAP[0]	
GPIOA[3]/VD[11]	G1	RstCfgShadow	SDRAM Shadow Enable,
GPIOA[1]/VD[9]	K6	RstCfgUARTBootClk	UART Boot Clock : 0 : PLL clock, 1 : ABITCLK
GPIOA[0]/VD[8]	H1	RstCfgBootDown	UART Boot Enable : 0
GPIOB[15]/VD[7]	J2	ARM940T DEBUG Enable	ARM940 ICE Debug Enable : 0
GPIOB[14]/VD[6]	J1	RstCfgSRBuf	SRAM Buffer Enable
GPIOB[13]/VD[5]	K4	RstCfgNFBuf	Nand flash Buffer Enable

TABLE 2-4. SYSTEM CONFIGURATION

2.5 TEST MODE PINS

Pin Name	Ball	Function Name	Description
TEST_EN	G12	Test Enable	0 : Normal mode 1 : Test mode
OM0	Y2	External Clock Enable for FCLK	0 : PLL clock enable 1 : External Clock enable
GPIOF[9]/ZA[25]	AA15	OM[3]	If TEST_EN is high this signals are used test pins.
GPIOF[8]/ZA[24]	AB16	OM[2]	If TEST_EN is high this signals are used test pins
GPIOF[7]/ZA[23]	V14	OM[1]	If TEST_EN is high this signals are used test pins

TABLE 2-5. TEST MODE PINS

2.6 PIN DESCRIPTION NOTES

GPIO Reset Operation

After reset, all GPIO pins except GPIOD[1:0], GPIOE[15:0], GPIOF[9:0], GPIOG[15:0], GPIOH[0], GPIOI[15:0], GPIOJ[15:0], and GPIOL[10], will be set to input. The default values of the excepted GPIO pins are as follows:

GPIOD[1:0] : Alt Function 1

GPIOE[15:8] : Alt Function 1 for SRAM Boot and the 16bit SRAM Bus Width. Otherwise, the default value will be GPIO input

GPIO[9:0] : Alt Function 1 for SRAM Boot. Otherwise, the default value will be GPIO Input

GPIOG[15:0] : Alt Function 1 for SRAM Boot. Otherwise, the default value will be the GPIO Input

If the GPIO Alt. Function Register is set, the GPIO pins are used as the alternative function.

GPIO Stop Mode Operation

In Stop mode, GPIO states of all pins are determined by the values of GPIO Alt. Function Register and GPIO Output Register, except for the GPIOE, GPIOF, GPIOG, GPIOI, and GPIOJ pins, the states of which are determined by the value of GPIO Alive Register.

DC- ELECTRICAL CHARACTERISTICS

 $V_{DDOP} = 3.3V$

Symbol	Paramente	Condition	Min	Type	Max	Unit
V _{IH}	High level input voltage					V
	LVC MOS interface		1.27			
V _{IL}	Low level input voltage					V
	LVC MOS interface				0.57	
VT	Switchig threshold			0.5VDD		V
VT+	Schmitt trigger,positive-going threshold	CMOS			1.27	V
VT-	Schmitt trigger,positive-going threshold	CMOS	0.57			V
I _{IH}	High lecvel input current					uA
	Input buffer	VIN=VDD	-10		10	
	Input buffer with pull-down		5	18	40	
I _{IL}	Low level input current					uA
	Input buffer	VIN=VSS	-10		10	
	Input buffer with pull-up		-40	-18	-5	
V _{OH}	High level input voltage					V
	TypeB8(Note#1)	I _{OH} = -8mA	1.2			
	TypeB12(Note#2)	I _{OH} = -12mA				
V _{OL}	Low level input voltage					V
	TypeB8	I _{OL} = 8mA			0.45	
	TypeB12	I _{OL} = 12mA				
I _{OZ}	Tri-state output leakage current	V _{OUT} =V _{SS} or V _{DD}	-10		10	uA
I _{DD}	Quiescent supply current				100	uA
C _{IN}	Input capacitance	Any input and Bi-directional buffers			4	pF
C _{OUT}	Output capacitance	Any output buffer			4	pF

NOTE#1:GPIOA[15:0],GPIOB[15:0],GPIOC[15:0],GPIOD[13:0],GPIOH[6:0],GPIOI[15],GPIOI[14],
GPIOK[7:0],GPIOL[12:0], GPIOM[8:0],GPION[7:0],GPIOO[5:0]

NOTE#2:

GPIOE[15:0],GPIOF[9:0],GPIOG[15:0],GPIOI[13:0],GPIOJ[15:0],GPIOL[14],GPIOL[13]

Absolute Maximum Ratings

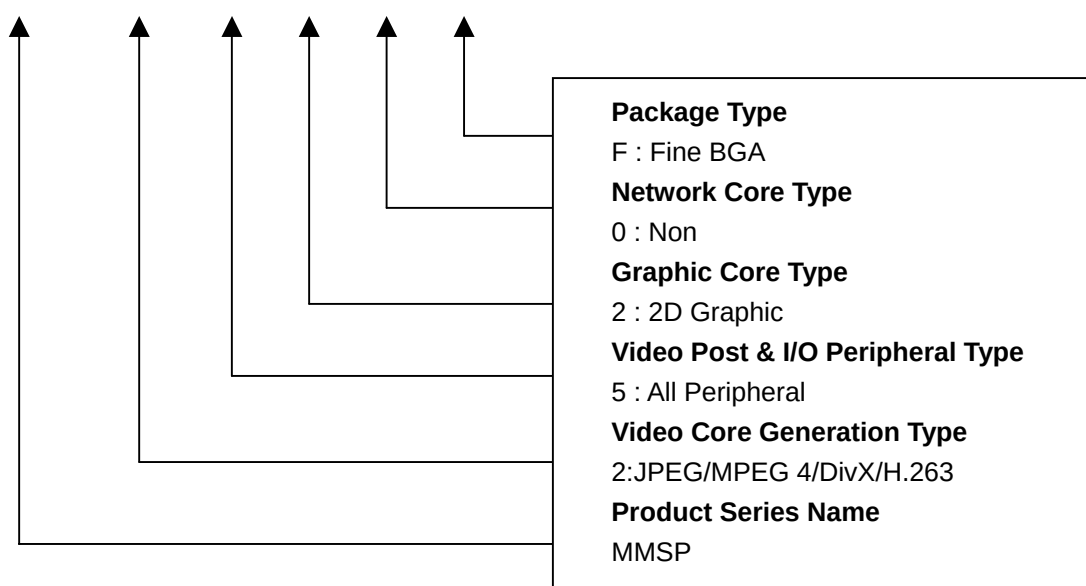
Symbol	Parameter	Rating			Unit
			Min	Max	
V _{DD}	DC supply voltage	1.8V V _{DD}	-0.5	2.7	
		3.3 V V _{DD}	-0.5	4.8	
V _{IN}	DC input voltage	1.8V input buffer	-0.5	2.7	
		3.3V input buffer	-0.5	4.8	
V _{OUT}	DC output voltage	1.8V output buffer	-0.5	2.7	
		3.3V output buffer	-0.5	4.8	
I _{IO}	Input/Output current	± 20			mA
T _A	Storage temperature	-65 to 150			°C

Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
			Min	Max	
V _{DD}	RTC power supply(=V _{DDRTC})	1.2V V _{DD}	1.2	1.8	V
	ARM920T Power supply (=V _{DDA920})	1.8V V _{DD}	1.65	1.95	
	ARM940T Power supply (=V _{DDA940})				
	Alive1 block power supply(=V _{VDDALIVE1})				
	Alive2 block power supply(=V _{VDDALIVE2})				
	APLL power supply(=V _{DDAPLL})				
	FPLL power supply(=V _{DDFPLL})				
	UPLL power supply(=V _{DDUPLL})				
	Internal logic power supply(=V _{DDI})				
	ADC power supply(=V _{DDADC})	3.3V V _{DD}	3.0	3.6	
	SDRAM I/O power supply(=V _{DDOPALIVE})				
V _{IN}	DC input voltage	3.3V input buffer	-0.3	V _{DDI0+0.3}	
V _{OUT}	DC output voltage	3.3V output buffer	-0.3	V _{DDI0+0.3}	
T _A	Commercial temperature range	0 to 70	⁰ C		⁰ C

MMSP™ 2 Ordering Information

MP 2 5 2 0 F



Processor Brand Name

MMSP™ 2

Series Model Number

MP2520F

Operation Temperature

0°C~70°C

MAGIC**EYES**

Product Number	MOQ	Package
MP2520F	840 EA 84* 10 Tray	400 pin FBGA (Fine Pitch Ball Grid Array) •Package Size : 18mm x 18mm x 1.22mm •Ball Pitch: 0.8mm •Ball Material Composition – Lead Free Sn: 96.5% Au: 0.5% Copper: 3%