MAGICEYES

MMSP™2

Data Book

MP2520F

Preliminary

Release Version 0.95

Document Release

2004/08/30

Copyright © 2001/2/3, MagicEyes Digitals Co.

All rights reserved. No part of this document may be reproduced in any form without written permission form MagicEyes Digital Co. MagicEyes Digital Co. reserved the rights to change in its products or product specification to improve functions or design at any time without notice.

MAGIC EYES

CONTENTS

UPDATA HISTORY

1. INTRODUCTION 1-5

1.1 GENERAL DESCRIPTION 1-5
1.2 KEY FEATURES 1-6
1.3 FUNCTIONAL SPECIFICATION 1-6
1.4 INTERNAL BUS ARCHITECTURE 1-7
1.5 MEMORY CONTROLLER 1-8
1.6 2D GRAPHIC PROCESSOR 1-8
1.7 IMAGE SIGNAL PROCESSOR 1-8
1.8 VIDEO PROCESSOR 1-8
1.9 VIDEO POST PROCESSOR 1-8
1.10 LCD CONTROLLER 1-9
1.11 USB HOST CONTROLLER 1-9
1.12 NAND FLASH CONTROLLER FOR H/W BOOTLOADER 1-9
1.13 IDE CONTROLLER 1-9
1.14 USB DEVICE 1-9
1.15 UART 1-9
1.16 I^2C 1-10
1.17 SPDIF CONTROLLER 1-10
1.18 AC97 CONTROLLER 1-10
1.19 I^2S CONTROLLER 1-10
1.20 SD/MMC CONTROLLER 1-10
1.21 DMA CONTROLLER 1-11
1.22 PWM CONTROLLER 1-11
1.23 CLOCK & POWER MANAGER 1-11
1.24 RTC CONTROLLER 1-11
1.25 TIMER / WATCH DOG TIMER 1-11
1.26 INTERRUPT CONTROLLER 1-12

1.27 TRANSPORT STREAM INTERFACE 1-12
1.28 ADC & TOUCH PANEL CONTROLLER 1-12
1.29 MEMORY STICK 1-12
1.30 CD-ROM DECODER 1-12
1.31 1-WIRE MASTER 1-12

2. I/O PIN DESCRIPTIONS 2-2

2.1 Mechanical Dimensions 2-2
2.2 MP2520F SIGNALS REFERENCE 2-3
2.3 MP2520F 2 I/O PIN LISTING 2-15
2.4 SYSTEM CONFIGURATION 2-29
2.5 TEST MODE PINS 2-30
2.6 PIN DESCRIPTION NOTES 2-30

3. MEMORY CONTROLLER 3-2

3.1 OVERVIEW 3-2
3.2 MEMORY MAP 3-3
3.2.1 MCU-C BANK (STATIC MEMORY CONTROLLER) 3-4
3.2.2 MCU-A BANK (SDRAM CONTROLLER) 3-10
3.3 INTERFACE 3-11
3.3.1 DRAM CONNECTION 3-11
3.3.2 IDE/PCMCIA INTERFACE 3-12
3.4 NAND BOOT OVERVIEW 3-13
3.5 BANK C MEMORY CONTROL REGISTER 3-15
3.6 BANK A MEMORY CONTROL REGISTER 3-27

4. DUAL CPU I/F 4-2

4.1 Overview 4-2

4.2 Operation 4-3

4.3 Dual-CPU Control Register LIST 4-3

5. CLOCKS AND POWER MANAGER 5-2

5.1 OVERVIEW 5-2

5.2 CLOCKS AND POWER MANAGER OPERATION 5-2

5.2.1 Clocks 5-3

5.2.2 Reference 5-4

5.2.3 MP2520F Clock Tree structure 5-5

5.2.4 Power Modes 5-24

5.2.5 Resets 5-29

5.3 Clocks And Power REGISTERs LIST 5-30

6. REAL TIME CLOCK(RTC) 6-2

6.1 OVERVIEW 6-2

6.2 RTC OPERATION 6-2

6.3 RTC REGISTER LIST 6-9

7. DMA CONTROLLER 7-2

7.1 OVERVIEW 7-2

7.2 PERIPHERAL INDEX TABLE 7-3

7.3 OPERATION 7-5

7.4 DMA REGISTERS LIST 7-6

8. INTERRUPT CONTROLLER 8-2

8.1 OVERVIEW 8-2

8.2 INTERRUPT CONTROLLER OPERATION 8-3

8.2.1 Interrupt Sources 8-4

8.2.2 Interrupt Priority Generation Block 8-5

8.2.3 Interrupt Priority 8-6

8.2.4 SOURCE PENDING REGISTER (SRCPEND) 8-6

8.2.5 INTERRUPT MODE REGISTER (INTMODE) 8-8

8.2.6 INTERRUPT MASK REGISTER (INTMASK) 8-10

8.2.7 INTERRUPT PRIORITY REGISTER(PRIORITY) 8-11

8.2.8 INTERRUPT PENDING REGISTER (INTPEND) 8-12

8.2.9 Interrupt Offset Register (INTOFFSET) 8-14

8.3 INTERRUPT CONTROLLER REGISTER LIST 8-14

9. TIMER/WATCH DOG TIMER 9-2

9.1 OVERVIEW 9-2

9.2 OPERATION 9-3

9.3 TIMER / WATCH DOG TIMER REGISTER LIST 9-6

10.UART 10-2

10.1 OVERVIEW 10-2

10.2 PIN DESCRIPTION 10-4

10.3 UART OPERATION 10-4

10.3.1 Data Transmission 10-4

10.3.2 Data Reception 10-5

10.3.3 Auto Flow Control(AFC) 10-5

10.3.4 Non Auto-Flow control (Controlling nRTS and nCTS by S/W) Example 10-6

10.3.5 SIR (Serial Infra-Red) Mode 10-6

10.3.6 Loop-back Mode 10-8

10.3.7 Modem Status Register Read 10-9

10.3.8 RS-232C interface 10-9

10.3.9 Interrupt/DMA Request Generation 10-9
10.3.10 UART ERROR STATUS FIFO 10-11
10.3.11 BAUD-RATE GENERATION 10-12
10.4 UART REGISTER LIST 10-13

11. GENERAL PURPOSE I/O (GPIO) 11-2
11.1 OVERVIEW 11-2
11.2 GPIP OPERATION 11-4
11.3 GPIO REGISTERS LIST 11-61

12. VIDEO PROCESSOR 12-2
12.1 OVERVIEW 12-2
12.2 VLD/VLC 12-3
12.3 PREDICTION 12-3
12.4 QUANTIZATION (Q/IQ) 12-4
12.5 DCT/IDCT 12-4
12.6 MOTION ESTIMATION 12-4
12.7 MOTION PREDICTION 12-4
12.8 DEBLOCKING/DERING 12-4

13. VIDEO POST PROCESSOR 13-2
13.1 OVERVIEW 13-2
13.2 FRAME DIMENSION CONVERTER 13-3
13.2.1 Overview 13-3
13.2.2 FDC Register LIST 13-4
13.3 SCALE PROCESSOR 13-6
13.3.1 Overview 13-6
13.3.2 Operation 13-7
13.3.3 SCALE PROCESS REGISTER LIST 13-15
13.4 MULTI LAYER CONTROLLOR 13-20
13.4.1 Overview 13-20
13.4.2 Operation 13-21

13.4.3 MLC REGISTER LIST 13-55

14. DISPLAY CONTROLLER 14-2

14.1 Overview 14-2

14.2 Operation 14-3

14.2.1 Display Clock Control 14-3

14.2.2 Horizontal Sync(HSYNC) Control 14-4

14.2.3 Vertical Sync(VSYNC) Control 14-7

14.2.4 Data Enable(DE) Control 14-8

14.2.5 Pixel Clock(CLKH) Control 14-10

14.2.6 Active Display Size 14-11

14.2.7 Video Data Bus(VD) Configuration 14-12

14.2.8 ESV/SAV 14-15

14.2.9 Composite Sync(CSYNC) 14-16

14.2.10 DAC Interface(YPbPr) 14-18

14.2.11 POL Control 14-20

14.2.12 CLKV Control 14-22

14.2.13 LP Control 14-23

14.2.14 FG, XDOFF, and PS Control 14-24

14.3 Display Controller Registers LIST 14-27

15.2D GRAPHIC ACCELERATOR..... 15-2
15.1 OVERVIEW 15-2
15.2 2D GRAPHIC CONTROLLER REGISTER 15-2

16.IMAGE SIGNAL PROCESSOR..... 16-2
16.1 OVERVIEW 16-2
16.2 OPERATION 16-4
16.2.1 Internal Signal Sync Generation 16-4
16.2.2 Image Signal Window 16-7
16.2.3 Gamma Control..... 16-13
16.2.4 RGB Recovery 16-14
16.2.5 Color Space Converter (RGB to YcbCr) 16-18
16.2.6 Luminance Enhancements 16-18
16.2.7 Chrominance Enhancement 16-21
16.2.8 lip & Color Suppress 16-24
16.2.9 Auto Exposure 16-27
16.2.10 Auto Focus..... 16-29
16.2.11 Auto White Balance 16-29
16.2.12 Possible Image Input Data Format and Related Port 16-35
16.3 IMAGE SIGNAL PROCESS REGISTER 16-36

17.PULSE WITH MODULATOR..... 17-2
17.1 OVERVIEW 17-2
17.2 PWM SIGNAL 17-3
17.3 PWM CONTROLLER REGISTERS LIST 17-4

18. PULSE PERIOD MEASUREMENT(PPM) 18-2

18.1 OVERVIEW 18-2

18.2 OPERATION 18-3

18.3 PPM CONTROLLER REGISTERS LIST 18-4

19. USB HOST / DEVICE 19-2

19.1 USB HOST 19-2

19.1.1 Overview 19-2

19.1.2 USB HOST CONTROL REGISTER 19-3

19.2 USB DEVICE 19-4

19.2.1 OVERVIEW 19-4

19.2.2 OPERATION 19-5

19.2.3 USB DEVICE REGISTERS LIST 19-25

20. I^2C 20-2

20.1 OVERVIEW 20-2

20.2 OPERATION 20-3

20.2.1 THE I^2C-BUS INTERFACE 20-3

20.2.2 READ-WRITE OPERATION 20-7

20.2.3 FLOWCHARTS OF THE OPERATIONS IN EACH MODE 20-8

20.3 I^2C -BUS INTERFACE REGISTER 20-13

21. SPDIF CONTROLLER 21-2

21.1 OVERVIEW 21-2

21.2 OPERATION 21-3

21.2.1 SPDIF Input 21-3

21.2.2 SPDIF Output 21-4

21.2.3 SPDIF Control Register (SPDIFCON) 21-4

21.2.4 SPDIF Interrupt Enable Register (SPDIFINTENB) 21-5

21.2.5 SPDIF Interrupt Status Register (SPDIFSTATUS) 21-5

21.2.6 SPDIF TX Clock Divider Register (SPDIFTXDIV) 21-6

21.3 SPDIF CONTROLLER REGISTERS LIST 21-6

22. AC97 22-2
22.1 OVERVIEW 22-2
22.2 PIN DESCRIPTION 22-3
22.2.1 External Interface Signal 22-3
22.3 OPERATION 22-3
22.3.1 AC-link Protocol 22-3
22.3.2 AC97 Controller Operation 22-6
22.3.3 Clocks and Sampling Frequencies 22-12
22.3.4 Buffers 22-13
22.3.5 Valid Data Structure 22-14
22.3.6 Operation Flow 22-15
22.4 AC97 REGISTER LIST 22-17

23. I^2S CONTROLLER 23-2
23.1 OVERVIEW 23-2
23.2 PIN DESCRIPTION 23-2
23.3 I^2S CONTROLLER OPERATION 23-2
23.3.1 Initialization 23-2
23.3.2 Clocks and Sampling Frequencies 23-5
23.3.3 Buffers 23-5
23.3.4 Valid Data Structure 23-6
23.3.5 Operation Flow 23-7
23.4 I^2S CONTROLLER REGISTER LIST 23-9

24. SSP/SPI 24-2
24.1 OVERVIEW 24-2
24.2 PIN DESCRIPTION 24-3
24.3 OPERATION 24-3
24.3.1 SPI Mode 24-4
24.3.2 SSP Mode 24-4
24.4 SSP/SPI CONTROLLER REGISTERS LIST 24-5

25. TRANSPORT STREAM INTERFACE(MPEG I/F) 25-2

25.1 OVERVIEW 25-2
25.2 PIN DESCRIPTION 25-4
25.3 OPERATION 25-4
25.4 TRANSPORT STREAM I/F REGISTERS LIST 25-5

26. ADC & TPC(TOUCH PANEL CONTROLLER) 26-2

26.1 OVERVIEW 26-2
26.2 OPERATION 26-3
26.2.1 CLOCK CONTROL 26-3
26.2.2 SAMPLING RATE CONTROL 26-5
26.2.3 MANUAL MODE 26-6
26.2.4 AUTO MODE 26-8
26.2.5 SWITCHING CONTROL 26-9
26.2.6 INTERRUPT 26-10
26.2.7 FIFO and Data FORMAT 26-11
26.3 ADC & TOUCH PANEL CONTROLLER REGISTER LIST 26-12

27. SD/MMC CONTROLLER 27-2

27.1 OVERVIEW 27-2
27.2 PIN DESCRIPTION 27-2
27.3 SD/MMC CONTROLLER OPERATION 27-2
27.3.1 Bus protocol 27-3
27.3.2 Initialization 27-4
27.3.3 Error Detection 27-4
27.3.4 Clocks 27-5
27.3.5 SDIO Operation 27-5
27.3.6 Operation Sequence Example 27-6
27.4 REGISTER MAP 27-17

28. MEMORY STICK CONTROLLER 28-2

28.1 OVERVIEW 28-2

28.2 SIGNAL DESCRIPTION 28-3
28.3 MEMORY STICK CONTROLLER OPERATION 28-3
28.3.1 PROTOCOL OVERVIEW 28-3
28.3.2 INITIALIZATION 28-4
28.3.3 DATA TRANSFER 28-4
28.3.4 INTERRUPT 28-4
28.4 MEMORY STICK CONTROLLER REGISTERS LIST 28-5

29. CD-ROM DECODER 29-2
29.1 OVERVIEW 29-2
29.1.1 CDRSYNCDESC Block 29-2
29.1.2 CDRECCEDC Block 29-4
29.2 OPERATION 29-4
29.2.1 CDROM Programming Guide 29-4
29.3 CDROM DECODER CONTROL REGISTER 29-6

30. 1-WIRE MASTER 30-2
30.1 OVERVIEW 30-2
30.2 PIN DESCRIPTION 30-2
30.3 OPERATION 30-2
30.3.1 Initialization 30-2
30.3.2 Clocks 30-2
30.3.3 Operation Flow 30-3
30.3.4 Timing Diagram 30-5
30.3.5 Read/write a Byte Data 30-8
30.3.6 1-Wire Status 30-9
30.4 REGISTER MAP LIST 30-14

31. DECSS 31-2
31.1 OVERVIEW 31-2
31.2 OPERATION 31-3
31.3 DECSS CONTROL REGISTERS LIST 31-4

MAGIC EYES

FIGURE OF CONTENTS

Figure 1-1. Top Level Block Diagram 1-5
Figure 2-1. MP2520F Package 2-2
Figure 2-2. MP2520F Package FBGA Ball Map 2-3
Figure 3-1. Memory Controller Block Diagram 3-2
Figure 3-2. SDRAM Bank/Static Memory Bank Exchange 3-3
Figure 3-3. DRAM Connection 3-11
Figure 3-4. IDE/PCMCIA Interface 3-12
Figure 3-5. NAND Boot Procedure 3-13
Figure 4-1. Dual CPU Block Diagram 4-2
Figure 5-1. Clocks and Power Manager Block Diagram 5-2
Figure 5-2. FPLLCLKGEN Block 5-5
Figure 5-3. UPLLCLKGEN Block 5-5
Figure 5-4. APLLCLKGEN Block 5-5
Figure 5-5. System Clock Gen 5-6
Figure 5-6. System Bus and I/O Bus Clock Generationeration 5-6
Figure 5-7. Peripheral Clock Generation 5-6
Figure 7-1. DMA Controller Block Diagram 7-2
Figure 8-1. Interrupt Process Diagram 8-2
Figure 8-2. Priority Generating Block 8-5
Figure 9-1. Timer Block Diagram 9-2
Figure 10-1. UART Block Diagram (with FIFO) 10-3
Figure 10-2. UART AFC interface 10-6
Figure 10-3. SIR Function Block Diagram 10-7
Figure 10-4. Serial I/O Frame Timing Diagram (Normal UART) 10-7
Figure 10-5. Infra-Red Transmit Mode Frame Timing Diagram 10-8
Figure 10-6. Infra-Red Receive Mode Frame Timing Diagram 10-8
Figure 10-7. nCTS and Delta CTS Timing Diagram 10-9
Figure 10-8. A Case showing UART Receiving 5 Characters with 2 Errors 10-12
Figure 11-1. GPIO Block Diagram 11-3

Figure 12-1. VIDEO PROCESSOR 12-3
Figure 13-1. Video Post Processor Diagram.....13-2
Figure 13-2. Frame Dimension Converter Block Diagram 13-3
Figure 13-4. Characteristics of Digital Filter 13-9
Figure 13-5. Multi Layer Controller Block Diagram 13-21
Figure 13-6. 4-Division of YUV Layer.....13-22
Figure 13-7. 8 bit Compressed Data Flow Chart.....13-33
Figure 13-8. OSD FileStructure.....13-34
Figure 13-9. RGB Display Mode 13-40
Figure 13-10. 8x8 Cursor Pattern 13-46
Figure 13-11. The basic Concept of Hue Control 13-51
Figure 14-1. Display Controller. 14-2
Figure 14-2. Display Controller Clock Control.....14-3
Figure 14-3. HSYNC Timing Diagram.....14-4
Figure 14-4. Vertical Sync Timing Diagram.....14-8
Figure 14-6. DE Timing Diagram in the STH Mode.....14-9
Figure 14-7. DE Timing Diagram in the PULSE Mode 14-9
Figure 14-8. CLKH and Pixel Data.....14-10
Figure 14-9. Relation Between EAV/SAV and Waveform.....14-15
Figure 14-10. Data Stream format for 625 Line Systems. 14-16
Figure. 14-11. Waveform for EQUALIZING and SERRATION PULSE.....14-16
Figure 14-12. Waveform in 525 Line System.....14-17
Figure 14-13. Pin Configuration for HSYNC and DE 14-17
Figure 14-14. Sync Waveform for HDTV and SDTV 14-18
Figure 14-15. POL Waveform 14-21
Figure 14-16. CLKV Waveform.....14-22
Figure 14-17. Waveform for LP and STH.....14-23
Figure 14-18. Waveform for PS, XDOFF and FG 14-24
Figure 14-19. HSYNC/VSYNC Interrupt 14-25
Figure 16-1. Image Signal Processor Block Diagram 16-3
Figure 16-2. Image Signal Horizontal/Vertical Sync.....16-7

Figure 16-3. Image Signal Vertical Processing Window 16-11
Figure 16-4. Image Signal Horizontal processing window 16-12
Figure 16-5. Bayer Color Arrangements 16-18
Figure 16-6. Frequency Response of Luminance Enhancement 16-21
Figure 16-7. Frequency Response of Chrominance Decimation Filter 16-22
Figure 16-8. The Basic Concept of Hue Control 16-23
Figure 16-9. Luminance Clip & Color Suppress by Level 16-26
Figure 16-10. Auto Exposure Coordinates 16-28
Figure 16-11. Auto White Balance Coordinates 16-34
Figure 17-1. PWM Block Diagram 17-3
Figure 18-1. PPM Block Diagram 18-2
Figure 19-1. USB Host Controller Block Diagram 19-2
Figure 19-2. USB Device Block Diagram 19-5
Figure 20-1. I^2C Block Diagram 20-3
Figure 20-2. Start and Stop Condition 20-4
Figure 20-3. I^2C -Bus Interface Data Format 20-5
Figure 20-4. Data Transfer on the I^2C -Bus 20-6
Figure 20-5. Acknowledge on the I^2C -Bus 20-7
Figure 20-6. Operations for Master/Transmitter Mode 20-9
Figure 20-7. Operations for Master/Receiver Mode 20-10
Figure 20-8. Operations for Slave/Transmitter Mode 20-11
Figure 20-9. Operations for Slave / Receiver Mode 20-12
Figure 21-1. SPDIF Block Diagram 21-3
Figure 22-1. AC97 Standard Bidirectional Audio Frame 22-3
Figure 22-2. AC-link Audio Output Frame 22-5
Figure 22-3. AC97 Input Frame 22-6
Figure 22-4. AC '97 Command Read/Write Flow Chart 22-8
Figure 22-5. Internal Data Path 22-13
Figure 22-6. AC '97 Operation Flow Chart 22-16
Figure 23-1. I^2S Buffer Block Diagram 23-6
Figure 24-1. SSP/SPI Block Diagram 24-2

Figure 24-2. SPI Mode Signal 24-4
Figure 25-1. Transport Stream I/F Block Diagram 25-2
Figure 25-2. In Serial Mode 25-3
Figure 25-3. In Parallel Mode 25-3
Figure 26-1. TPC System Block Diagram 26-2
Figure 26-2. Pen Input Sampling Time 26-3
Figure 26-3. Switching Control 26-10
Figure 27-1. Operation Without Data 27-3
Figure 27-2. Operation With Data 27-4
Figure 28-1. Memory Stick Controller Block Diagram 27-2
Figure 28-2. Timing Diagram 27-3
Figure 29-1. CDRSYNCDESC Block Diagram 29-2
Figure 29-2. Supported CD Formats 29-3
Figure 29-3. Internal Block Diagram 29-4
Figure 30-1. Reset and Presence Detection Timing 30-5
Figure 30-2. Write Time Slot 30-6
Figure 30-3. Read Time Slot 30-7
Figure 31-1. DECSS Block Diagram 31-2

TABLE OF CONTENTS

TABLE 2-1. Signal Descriptions for MP2520F 2-10
TABLE 2-2. MP2520F GPIO pin map 2-14
TABLE 2-3. MP2520F Pin Out – Ballpad Number Order 2-28
TABLE 2-4. System Configuration 2-29
TABLE 2-5. Test Mode Pins 2-30
TABLE 3-1. 512Byte ECC Parity Code Assignment Table 3-14
TABLE 3-2. Bank C Configuration Register (MEMCFGW) 3-15
TABLE 3-3. Bank C Timing Register #0 (MEMTIMEW0) 3-16
TABLE 3-4. Bank C Timing Register #1 (MEMTIMEW1) 3-16
TABLE 3-5. Bank C Timing Register #2 (MEMTIMEW2) 3-16
TABLE 3-6. Bank C Timing Register #3 (MEMTIMEW3) 3-17
TABLE 3-7. Bank C Timing Register #4 (MEMTIMEW4) 3-17
TABLE 3-8. Bank C Wait Control Register (MEMWAITCTRLW) 3-17
TABLE 3-9. Bank C Page Control Register (MEMPAGEW) 3-18
TABLE 3-10. Bank C IDE Timing Control Register (MEMIDETIMEW) 3-18
TABLE 3-11. Bank C PCMCIA Memory Timing Control Register (MEMPCMCIAMW) 3-18
TABLE 3-12. Bank C PCMCIA Attribute Timing Control Register (MEMPCMCIAAW) 3-19
TABLE 3-13. Bank C PCMCIA I/O Timing Register (MEMPCMCIAIW) 3-19
TABLE 3-14. Bank C PCMCIA Wait Timing Register #0 (MEMPCMCIAWAITW) 3-19
TABLE 3-15. Bank C IDE Wait Timing Register #1 (MEMIDEWAITW) 3-19
TABLE 3-16. Bank C DMA Timeout Register (MEMDTIMEOUTW) 3-20
TABLE 3-17. Bank C DMA Control Register (MEMDMACTRLW) 3-20
TABLE 3-18. Bank C DMA Polarity Register (MEMDMAPOLW) 3-21
TABLE 3-19. Bank C DMA Timing Register #0 (MEMDMATIMEW0) 3-21
TABLE 3-20. Bank C DMA Timing Register #1 (MEMDMATIMEW1) 3-21
TABLE 3-21. Bank C DMA Timing Register #1 (MEMDMATIMEW1) 3-22
TABLE 3-22. Bank C DMA Timing Register #3 (MEMDMATIMEW3) 3-22
TABLE 3-23. Bank C DMA Timing Register #4 (MEMDMATIMEW4) 3-22

TABLE 3-24. Bank C DMA Timing Register #5 (MEMDMATIMEW5)..... 3-22
TABLE 3-25. Bank C DMA Timing Register #6 (MEMDMATIMEW6)..... 3-23
TABLE 3-26. Bank C DMA Timing Register #8 (MEMDMATIMEW8)..... 3-23
TABLE 3-27. Bank C DMA Strobe Control Register (MEMDMASTRBW) 3-23
TABLE 3-28. Bank C NAND FLASH CTRL Register (MEMNANDCTRLW) 3-24
TABLE 3-29. Bank C NAND FLASH Timing Register (MEMNANDTIMEW)..... 3-24
TABLE 3-30. Bank C NAND FLASH ECC0 Register (MEMNANDECC0W) 3-25
TABLE 3-31. Bank C NAND FLASH ECC1 Register (MEMNANDECC1W) 3-25
TABLE 3-32. Bank C NAND FLASH ECC2 Register (MEMNANDECC2W) 3-25
TABLE 3-33. Bank C NAND FLASH Data Counter Register (MEMNANDCNTW) 3-25
TABLE 3-34. Bank C Chip Selection Control Register (MEMCHIPSELTW) .....
TABLE 3-35. NAND Flash Data Register (NFDATA) 3-26
TABLE 3-36. NAND Flash Command Register (NFCMD)..... 3-26
TABLE 3-37. NAND Flash Address Register (NFADDR) 3-26
TABLE 3-38. Bank A SDRAM Configuration Register (MEMCFGX) 3-27
TABLE 3-39. Bank A TIMMING Register #0 (MEMTIMEX0) 3-27
TABLE 3-40. Bank A TIMMING Register #1 (MEMTIMEX1) 3-28
TABLE 3-41. Bank A Active Power Down Control Register (MEMACTPWDX)..... 3-28
TABLE 3-42. Bank A Refresh Control Register (MEMREFX) 3-28
TABLE 4-1. Dual CPU Control Registers List..... 4-4
TABLE 5-1. Clock Source Table..... 5-3
TABLE 5-2. Power Mode Register (PWMODEREG) 5-7
TABLE 5-3. System Clock PLL Divide Value Set Register (SYSCSETREG) 5-9
TABLE 5-4. External System Clock Time Set Register (ESYSCSETREG) 5-9
TABLE 5-5. USB/MMC Clock Generation U-PLL Divide Value Set Register (UIRMCSETREG)..... 5-10
TABLE 5-6. SPDIF Controller Clock Generation PLL Divide Value Set Register (SPDICSETREG)..... 5-11
TABLE 5-7. Audio Controller Clock Generation PLL Divide Value Set (AUDICSETREG)..... 5-11
TABLE 5-8. Display Clock Generation PLL Divide Value Set Register (DISPCSETREG) 5-12
TABLE 5-9. Image Pixel Clock Generation PLL Divide Value Set Register (IMAGCSETREG)..... 5-12
TABLE 5-10. UART0/1 TX/RX Clock Generation PLL Divide Value Set Register (URT0CSETREG)..... 5-13
TABLE 5-11. UART TX/RX Clock Generation PLL Divide Value Set Register (URT1CSETREG)4 5-13

TABLE 5-12. ARM940T CPU Power Manage Mode Register (A940TMODEREG) 5-14
TABLE 5-13. System Clock Enable Register (SYSCLKENGEG) 5-15
TABLE 5-14. Communication Device Clock Enable Register (COMCLKENREG) 5-17
TABLE 5-15. Video & Graphic Device Clock Enable Register (VGCLKENREG) 5-18
TABLE 5-16. Audio & Storage Device Clock Enable Register (ASCLKENREG) 5-20
TABLE 5-17. CLOCK LIST table. 5-23
TABLE 5-18. Various Clock Source List 5-24
TABLE 5-19. System Operation Mode 5-25
TABLE 5-20. Power Mode Sequence Table 5-28
TABLE 5-21. Clock And Power Registers List 5-35
TABLE 6-1. RTC Counter Set Register 6-2
TABLE 6-2. RTC Time Count Register 6-3
TABLE 6-3. RTC Sub-Second Time Count Register 6-3
TABLE 6-4. RTC Time Tick Set Register 6-3
TABLE 6-5. ALARM Time Set Register 6-4
TABLE 6-6. Power Manage Register 6-4
TABLE 6-7. Clock Manage Register 6-4
TABLE 6-8. Reset Enable Control Register 6-5
TABLE 6-10. Boot Operation control Register 6-6
TABLE 6-11. Clock Locking Time Set Register 6-6
TABLE 6-12. Reset Width Time Set Register 6-6
TABLE 6-13. Ext. Input 0/1 Pin State Control Register 6-7
TABLE 6-14. Stop Watch Timer register 6-7
TABLE 6-15. RTC control register 6-8
TABLE 6-16. RTC interrupt status register 6-8
TABLE 6-17. RTC Registers List 6-13
TABLE 7-1. Peripheral Index Table 7-4
TABLE 7-2. Channel Base Address 7-5
TABLE 7-3. Channel Priority 7-6
TABLE 7-4. DMA Controller Registers List 15
TABLE 8-1. Interrupt Source Table 8-5

TABLE 8-2. Source Pending Register 8-7
TABLE 8-3. Interrupt Mode Register 8-9
TABLE 8-4. Interrupt Mask Register 8-11
TABLE 8-5. Interrupt Priority Register 8-12
TABLE 8-6. Interrupt Pending Register 8-13
TABLE 8-7. Interrupt Offset Register 8-14
TABLE 8-8. Interrupt Controller Registers List 8-19
TABLE 9-1. Timer Counter Register 9-3
TABLE 9-2. Timer Match 0 Register 9-3
TABLE 9-3. Timer Match 1 Register 9-3
TABLE 9-4. Timer Match 2 Register 9-4
TABLE 9-5. Timer match 3 / watch dog timer register 9-4
TABLE 9-6. Watchdog Timer Enable Register 9-4
TABLE 9-7. Timer status register 9-5
TABLE 9-8. Timer Interrupt Enable Register 9-5
TABLE 9-9. Timer / Watch Dog Timer Registers List 9-7
TABLE 10-1. Pin Description Table 10-4
TABLE 10-2. Interrupts in Connection with FIFO 10-10
TABLE 10-3. Error Interrupts Table 10-11
TABLE 10-4. Uart Interrupt Registers List 10-19
TABLE 11-1. GPIO Pin Group 11-2
TABLE 11-2. GPIOx Alternate Function Low Register 11-4
TABLE 11-3. GPIOx Alternate Function High Register 11-4
TABLE 11-4. GPIOx Output Level Register 11-27
TABLE 11-5. GPIOx Event Type Low Register .....
TABLE 11-6. GPIOx Event Type High Register .....
TABLE 11-7. GPIOx Pull Up Enable Register 11-51
TABLE 11-8. GPIOx Interrupt Enable Register 11-53
TABLE 11-9. GPIOx Event Register 11-54
TABLE 11-10. GPIO PAD Selection Register 11-55
TABLE 11-11. GPIO Group Event Register 11-56

TABLE 11-12. GPIOx Pin Level Register 11-57
TABLE 11-13. GPIOE Output Alive Register (GPIOEOUT_ALIVE) 11-57
TABLE 11-14. GPIOE Output Enable Alive Register (GPIOEOUTENB_ALIVE) 11-57
TABLE 11-15. GPIOE Pull Up Enable Alive Register (GPIOEPUENB_ALIVE) 11-57
TABLE 11-16. GPIOF Output Alive Register (GPIOFOUT_ALIVE) 11-58
TABLE 11-17. GPIOF Output Enable Alive Register (GPIOFOUTENB_ALIVE) 11-58
TABLE 11-18. GPIOF Pull Up Enable Alive Register (GPIOFPUENB_ALIVE) 11-58
TABLE 11-19. GPIOG Output Alive Register (GPIOGOUT_ALIVE) 11-58
TABLE 11-20. GPIOG Output Enable Alive Register (GPIOGOUTENB_ALIVE) 11-59
TABLE 11-21. GPIOG Pull Up Enable Register (GPIOGPUENB_ALIVE) 11-59
TABLE 11-22. GPIOI Output Alive Register (GPIOIOUT_ALIVE) 11-59
TABLE 11-23. GPIOI Output Enable Alive Register (GPIOIOUTENB_ALIVE) 11-59
TABLE 11-24. GPIOI Pull Up Enable Alive Register (GPIOIPUENB_ALIVE) 11-60
TABLE 11-25. GPIOJ Output Alive Register (GPIOJOUT_ALIVE) 11-60
TABLE 11-26. GPIOJ Output Enable Alive Register (GPIOJOUTENB_ALIVE) 11-60
TABLE 11-27. GPIOJ Pull Up Enable Alive Register (GPIOJPUENB_ALIVE) 11-60
TABLE 11-28. GPIO REGISTERS LIST 11-99
TABLE 13-1. FRAME DIMENSION CONVERTER 13-6
TABLE 13-2. Pre-Scale Ratio (SC_PRE_VRATIO) 13-7
TABLE 13-3. Pre-Scale Ratio (SC_PRE_HRATIO) 13-7
TABLE 13-4. Pre-Scale Ratio 13-7
TABLE 13-5. Pre-Scale Ratio 13-8
TABLE 13-6. Post-Scale VRATIO 13-8
TABLE 13-7. Post-Scale HRATIO 13-8
TABLE 13-8. Y/Cb/Cr Separation Function 13-10
TABLE 13-9. Y/Cb/Cr Separation Function 13-10
TABLE 13-10. Status Register(SC_MIRROR) 13-11
TABLE 13-11. Source / Destination Address Starting Point 13-12
TABLE 13-12. Source / Destination Address Starting Point 13-12
TABLE 13-13. Source / Destination Address Starting Point 13-12
TABLE 13-14. Source / Destination Address Starting Point 13-12

TABLE 13-15. Source / Destination Address Starting Point 13-12
TABLE 13-16. Source / Destination Address Starting Point 13-13
TABLE 13-17. Status Register (SC_STATUS) 13-13
TABLE 13-18. Scale Processor Paths by Function 13-14
TABLE 13-19. Scale Processor Registers List 13-19
TABLE 13-20. YUV Layer list 13-23
TABLE 13-21. Effect of Video Image (MLC_YUV_EFECT) 13-24
TABLE 13-22. Video Image Control Register (MLC_YUV_CNTL) 13-25
TABLE 13-23. Scale Factor Register of Region A (MLC_YUVA_TP_HSC) 13-25
TABLE 13-24. Scale Factor Register of Region A (MLC_YUVA_BT_HSC) 13-25
TABLE 13-25. Scale Factor Register of Region A (MLC_YUVA_TP_HSCL, MLC_YUVA_TP_HSCH) 13-25
TABLE 13-26. Scale Factor Register of Region A (MLC_YUVA_BT_HSCL, MLC_YUVA_BT_HSCH) 13-26
TABLE 13-27. Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW) 13-26
TABLE 13-28. Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW) 13-26
TABLE 13-29. Coordinate Register of Region A (MLC_YUVA_STX) 13-26
TABLE 13-30. Coordinate Register of Region A (MLC_YUVA_ENDX)1 13-26
TABLE 13-31. Coordinate Register of Region A (MLC_YUVA_TP_STY) 13-27
TABLE 13-32. Coordinate Register of Region A (MLC_YUVA_TP_ENDY) 13-27
TABLE 13-33. Coordinate Register of Region A (MLC_YUVA_BT_ENDY) 13-27
TABLE 13-34. Source Address of Region A (MLC_YUVA_TP_OADRL, MLC_YUVA_TP_OADRH) 13-27
TABLE 13-35. Source Address of Region A (MLC_YUVA_TP_EADRL, MLC_YUVA_TP_EADRH) 13-27
TABLE 13-36. Source Address of Region A (MLC_YUVA_BT_OADRL, MLC_YUVA_BT_OADRH) 13-28
TABLE 13-37. Source Address of Region A (MLC_YUVA_BT_EADRL, MLC_YUVA_BT_EADRH) 13-28
TABLE 13-38. Scale Factor Register of Region B (MLC_YUVB_TP_HSC) 13-28
TABLE 13-39. Scale Factor Register of Region B (MLC_YUVB_BT_HSC) 13-28
TABLE 13-40. Scale Factor Register of Region B (MLC_YUVB_TP_VSCL, MLC_YUVB_TP_VSCH) 13-29
TABLE 13-41. Scale Factor Register of Region B (MLC_YUVB_BT_VSCL, MLC_YUVB_BT_VSCH) 13-29
TABLE 13-42. Horizontal Pixel Width Register of Region B(MLC_YUVB_TP_PXW) 13-29
TABLE 13-43. Horizontal Pixel Width Register of Region B(MLC_YUVB_BT_PXW) 13-29
TABLE 13-44. Coordinate Register of Region B (MLC_YUVB_STX) 13-30
TABLE 13-45. Coordinate Register of Region B (MLC_YUVB_ENDX) 13-30

TABLE 13-46. Coordinate Register of Region B (MLC_YUVB_TP_STY) 13-30
TABLE 13-47. Coordinate Register of Region B (MLC_YUVB_TP_ENDY) 13-30
TABLE 13-48. Coordinate Register of Region B (MLC_YUVB_BT_ENDY) 13-30
TABLE 13-49. Source Address of Region B(MLC_YUVB_TP_OADR) 13-31
TABLE 13-50. Source Address of Region B(MLC_YUVB_TP_EADR) 13-31
TABLE 13-51. Source Address of Region B(MLC_YUVB_BT_OADR) 13-31
TABLE 13-52. Source Address of Region B(MLC_YUVB_BT_EADR) 13-31
TABLE 13-53. OSD Top Header 13-34
TABLE 13-54. OSD Region Header 13-35
TABLE 13-55. OSD Palette 13-35
TABLE 13-56. OSD Register 13-36
TABLE 13-57. Source Address of OSD(MLC_OSD_OADRL, MLC_OSD_OADRH) 13-36
TABLE 13-58. Source Address of OSD(MLC_OSD_EADRL, MLC_OSD_EADRH) 13-36
TABLE 13-59. Base Information Format 13-37
TABLE 13-60. Change Command Information Format 13-38
TABLE 13-61. Highlight Information Format 13-39
TABLE 13-62. RGB Layer 13-39
TABLE 13-63. RGB Plane Registers List1 3-41
TABLE 13-64. Still Image Control Register (MLC_STL_CNTL) 13-42
TABLE 13-65. Mix/ Mux Control Register (MLC_STL_MIXMUX) 13-42
TABLE 13-66. Alpha Blending Value Register (MLC_RGB_ALPHAL) 13-42
TABLE 13-67. Alpha Blending Value register (MLC_STL_ALPHAL) 13-42
TABLE 13-68. Alpha Blending Value Register (MLC_STL_ALPHAH) 13-43
TABLE 13-69. Coordinate Register of Still Image (RGB) Layer
(MLC_STL1_STX, MLC_STL2_STX, MLC_STL3_STX, MLC_STL4_STX) 13-43
TABLE 13-70. Coordinate Register of Still Image (RGB) Layer
(MLC_ STL1_ENDX, MLC_ STL2_ENDX, MLC_ STL3_ENDX, MLC_ STL4_ENDX) 13-43
TABLE 13-71. Coordinate Register of Still Image (RGB) Layer
(MLC_ STL1_STY, MLC_ STL2_STY, MLC_ STL3_STY, MLC_ STL4_STY) 13-43
TABLE 13-72. Coordinate Register of Still Image (RGB) Layer
(MLC_ STL1_ENDY, MLC_ STL2_ENDY, MLC_ STL3_ENDY, MLC_ STL4_ENDY) 13-44

TABLE 13-73. Color Key register of Still Image (RGB) Layer (MLC_STL_CKEY_GR) 13-44
TABLE 13-74. Color Key Register of Still Image (RGB) Layer (MLC_STL_CKEY_R) 13-44
TABLE 13-75. Scale Factor Register of Still Image (RGB) Layer (MLC_STL_HSC) 13-44
TABLE 13-76. Scale Factor Register of Still Image(RGB) Layer (MLC_STL_VSCL, MLC_STL_VSCH) 13-45
TABLE 13-77. Horizontal Width Register of Still Image(RGB) Layer (MLC_STL_HW) 13-45
TABLE 13-78. Source Address of Still Image (RGB) Layer (MLC_STL_OADRL, MLC_STL_OADRH) 13-45
TABLE 13-79. Source Address of Still Image (RGB) Layer (MLC_STL_EADRL, MLC_STL_EADRH) 13-45
TABLE 13-80. Cursor Pattern Data 13-46
TABLE 13-81. Hardware Cursor Registers 13-47
TABLE 13-82. Hardware Cursor Control Register (MLC_HWC_CNTR) 13-47
TABLE 13-83. Hardware Cursor Control Register (MLC_HWC_STX, MLC_HWC_STY) 13-48
TABLE 13-84. Hardware Cursor Control Register (MLC_HWC_FGR) 13-48
TABLE 13-85. Hardware Cursor Control Register (MLC_HWC_FB) 13-48
TABLE 13-86. Hardware Cursor Control Register (MLC_HWC_BGR) 13-48
TABLE 13-87. Hardware Cursor Control Register (MLC_HWC_BB) 13-49
TABLE 13-88. Source Address of Hardware Cursor (MLC_HWC_OADRL, MLC_HWC_OADRH) 13-49
TABLE 13-89. Source Address of Hardware Cursor (MLC_HWC_EADRL, MLC_HWC_EADRH) 13-49
TABLE 13-90. Luminance Enhancement Control Register (MLC_LUMA_ENH) 13-49
TABLE 13-91. Hue Control 13-51
TABLE 13-92. Chrominance Enhancement Control Register
(MLC_HUECB1AB, MLC_HUECB2AB, MLC_HUECB3AB, MLC_HUECB4AB) 13-52
TABLE 13-93. Chrominance Enhancement Control Register
(MLC_HUECR1AB, MLC_HUECR2AB, MLC_HUECR3AB, MLC_HUECR4AB) 13-52
TABLE 13-94. Dither Control Register (MLC_DITHER) 13-53
TABLE 13-95. Gamma Correction Registers 13-53
TABLE 13-96. Display Table Control (MLC_GAMMA_A, DISP_ GAMMA_D) 13-54
TABLE 13-97. Scale Information 13-54
TABLE 13-98. Interlaced/Progressive Display Registers List 13-55
TABLE 13-99. MLC REGISTER LIST 13-65
TABLE 14-1. Clock Control Register (DPC_CLKCNTL) 14-4
TABLE 14-2. HSYNC WIDTH Register (DPC_HS_WIDTH) 14-5

TABLE 14-3. HSYNC Start Register(DPC_HS_STR)..... 14-5
TABLE 14-4. HSYNC End Register(DPC_HS_END)..... 14-5
TABLE 14-5. DE Control Register(DPC_DE)..... 14-6
TABLE 14-6. Vertical Sync Control Register(DPC_V_SYNC)..... 14-7
TABLE 14-7. Vertical Sync End Register(DPC_VS_END)..... 14-7
TABLE 14-8. PAD Control Register(DPC_FPICNTL)..... 14-10
TABLE 14-9. PAD Polarity Control Register(DPC_FPIPOL1)..... 14-11
TABLE 14-10. Active Horizontal Width (DPC_X_MAX)..... 14-11
TABLE 14-11. Active Vertical Height (DPC_Y_MAX)..... 14-12
TABLE 14-12. Bus Setting in Accordance with the Types of Data..... 14-12
TABLE 14-13. DPC Control Register(DPC_CNTL)..... 14-13
TABLE 14-14. VD Configuration in RGB Mode..... 14-14
TABLE 14-15. VD Configuration in MGRB Mode..... 14-14
TABLE 14-16. VD Configuration in YCbCr Mode..... 14-14
TABLE 14-17. EAV/SAV Code According to F,V,H..... 14-15
TABLE 14-18. CSYNC Control Register(DPC_MID_SYNC)..... 14-16
TABLE 14-19. BLANK Level for Luminance(DPC_Y_BLANK)..... 14-18
TABLE 14-20. BLANK Level for Chrominamce (DPC_C_BLANK)..... 14-19
TABLE 14-21. Positive Sync Level for Luminance(DPC_YP_CSYNC)..... 14-19
TABLE 14-22. Negative Sync Level for Luminance(DPC_YN_CSYNC)..... 14-19
TABLE 14-23. Positive Sync Level for Chrominance(DPC_CP_CSYNC)..... 14-19
TABLE 14-24. Negative Sync Level for Chrominance(DPC_CN_CSYNC)..... 14-19
TABLE 14-25. POL Control Register(DPC_POL)..... 14-20
TABLE 14-26. CLKV Control Register(DPC_CLKVL)..... 14-21
TABLE 14-27. CLKV Control Register(DPC_CLKVH)..... 14-22
TABLE 14-28. LP Control Register(DPC_LP)..... 14-23
TABLE 14-29. PS Control Register(DPC_PS)..... 14-24
TABLE 14-30. FG Control Register(DPC_FG)..... 14-25
TABLE 14-31. Interrupt Control Register(DPC_INTR)..... 14-26
TABLE 14-32. Display Cotroller Registers List..... 14-34
TABLE 15-1. Display Cotroller Registers List..... 15-5

TABLE 15-2. Destination Address Register (MESGDSTADDR) 15-5
TABLE 15-3. Destination Stride Register (MESGDSTSTRIDE) 15-5
TABLE 15-4. Source Control Register (MESGSRCCTRL) 15-6
TABLE 15-5. Source Address Register (MESGSRCADDR) 15-6
TABLE 15-6. Source Stride Register (MESGSRCSTRIDE) 15-6
TABLE 15-7. Source Foreground Color Register (MESGSRCFORCOLOR) 15-6
TABLE 15-8. Source Background Color Register (MESGSRCBACKCOLOR) 15-7
TABLE 15-9. Pattern Control Register (MESGPATCTRL) 15-7
TABLE 15-10. Pattern Foreground Color Register (MESGFORCOLOR) 15-7
TABLE 15-11. Pattern Background Color Register (MESGBACKCOLOR) 15-8
TABLE 15-12. Size Register (MESGSIZE) 15-8
TABLE 15-13. Control Register (MESGCTRL) 15-8
TABLE 15-14. Status Register (MESGSTATUS) 15-9
TABLE 15-15. FIFO Status Register (MESGFIFOSTATUS) 15-9
TABLE 15-16. Source FIFO Register (MESGFIFO) 15-9
TABLE 15-17. Pattern Register (MESGPAT) 15-9
TABLE 16-1. ISP Sync Control Register(ISP_ VPERIOD) 16-5
TABLE 16-2. ISP Sync Control Register(ISP_VPW) 16-5
TABLE 16-3. Sync Control Register(ISP_ HPERIOD) 16-5
TABLE 16-4. Sync Control Register(ISP_ HPW) 16-5
TABLE 16-5. Sync Control Register(ISP_HACT_STW) 16-6
TABLE 16-6. Sync Control Register(ISP_H_WIDTH) 16-6
TABLE 16-7. Sync Control Register(ISP_VACT_ST) 16-6
TABLE 16-8. Sync Control Register(ISP_V_HEIGHT) 16-6
TABLE 16-9. Processing Window Control Register(ISP_RGBSV) 16-8
TABLE 16-10. Processing Window Control Register(ISP_RGBEV) 16-8
TABLE 16-11. Processing Window Control Register(ISP_RGBSH) 16-8
TABLE 16-12. Processing Window Control Register(ISP_RGBEH) 16-8
TABLE 16-13. Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESV) 16-9
TABLE 16-14. Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEV) 16-9
TABLE 16-15. Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESH) 16-9

TABLE 16-16. Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEH)..... 16-9
TABLE 16-17. Auto Focus Accumulation Window Control Register(ISP_ AFSV)..... 16-10
TABLE 16-18. Auto Focus Accumulation Window Control Register(ISP_ AFEV)..... 16-10
TABLE 16-19. Auto Focus Accumulation Window Control Register(ISP_ AFSH) 16-10
TABLE 16-20. Auto Focus Accumulation Window Control Register(ISP_ AFEH) 16-10
TABLE 16-21. Gamma Table Control(ISP_GAMMA) 16-13
TABLE 16-22. Gamma Table Control(ISP_GAMMD) 16-13
TABLE 16-23. RGB Recovery..... 16-14
TABLE 16-24. Image Signal Processor Control Register(ISP_CON_1) 16-16
TABLE 16-25. External Memory Address(ISP_MEMADDRL1, ISP_MEMADDRH1)..... 16-16
TABLE 16-26. External Memory Address(ISP_MEMADDRL2, ISP_MEMADDRH2)..... 16-16
TABLE 16-27. Image Signal Processor Source Pixel Width register(ISP_SRC_HWIDTH) 16-16
TABLE 16-28. Image Signal Processor Source Pixel Width Register(ISP_DST_HWIDTH)..... 16-17
TABLE 16-29. Bayer RGB Recovery Method(ISP_RGBREC)..... 16-17
TABLE 16-30. Horizontal Luminance Enhancement Gain(ISP_YGAIN)..... 16-18
TABLE 16-31. Horizontal Edge Enhancement Slice Limit(ISP_SLICELMT)…….16-18
TABLE 16-32. Contrast Control Register(ISP_CNTRSTAIN)..... 16-19
TABLE 16-33. Contrast Control Register(ISP_CNTRSTLIM) 16-19
TABLE 16-34. Brightness Register(ISP_BRIGHT)..... 16-20
TABLE 16-35. Clip Point& Color Suppress Register(ISP_CSUPSLANT) 16-21
TABLE 16-36. Hue Control For Each of 4 Coordinater Register 16-23
TABLE 16-37. Hue Control for Each of 4 Coordinates Register..... 16-24
TABLE 16-38. Clip & Color Suppress..... 16-25
TABLE 16-39. Clip Point & Color Suppress Register(ISP_YCLIP)..... 16-25
TABLE 16-40. Clip Pont & Color Suppress Register(ISP_YCLIPSLANT)..... 16-25
TABLE 16-41. Clip Point & Color Suppress Register(ISP_CSUPSLANT) 16-25
TABLE 16-42. Auto Exposure Accumulation Control Register(ISP_AELIM) 16-27
TABLE 16-43. Auto Exposure Accumulation Control Register(ISP_ AEVSTEP)..... 16-27
TABLE 16-44. Auto Exposure Accumulation Control Register(ISP_ AEHSTEP)..... 16-27
TABLE 16-45. Auto Exposure Result Register(ISP_AEACCH) 16-27
TABLE 16-46. Auto Exposure Result Register(ISP_AEACCL)..... 16-28

TABLE 16-47. Auto Focus Accumulation Register(ISP_AFACCL, ISP_AFACCH) 16-29
TABLE 16-48. Upper/ Lower Limit for White Balance Accumulation Register(ISP_WBLMT) 16-29
TABLE 16-49. Upper/ Lower Limit for White Balance Accumulation Register
(ISP_WBACCCNTH, ISP_WBACCCNTL) 16-30
TABLE 16-50. Upper/ Lower Limit for White Balance Accumulation Register
(ISP_WBCBACCH, ISP_WBCBACCL) 16-30
TABLE 16-51. Upper/ Lower Limit for White Balance Accumulation Register
(ISP_WBCRACCH, ISP_WBCRACCL) 16-30
TABLE 16-52. Color Coordinate Selection for White Balance Register(ISP_WBCOORD0) 16-30
TABLE 16-53. Color Coordinate Selection for White Balance Register(ISP_WBCOORD1) 16-31
TABLE 16-54. Color Coordinate Selection for White Balance Register(ISP_WBCOORD2) 16-31
TABLE 16-55. Color Coordinate Selection for White Balance Register(ISP_WBCOORD3) 16-31
TABLE 16-56. Color Coordinate Selection for White Balance Register(ISP_WBCOORD4) 16-31
TABLE 16-57. Color Coordinate Selection for White Balance Register(ISP_WBCOORD5) 16-31
TABLE 16-58. Color Coordinate Selection for White Balance Register(ISP_WBCOORD6) 16-32
TABLE 16-59. Color Coordinate Selection for White Balance Register(ISP_WBCOORD7) 16-32
TABLE 16-60. Color Coordinate Selection for White Balance Register (ISP_WBCOORD8) 16-32
TABLE 16-61. Color Coordinate Selection for White Balance Register(ISP_WBCOORD9) 16-32
TABLE 16-62. Color Coordinate Selection for White Balance Register(ISP_WBCOORD10) 16-32
TABLE 16-63. Color Coordinate Selection for White Balance Register(ISP_WBCOORD11) 16-33
TABLE 16-64. Color Coordinate Selection for White Balance Register(ISP_WBCOORD12) 16-33
TABLE 16-65. Color Coordinate Selection for White Balance Register(ISP_WBCOORD13) 16-33
TABLE 16-66. Color Coordinate Selection for White Balance Register(ISP_WBCOORD14) 16-33
TABLE 16-67. Color Coordinate Selection for White Balance Register(ISP_WBCOORD15) 16-33
TABLE 16-68. Possible Image Input Data Format and Related Port 16-35
TABLE 16-69. Image Signal Processor Registers List 16-48
TABLE 17-1. Pulse with Modulator Registers List 17-5
TABLE 18-1. PPM Controller Registers List 18-4
TABLE 19-1. OHCI REGISTERs for USB Host Controller 19-3
TABLE 19-2. USB DEVICE SPECIAL REGISTERS 19-7
TABLE 19-3. FUNCTION ADDRESS REGISTER(FUNC_ADDR_REG) 19-8

TABLE 19-5. INTERRUPT REGISTER(EP_INT_REG, USB_INT_REG) 19-9
TABLE 19-6. INTERRUPT REGISTER(EP_INT_REG, USB_INT_REG) 19-10
TABLE 19-7. INTERRUPT ENABLE REGISTER(EP_INT_EN_REG, USB_INT_REG) 19-10
TABLE 19-8. INTERRUPT ENABLE REGISTER(EP_INT_EN_REG, USB_INT_REG) 19-11
TABLE 19-9. FRAME NUMBER REGISTER(FRAME_NUM1_REG, FRAME_NUM2_REG) 19-11
TABLE 19-10. FRAME NUMBER REGISTER(FRAME_NUM1_REG, FRAME_NUM2_REG) 19-11
TABLE 19-11. INDEX REGISTER(INDEX_REG) 19-11
TABLE 19-12. END POINT0 CONTROL STATUS REGISTER(EP0_CSR) 19-12
TABLE 19-13. END POINT in CONTROL STATUS REGISTER(IN_CSR1_REG) 19-13
TABLE 19-14. END POINT in CONTROL STATUS REGISTER(IN_CSR2_REG) 19-14
TABLE 19-15. End Point out control status register(OUT_CSR1_REG) 19-15
TABLE 19-16. End Point out control status register(OUT_CSR2_REG) 19-16
TABLE 19-17. END POINT FIFO REGISTER(EP0_FIFO_REG) 19-16
TABLE 19-18. END POINT FIFO REGISTER(EP1_FIFO_REG) 19-16
TABLE 19-19. END POINT FIFO REGISTER(EP2_FIFO_REG) 19-17
TABLE 19-20. END POINT FIFO REGISTER(EP3_FIFO_REG) 19-17
TABLE 19-21. END POINT FIFO REGISTER(EP4_FIFO_REG) 19-17
TABLE 19-22. IN MAX Packet Register(IN_MAXP_REG) 19-17
TABLE 19-23. OUT MAX Packet Register(OUT_MAXP_REG) 19-18
TABLE 19-24. END POINT Out Write Count REGISTER(OUT_FIFO_CNT1_REG) 19-18
TABLE 19-25. END POINT Out Write Count REGISTER(OUT_FIFO_CNT2_REG) 19-18
TABLE 19-26. DMA INTERFACE CONTROL REGISTER(EP1_DMA_CON) 19-19
TABLE 19-27. DMA INTERFACE CONTROL REGISTER(EP2_DMA_CON) 19-20
TABLE 19-28. DMA INTERFACE CONTROL REGISTER(EP3_DMA_CON) 19-21
TABLE 19-29. DMA INTERFACE CONTROL REGISTER(EP4_DMA_CON) 19-22
TABLE 19-30. DMA FIFO COUNTER REGISTER(EP1_DMA_FIFO) 19-22
TABLE 19-31. DMA FIFO COUNTER REGISTER(EP2_DMA_FIFO) 19-23
TABLE 19-32. DMA FIFO COUNTER REGISTER(EP3_DMA_FIFO) 19-23
TABLE 19-33. DMA FIFO COUNTER REGISTER(EP4_DMA_FIFO) 19-23
TABLE 19-34. DMA TOTAL Transfer Counter REGISTER
(EP1_DMA_TTC_L, EP1_DMA_TTC_M, EP1_DMA_TTC_H) 19-23

TABLE 19-35. DMA TOTAL Transfer Counter REGISTER
(EP2_DMA_TTC_L, EP2_DMA_TTC_M, EP2_DMA_TTC_H) 19-24
TABLE 19-36. DMA TOTAL Transfer counter REGISTER
(EP3_DMA_TTC_L, EP3_DMA_TTC_M, EP3_DMA_TTC_H) 19-24
TABLE 19-37. DMA TOTAL Transfer counter REGISTER
(EP4_DMA_TTC_L, EP4_DMA_TTC_M, EP4_DMA_TTC_H) 19-25
TABLE 19-38. USB DEVICE REGISTERS LIST 19-29
TABLE 20-1. I^2C -BUS INTERFACE REGISTER 20-15
TABLE 21-1. SPDIF Input Data Format 21-4
TABLE 21-2. SPDIF Output Data Format 21-4
TABLE 21-3. SPDIF Control Register (SPDIFCON) 21-5
TABLE 21-4. SPDIF Interrupt Enable Register (SPDIFINTENB) 21-5
TABLE 21-5. SPDIF Interrupt Status Register (SPDIFSTATUS) 21-5
TABLE 21-6. SPDIF TX Clock Divider Register (SPDIFTXDIV) 21-6
TABLE 21-7. SPDIF CONTROLLER REGISTERS LIST 21-6
TABLE 22-1. External Interface Signal 22-3
TABLE 22-2. AC97 Control Register (AC_CTRL_REG) 22-7
TABLE 22-3. AC_CONFIG_REG 22-7
TABLE 22-4. AC_STA_ENA_REG 22-9
TABLE 22-5. AC_STATUS_REG 22-10
TABLE 22-6. AC_STATE_MACHINE 22-11
TABLE 22-7. AC_CODEC_ADDR 22-11
TABLE 22-8. AC_CODEC_DATA 22-11
TABLE 22-9. AC_CODEC_ACCESS 22-12
TABLE 22-10. AC97 REGISTER LIST 22-18
TABLE 23-1. PIN DESCRIPTION 23-2
TABLE 23-2. I2S Control Register 23-3
TABLE 23-3. I2S Configuration Register 23-4
TABLE 23-4. I2S Status Enable Register 23-4
TABLE 23-5. I2S Status Register 23-5
TABLE 23-6. I2S CONTROLLER REGISTER LIST 23-9

TABLE 24-1. PIN DESCRIPTION 24-3
TABLE 25-2. SSP/SPI CONTROLLER REGISTERS LIST 24-6
TABLE 25-1. PIN DESCRIPTION 25-4
TABLE 25-2. TRANSPORT STREAM I/F REGISTERS LIST 25-5
TABLE 26-1. Clock Control Register(TPC_CLK_CNTL) 26-4
TABLE 26-2. Control Register(TPC_CNTL) 26-4
TABLE 26-3. Sampling Rate Control Parameters 26-5
TABLE 26-4. Timing Parameter Register 1(TPC_TIME_PARM1) 26-5
TABLE 26-5. Timing Parameter Register 2(TPC_TIME_PARM2) 26-5
TABLE 26-6. Sampling Rate Calculation 26-6
TABLE 26-7. MANUAL MODE OPERATION 26-6
TABLE 26-8. X Value Register(TPC_X_VALUE) 26-7
TABLE 26-9. Y Value Register(TPC_Y_VALUE) 26-7
TABLE 26-10. Auto Zero Value Register(TPC_Y_VALUE) 26-7
TABLE 26-11. U1 Value Register(TPC_U1_VALUE) 26-8
TABLE 26-12. U2 Value Register(TPC_U2_VALUE) 26-8
TABLE 26-13. AUTO MODE OPERATION 26-8
TABLE 26-14. Switch Default Control 26-9
TABLE 26-15. Data Format 26-11
TABLE 26-16. Data Type 26-11
TABLE 27-1. PIN DESCRIPTION 27-2
TABLE 27-2. SDI Control Register (SDICON) 27-5
TABLE 27-3. SDI Prescaler Register (SDIPRE) 27-5
TABLE 27-4. SDI Command Argument Register Low (SDICmdArgL) 27-7
TABLE 27-5. SDI Command Argument Register High (SDICmdArgH) 27-7
TABLE 27-6. SDI Command Control Register (SDICmdCon) 27-8
TABLE 27-7. SDI Command Status Register (SDICmdSta) 27-8
TABLE 27-8. SDI Response Register 0 (SDIRSP0) 27-9
TABLE 27-9. SDI Response Register 1 (SDIRSP1) 27-9
TABLE 27-10. SDI Response Register 2 (SDIRSP2) 27-9
TABLE 27-11. SDI Response Register 3 (SDIRSP3) 27-9

TABLE 27-12. SDI Response Register 4 (SDIRSP4) 27-9
TABLE 27-13. SDI Response Register 5 (SDIRSP5) 27-10
TABLE 27-14. SDI Response Register 6 (SDIRSP6) 27-10
TABLE 27-15. SDI Response Register 7 (SDIRSP7) 27-10
TABLE 27-16. SDI BLOCK SIZE REGISTER (SDIBSize) 27-10
TABLE 27-17. SDI DATA CONTROL REGISTER LOW(SDIDatConL) 27-11
TABLE 27-18. SDI Data Control Register High (SDIDatConH) 2711
TABLE 27-19. SDI Data Remain Counter Register Low (SDIDatCntL) 2711
TABLE 27-20. SDI Data Remain Counter Register High (SDIDatCntH) 27-12
TABLE 27-21. SDI Data Status Register (SDIDatSta) 27-12
TABLE 27-22. SDI FIFO Status Register (SDIFSTA) 27-13
TABLE 27-23. SDI Data Register (SDIDAT) 27-13
TABLE 27-24. SDI Interrupt Mast Register0 (SDIIntMsk0) 27-14
TABLE 27-25. SDI Interrupt Mast Register1 (SDIIntMsk1) 27-15
TABLE 27-26. SDI Data Timer Register Low (SDIDTimerL) 27-15
TABLE 27-27. SDI Data Timer Register High (SDIDTimerH) 27-15
TABLE 27-28. SDI Shift Register Low (SDSftRegL) 27-15
TABLE 27-29. SDI Shift Register High (SDSftRegH) 27-16
TABLE 27-30. REGISTER MAP 27-21
TABLE 28-1. Interface Signal 28-3
TABLE 28-2. MEMORY STICK CONTROLLER REGISTERS LIST 28-7
TABLE 29-1. CDP Input Format Register (CDPIFORMAT) 29-6
TABLE 29-2. CDP Decoding Control Register (CDPDECCTRL) 29-6
TABLE 29-3. CDP Raw Data Base Address #0 Register (CDPRAWADDR0L/H) 29-7
TABLE 29-4. CDP Raw Data Base Address #1 Register (CDPRAWADDR1L/H) 29-7
TABLE 29-5. CDP Decoded Data Base Address Register (CDPDECADDRL/H) 29-7
TABLE 29-6. CDP Timeout Register (CDPTIMEOUT) 29-7
TABLE 29-7. CDP Target & RAW Sec/Frame Control Register (CDPTRGRAWSECFRAME) 29-8
TABLE 29-8. CDP ECC&EDC Min/Mode Control Register (CDPECDMODEMIN) 29-8
TABLE 29-9. CDP ECC&EDC Sec/Frame Control Register (CDPECDSECFRAME) 29-8
TABLE 29-10. CDP Current Min/Mode Control Register (CDPCURMODEMIN) 29-8

TABLE 29-11. CDP Current Sec/Frame Control Register (CDPCURSECFRAME) 29-8
TABLE 29-12. CDP Interrupt Control Register (CDPINTP) 29-9
TABLE 30-1. PIN DESCRIPTION 30-2
TABLE 30-2. OWM Command Register (OWM_CMD) 30-4
TABLE 30-3. OWM Data Buffer Register (OWM_BUF) 30-9
TABLE 30-4. Status Register 30-11
TABLE 30-5. OWM Status Register (OWM_STA) 30-12
TABLE 30-6. Clock Divisor Register 30-13
TABLE 30-7. OWM Clock Divisor Register (OWM_CLK_DIVISOR) 30-13
TABLE 30-8. IRQ Register 30-13
TABLE 30-9. Command Register (OWM_CMD) 30-15

MAGIC EYES

UPDATE HISTORY

Ver 0.91 : 2004/2/26

- Chapter 1. Introduction / Key Features → Edit
- Chapter 2. I/O Pin Description -> Edit

  Table 2-3. MP2520F Pin out – Ball pad Number Order → Edit

  Table 2-4. System configuration → Edit
- Chapter 7. DMA Controller

  Block Diagram → Edit

  Table 7-1. Peripheral Index Table → Add

  Chapter 7.3 Operation → Text Edit

  Table 7-4. DMA Controller Register List → Edit
- Chapter 16. Image Signal Processor

  Table 16-5. Sync Control Register (ISP_H_Width) → Edit

  Table 16-5. Sync Control Register (ISP_V_Height) → Edit

  Table 16-28. Bayer RGB Recovery Method → Edit

  Chapter 16.2.6.2 Contrast → Text Edit

  Chapter 16.2.11 Auto White Balance → Text Edit
- Chapter 20. USB Host / Device

  Chapter 20.2 USB Device Register Map (Address) → Edit

Ver 0.92 : 2004/4/20

- Table 2-1. nPWRRGLTOn → Descripsions Add
- Table 2-4. System Configuration → Edit
- Chapter 3.5 Bank C Memory Control Register → Address Edit
- Table 5-20. Power Mode Sequence Table → Edit
- Table 28-3. SDI Prescaler Register (SDIPRE) → Edit

Ver 0.93 : 2004/5/24

- Table 5-21. Clocks and Power Registers List → Edit
- Table 6-11/12. Reset Value → Edit

- Table 7-4. DMA Registers List → Edit
- Table 10-14. UART Registers List → Edit
- Chapter 14. Registers → Edit
- Chapter 15. Registers → Edit
- Table 16-1. ISP Sync Control Register (ISP_VPERIOD) → Add
- Table 16-28. Bayer RGB Recovery Method (ISP_RGBREC) → Edit
- Table 20-1. OHCI Registers form USB Host Controller → Base Address Edit
- Table 21-1. I2C-Bus Interface Register → Address Edit
- Table 25-2. SSP/SPI Control Register → Edit

Ver 0.94 : Not Released

Ver 0.95 : 2004/8/30

- Figure 2-2. MP2520F Package FBGA Ball Map : U18 (GND → VDDOP)
- Table 2-1. Signal Descriptions for MP2520F : Transport Stream I/F Pins → Add
  SSP Pins → Add
- Table 2-4. GPIOB[13]/VD[5] : Ball → (J4 →K4) Edit
- Figure 3-1. Memory Controller Block Diagram → Edit
- Chapter 3.2.1 MCU-C BANK (Chapter D, E, F, G) → Add Comment
- Table 3-3~7. Bank C Timing Regster #0, #1, #2, #3, #4, → Edit
- Table 3-8. Bank C Wait Control Register → Edit
- Table 3-16. Bank C DMA Timeout Register → Edit
- Table 3-28. Bank C NAND Flash CTRL Register → Edit
- Chapter 3.4 NAND BOOT OVERVIEW : cfgNFSize 16/32KB → 512Byte
- Table 3-24. Bank C NAND FLASH CTRL REGISTER : Bit → Edit
- Table 3-28. Bank C NAND FLASH CTRL Register : Bit[5] → Edit
- Chapter 3.6 Bank A Memory Control Register Address : C000 54xxh → C000 38xxh
- Table 4-1. Dual CPU Control Register List → Edit
- Chapter 6.2 RTC Counter Set Register (RTCTSETREG) description → Add
- Table 7-4. DMA Controller Register List : DMA Command Register 0 → Edit
  DMA Control/Status Register → Edit
- Table 9-1. Timer Counter Register : 0.27uSec → 0.135uSec
- Chapter 1.10 LCD Controller description → Edit
- Chapter 11. GPIO → Full Edit

- Table 14-32. Display Controller Regiser List Address → All Edit
- Chapter 15.2 2D Graphic Accelerator Operation → Add
- Table 15-18~22. Table Deleted
- Chapter 19. IrDA → Deleted
- Table25-2. SP / SPI Controller Register List → SSP/SPI Data Register Edit
- Chapter 28.3.6.2 Multiple Block Write with DMA and wide Bus → Deleted
- Chapter 28.3.6.4 Multiple Block Read with DMA and wide data line → Deleted
- Table 28-17. SDI Block Size Register : Bit [15] → Reserved
- Table 28-30. SD/MMC Controller Register Map : SDI Data Control Register Low (Bit 14, 15) → Deleted
  SDI Interrupt Mast Register 0, 1 : RW → W

CHAPTER 1

INTRODUCTION

1. INTRODUCTION

1.1 GENERAL DESCRIPTION

MP2520F is the 2nd generation MagicEyes Digital's Multimedia Signal Processor. **MP2520F** is a super-integrated SoC (system on a chip) aimed at providing high performance multimedia functionality and low power consumption for Personal Multimedia Digital Assistants.

MP2520F incorporates a Dual 32bit CPU Processor, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor and a variety of I/O peripheral components. **MP2520F** can significantly reduce system costs by eliminating not only the system control CPU, but also the Graphic IC, DVD Decoder (MPEG2 Video + Dolby AC3 Audio) IC, MPEG4 Codec IC, Camera Image Processor IC, as well as the USB Host IC. **MP2520F** helps system designers reduce engineering effort and time taken to develop a new system, by adding only memory and I/O devices such as the LCD panel, HDD, DVD-ROM, Modem module and human I/F devices.

Therefore **MP2520F** is the best solution for high-end Multimedia PDAs, DVD/DivX Players, multi-functional Digital Cameras, Portable Visual Players, Smart Phones, MoIP (Multimedia over IP) Phones, DVRs, Security Cameras over IP, and Car Infotainment.

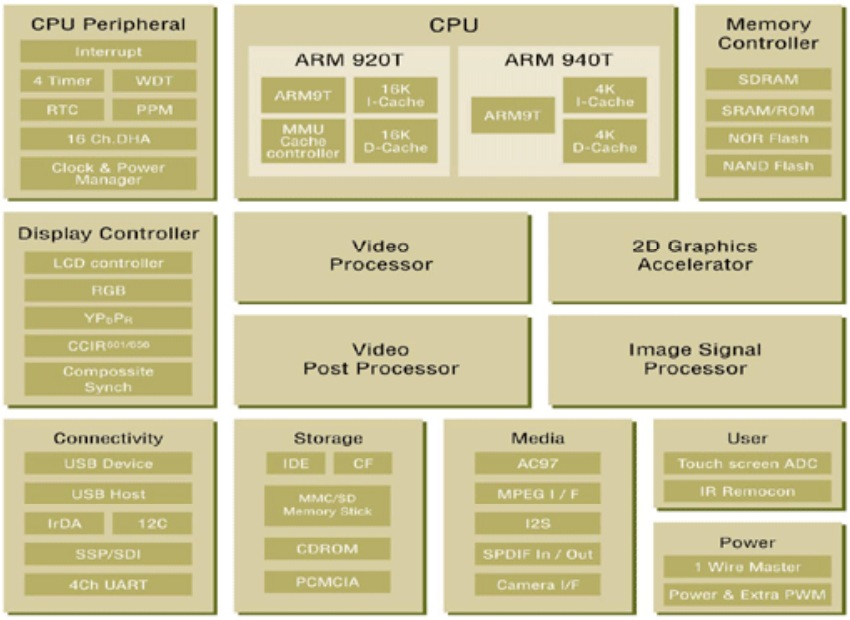


Figure 1-1. Top Level Block Diagram

1.2 KEY FEATURES

- 0.18um, 1.8V CMOS Process Technology.
- 400 pin FBGA (Fine BGA) Package, 18 x 18 mm^2
- Dual 32bit CPU 400+ (Main Processor, Coprocessor) Embedded Architecture
  - Main Processor used for Operating System & System Control, Audio Processing: ARM 920T CPU (200MHz, >220MIPS), 16KB I-Cache + 16KB D-Cache + MMU
  - Coprocessor used for Video Header Parsing, Video Post Processor Control: ARM 940T CPU (200MHz, >220MIPS), 4KB I-Cache + 4KB D-Cache
- Multi Standard Video Codec including MPEG1/2/4, H.263 and JPEG/MJPEG
- Multi Functional Video Post Processor
- Win CE 3.0/4.0 Compatible 2D Graphic Accelerator
- Image Processor with Real Time Digital Zoom & Three (3) Auto Processing
- Pseudo Message Broadcasting with Command Write Buffer Memory Control Bus Architecture for High Performance Pipelined & Burst Data Operation
- USB 1.1 Host Controller, USB 1.1 Slaver, SIR, 4CH UART
- LCD Controller, 16CH.DMA, Timer, Interrupt Controller, RTC, Ultra DMA
- PCMCIA, Compact Flash, MMC, SD, Memory Stick Controller
- AC97 Controller, SPDIF In/Out Controller, CD-ROM Decoder, DeCSS, MPEG I/F, RDI I/F
- I^2C, I^2S, SSP, Touch Screen ADC, GPIOs, PWM, Power Manager
- Whole Chip Operating Clock 100MHz

1.3 FUNCTIONAL SPECIFICATION

Video (H/W Video Processor):

- MPEG1 Decode (Video CD)
- MPEG2 MP@ML Encoder (P, I frame only) / Decode (DVD playback, SD-TV)
- MPEG4 ASP Decode @720 x 480, 30fps (DivX 3.11/4.x/5.x Playback)
- MPEG4 SP Encoder / Decode @720 x 480, 30fps (MPEG4 Camcorder, PVR, MMS)
- MPEG4 SP/H.263 L3 Codec @352 x 288, 30fps (Video Conferencing)
- JPEG Encode or Decode up to 4M pixels (DSC)
- MJPEG Encode or Decode @720 x 480, 30fps (Security Camera)

Speech & Audio (ARM920T CPU S/W):

- Need software development or porting at ARM 920T
- Support from WinCE.NET: MP3, WMA
- License from 3rd party: G.723.1/G.729/AMR Speech Codec, ADPCM (G.722/G.726) Codec, AC-3
- MPEG1/2 Audio Codec, AAC-LC
- Support from MagicEyes: PCM

System (ARM920T CPU S/W) :

- DVD, H.323/H.324M, MPEG4 System, SIP

High Performance 2D Graphics & LCD Controller (H/W)

- Resolution up to 1024 x 768 @ 60Hz
- Two (2) Hardware Video Overlay Surface Support

1.4 INTERNAL BUS ARCHITECTURE

MP2520F has a unique internal bus architecture, which consists of one DRAM memory bus, one Non-DRAM memory & Fast I/O bus, one I/O Peripheral bus and one local data bus. Nine memory bus masters including ARM920T^{TM} CPU, ARM940T^{TM} CPU, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor, LCD Controller, USB Host and DMA can access either internal DRAM memory bus or Non-DRAM memory & Fast I/O bus independently. ARM920T^{TM} CPU, ARM940T^{TM} CPU and DMA are the masters of the I/O Peripheral bus. DMA can read and/or write data from/to the Huffman Controller resident in the Video Post Processor directly through one local data bus.

MP2520F can handle four parallel data access operations through allowing four out of nine bus masters to access one of four internal data buses independently and concurrently. For example, MP2520F allows the ARM920T^{TM} CPU to access I/O components though the I/O Peripheral bus, while one of the 16 DMAs to access the Huffman Controller via the local data bus, another DMA to access external I/O components via the Fast I/O bus, and the Video Processor to access external SDRAM through the DRAM memory concurrently.
One local data bus consists of one data read bus and one data write bus. Therefore two out of the sixteen (16) channel DMAs can read and write data from/to the Huffman Controller simultaneously.
There is a pipelined operation between the Video Post Processor and LCD controller, which can display the decoded YUV video signal on the LCD panel directly, through multiple signal processing operations such as de-blocking, de-ring, image scaling down or up, CSC (color space converting) and color dithering. Additionally there is a pipelined operation between the Image Signal Processor and Video Processor, which can support any size of camera input image pixel resolution to be scaled down matching the LCD display pixel resolution size with the CSC operation in real time, without accessing the external video frame buffer. Those pipelined operation structures can significantly reduce external memory bandwidth requirements.

1.5 MEMORY CONTROLLER

The benefits of the super-integration of the ARM920T™ CPU, Video Processor, Video Post Processor, 2D Graphic Processor, Image Signal Processor and LCD Controller into one chip are as follows:

1) Availability of a simple and unified common system memory usage

2) No necessity for data transfer operations between Host CPU and Video Processor, Video Post Processor, 2D Graphic Processor and Image Signal Processor. It can reduce CPU horsepower requirement and external memory bandwidth requirements as well as total power consumption at system level.

The DRAM and Non-DRAM memory bus controllers have a sixteen level individual command & data write buffer in order to enable all nine memory bus masters to access either external DRAM or Non-DRAM memory devices in burst and pipelined operation mode (without having to wait for its and/or the other memory bus masters' data to be completely written to the external memory). The DRAM memory controller can interface with various types of SDRAM memory devices. The Non-DRAM memory controller can interface with various types of Non-DRAM memory device such as SRAM, ROM, NAND/NOR Flash, PCMCIA and Compact Flash.

1.6 2D GRAPHIC PROCESSOR

MP2520F's 2D Graphic Processor accelerates the WinCE™ GDI and Direct2D™ operation without sacrificing CPU horsepower. This feature guarantees the high-resolution (up to 1024x768 pixel) display performance. Additionally it supports two hardware Video Overlay Surface acceleration, which provides two independent YUV video display windows on an RGB graphic window. It allows two different YUV video signals to be scaled down or up, to the size of each video display window, and converted simultaneously into RGB signals in real time.

1.7 IMAGE SIGNAL PROCESSOR

MP2520F's Image Signal Processor supports a CIS/CCD back-end image processing operation, which includes Auto Focus, Auto Exposure and Auto White Balance functionality. It also has Gamma Correction functionality. It can handle CCIR601 and CCIR656 video formats.

1.8 VIDEO PROCESSOR

MP2520F's Video Processor can support multiple standard video codec functionality including MPEG1/2/4, DivX 3.11/4.x/5.x, H.263 and JPEG standard. The Video Processor consists of multiple macro-functional H/W blocks including VLD/VLC, DCT/IDCT, Q/IQ, ME, MP, MC, De-Block, De-Ring and SP(stream packet processor).

1.9 VIDEO POST PROCESSOR

MP2520F's Video Post Processor consists of multiple macro-functional H/W blocks including a video signal scaling block and OSD, sub picture, hardware cursor, hue control, contrast, brightness, dithering, gamma, alpha blending, color key and CSC(color space converting) blocks. Video signal scaling can provide a high precision video signal zoom-in/out functionality to support SD-TV level video quality even during digital zoom-in or zoom-out operations. Also it enables a high resolution CCD/CIS camera image signal to be displayed on the LCD panel, with scaling down to the LCD display panel resolution size being done in real time. Also either the original camera image or the scaled down image can be recoded selectively.

MP2520F can support up to four (4) screen split functionality with independent scaling, 90/180/270 degree rotation, and a mirror effect. MP2520F can also support a letterbox and Pan/Scan conversion functionality.

MP2520F can support three (3) staged alpha blending operations and six (6) level video mixing operations using two (2) YUV video sources, OSD, Sub Picture, RGB graphics and H/W cursor.

1.10 LCD CONTROLLER

MP2520F's LCD Controller (LCDC) generates the data and timing for active display. It has a variety of user-programmable options including display type and size, output data width, and output data type.

Display sizes up to 1024x768 pixels are supported. However, Bit per pixel (BPP) limits the maximum size screen the LCDC can drive, due to the memory bandwidth. The digital video output supports 12bit/16bit/18bit/24bit RGB, 8bit/12bit Multiplexed RGB (MRGB), and CCIR656, CCIR601, 4:4:4 YCbCr. The MRGB output mode supports the external DVI transmitter.

1.11 USB HOST CONTROLLER

MP2520F has aUSB Host Controller 1.1, which makes it possible to enhance or upgrade the system easily by introducing a number of optional modules via the USB connector. Those optional modules can include a camera, portable printer, portable scanner, IC card reader etc.

1.12 NAND FLASH CONTROLLER FOR H/W BOOTLOADER

MP2520F can provide a cost effective solution for program memory, using NAND type FLASH memory instead of the expensive NOR type. It automatically loads the operating system resident in NAND type FLASH memory into the system memory (SDRAM or SRAM), before the CPU accesses the operating system when MP2520F boots up. It also supports a H/W Bootdown function that allows a PC to update the system program memory contents directly via the UART I/F port. This can eliminate the use of any kind of boot program device such as PROM or Mask ROM in the system, thus saving money as well as system board space.

1.13 IDE CONTROLLER

MP2520F has an Ultra DMA 66MHz functional block, which can access external HDD, DVD-ROM and CD-ROM devices directly without using any glue logic.

1.14 USB DEVICE

MP2520F has a USB function controller. The USB function controller is designed to provide a high performance full speed function controller solution with DMA I/F. The USB function controller allows bulk transfer with DMA, interrupt transfer and control transfer.

1.15 UART

MP2520F's UART unit provides four independent asynchronous serial I/O (SIO) ports, each of which can operate in interrupt-based or DMA-based mode. In other words, UART can generate an interrupt or DMA request to transfer data between CPU and UART. It can support bit rates of up to 115.2K bps. Each UART channel contains two 16-byte FIFOs for receive and transmit. The MP2520F UART includes programmable baud-rates, one or two stop bit insertion, 5-bit, 6-

bit, 7-bit or 8-bit data width and parity checking. Each UART contains a baud-rate generator, transmitter, receiver and control unit. The baud-rate generator can be clocked by PCLK. The transmitter and the receiver contain 16-byte FIFOs and data shifters. Data which is to be transmitted, is written to FIFO and then copied to the transmit shifter. It is then shifted out by the transmit data pin (TxDn). The received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

1.16 I^2C

MP2520F can support a multi-master I^2C-bus serial interface. A dedicated serial data Line (SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices that are connected to the I^2C-bus. The SDA and SCL lines are bi-directional.

1.17 SPDIF CONTROLLER

The SPDIF Controller supports Standard IEC958 Digital audio interface and Input/Output Mode. It enables to transmit high speed data with the DAM controller.

1.18 AC97 CONTROLLER

The AC97 Controller Unit can support AC97 revision 2.2 features. The AC97 Controller and External codec communicate via an AC-link. AC-link is a serial interface for transferring digital audio, Mic-in, Codec register control, and status information. The AC97 Codec sends the digitized audio samples that the AC97 Controller Unit stores in memory. For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the Codec through the AC-link. The digital-to-analog converter (DAC) in the Codec then converts the audio sample to an analog audio waveform. This chapter describes the programming model for the AC97 Controller Unit. The information in this chapter requires an understanding of the AC97 revision 2.2 specification.

1.19 I^2S CONTROLLER

The I^2S controller provides a serial link to standard I^2S CODECs for digital stereo audio. It supports both the Normal-I^2S and MSB-Justified I^2S formats, and provides four signals for connection to an I^2S CODEC. I^2S Controller signals are multiplexed with AC97 Controller pins. The controller includes FIFOs that support DMA access to memory.

1.20 SD/MMC CONTROLLER

The MMC is a universal low cost data storage and communication medium implemented as a hardware card with a simple control unit and a compact, easy-to-use interface that is designed to cover a wide variety of applications such as electronic toys, organizers, PDAs, and smart phones. MMC communication is based on an advanced 6-pin serial bus designed to operate in a low voltage range at medium speed (20 Mbps).

The SD is an evolution of the MMC with an additional 2 pins in a form factor that is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in new audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are compatible with the MMC. The SD is composed of a memory card and an I/O card. The memory card includes a copyright protection mechanism that complies with the security requirements of the Secure Digital Music Initiative (SDMI) standard, and is faster and has a higher

memory capacity. The I/O card combines high-speed data I/O with low-power consumption for mobile electronic devices. The MMC/SD Host Controller module (MMC/SD module) integrates MMC support with SD memory and I/O functions. The copyright protection mechanism employs mutual authentication and a new cipher algorithm, and is handled in software post-processing.

1.21 DMA CONTROLLER

The DMA Controller transfers data to and from main memory in response to requests generated by internal and external peripherals. The peripherals do not directly supply addresses and commands to the memory system. The DMA Controller has 16DMA channels, 0 through 15, and every DMA request from the peripheral generates at least one memory bus cycle.

1.22 PWM CONTROLLER

MP2520F contains two pulse width modulators: PWM0 and PWM1. Each PWM is controlled by its own set of registers. The PWM unit is clocked off the 7.3728MHz oscillator output and produces a pulse width modulated output signal. Each register contains one or more fields which determine an attribute of the PWMOUTn waveform.

1.23 CLOCK & POWER MANAGER

The Clocks and Power Manager block controls the power mode and the clock frequency of each module. This block has two clock sources. One is EXTCLK and the other is XTI that is a Crystal input. One of these two clock sources is multiplexed according to **MP2520F**'s operation mode and used for the input clock of the PLL. After that, the clock frequency is divided in the CLKGEN block in accordance with the divider register value set. In addition, the divided clock is used for the input clock of the BCLKCTRL, PCLKCTRL and VCLKCTRL blocks, and these blocks divide the clock using the Control Register or cut off. The **MP2520F** power mode consists of Normal, Idle, Sleep, Deep Sleep and Stop Modes. The CPU can execute each Power Mode by setting a PWRMODE register.

1.24 RTC CONTROLLER

The real-time clock (RTC) provides a general-purpose real-time reference. It is a free running counter and starts incrementing the count value after the de-assertion of reset. The counter is incremented on rising edges of the 1Hz clock. Set this counter to the desired value.

The RTC incorporates a 32-bit RTC Alarm register. This may be programmed with a value that is compared against the RTC Time Counter register. On each rising edge of the 1Hz clock, the counter is incremented and then compared to the RTC Time Counter register. This status bit is also routed to the interrupt controller and may be unmasked in the interrupt controller to generate a processor interrupt. The clock is generated by dividing the clock source: 32.768 kHz. The divide logic is programmable as unit time is 32.768KHz.

1.25 TIMER / WATCH DOG TIMER

MP2520F contains a 32-bit timer that is clocked by the 7.3728MHz oscillator. The TCOUNT register is a free running upcounter. The timer also contains four 32-bit match registers (TMATCH0, TMATCH1, TMATCH2, TMATCH3). You can read and write to each register. When the value in the TCOUNT is equal to the value within any of the match registers, and the interrupt enable bit is set, the corresponding bit in the TSTATUS is set. These bits are also routed to the interrupt controller where they can be programmed to cause an interrupt.

TMATCH3 also serves as a watchdog timer enable register that resets the **MP2520F** when a match occurs, provided the TCONTROL is set. You must initialize the TCOUNT and TMATCHn registers and clear any set status bits before the FIQ and IRQ interrupts are enabled within the CPU.

1.26 INTERRUPT CONTROLLER

MP2520F has two interrupt controllers. One is the controller for ARM920T and the other is the controller for ARM940T. Interrupt controllers in **MP2520F** receive requests from 28 interrupt sources. These interrupt sources are provided by internal peripherals such as the DMA controller, UART, IIC etc.

The role of the interrupt controller is to ask for the FIQ or IRQ interrupt requests to the ARM920T core after the arbitration process when there are multiple interrupt requests from internal peripherals and external interrupt request pins. The arbitration process is performed by the hardware priority logic and the result is written to the interrupt pending register.

1.27 TRANSPORT STREAM INTERFACE

This block receives the output of the MPEG transport chip decoder, and then transmits data to the Main Memory using the MP2520F's FastDMA.

1.28 ADC & TOUCH PANEL CONTROLLER

The Touch Panel Controller (TPC) controls the switch, comparator, and ADC to read the X, Y position of the TOUCH PANEL touched. It also reads data form any ADC Channel. All Data is transmitted to external memory using the DMA.

1.29 MEMORY STICK

The MP2520F provides a Memory Stick Controller to access SONY Memory Sticks. This controller automatically creates H/W Protocol defined by the Memory Stick, and supports Card In/Out Detect and Memory Stick Interrupt functions.

Data transferred from/to the Memory Stick is stored in an Internal Data FIFO. Therefore the CPU can access Data in PIO Mode and transmit to the Memory via the DMA.

1.30 CD-ROM DECODER

The CDRSYNCDESC block receives a CDP signal input from external and detects Sync. This block then descrambles the signal according to CDRD_DESCENB or writes Data to the Memory.

If Sync is detected, the block writes 2340 Bytes unconditionally. If, however, Data error occurs or new Sync is detected before writing, the block stops the writing operation and generates o_EndRAW.

1.31 1-WIRE MASTER

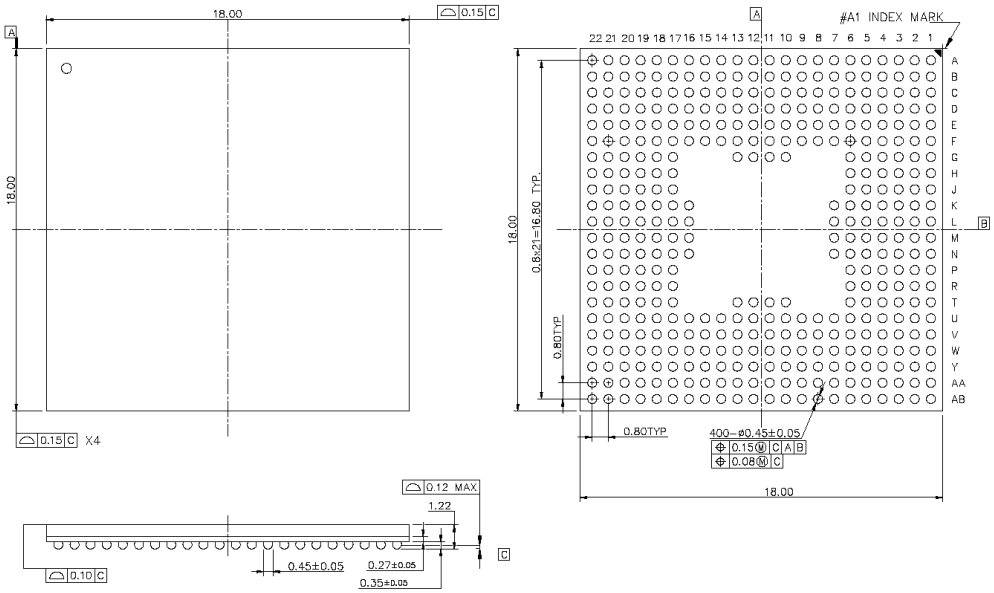
The 1-Wire Master supports 1-wire bus communication with 1-wire devices. 1-Wire Master generates all 1-wire timing and control signals and supports variable peripheral bus clock with clock divider (up to 100MHz).

CHAPTER 2

I/O PIN DESCRIPTIONS

2. I/O PIN DESCRIPTIONS

2.1 Mechanical Dimensions



Package Information

ITEM	DETAILS
UNIT	mm
Package Size	18.0TYP X 18.0TYP
Tolerance	±0.10
Ball Count	400 Balls
Ball Pitch	(x, y)=(0.8TYP, 0.8TYP)
Package Height	1.22TYP

Figure 2-1. MP2520F Package

2.2 MP2520F SIGNALS REFERENCE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VDDADC	VDDOP	DP1	GPIO[4]	GPIO[5]	GPIO[5]	GPIO[7]	nRESET	nPORSEL	XA[1]	XA[4]	XA[9]	XD[31]	XD[29]	XD[27]	XD[25]	XD[23]	XD[21]	XD[19]	XD[17]	GND	GND	A
B	VDDAPLL	ADCIN1	ADCIN3	ADCIN4	DP0	GPIO[0]	GPIO[6]	GPIO[9]	GPIO[10]	SDCLK	XA[0]	XA[5]	XD[30]	XD[28]	XD[26]	XD[24]	XD[22]	XD[20]	XD[18]	XD[16]	XD[15]	XD[14]	B
C	XTIRTC	XTORTC	VSSADC	ADCIN0	ADCIN2	DN0	DP2	VDDALIVE2	VDDOP	GPIO[11]	nBATTF	XA[2]	XA[6]	XA[8]	XBA[1]	VDDOPALIVE	GND	GND	GND	GND	XD[13]	XD[12]	C
D	XTI	XTO	VDDUPLL	VSSAPLL	ADCIN5	DN1	VDDOP	GPIO[2]	VDDI	GPIO[13]	EXTIN0	XA[3]	XA[7]	XA[10]	XBA[0]	VDDOPALIVE	GND	GND	GND	GND	XD[11]	XD[10]	D
E	GPIO[9]	GPIO[14]	VDDFPLL	VSSUPLL	GND	VREF	DN2	VDDI	GPIO[3]	GPIO[8]	VDDI	EXTIN1	VDDALIVE1	XA[11]	XA[12]	GND	GND	GND	GND	VDDOPALIVE	XD[9]	XD[8]	E
F	GPIO[7]	GPIO[11]	VDDRTC	VSSRTC	VSSFPLL	GND	GND	GPIO[0]	GPIO[4]	GPIO[10]	VDDI	nPWRRGLTON	VDDOPALIVE	GND	GND	GND	GND	GND	GND	VDDOPALIVE	XD[7]	XD[6]	F
G	GPIO[3]	GPIO[8]	GPIO[12]	GPIO[13]	VDDOP	GPIO[15]	NC	NC	NC	GND	GPIO[12]	TEST_EN	VDDOPALIVE	NC	NC	NC	GND	GND	SCKEX	VDDALIVE1	XD[5]	XD[4]	G
H	GPIO[0]	GPIO[4]	GPIO[6]	VDDI	GPIO[10]	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	nSCSX1	nSCSX0	VDDOPALIVE	XD[3]	XD[2]	H
J	GPIO[14]	GPIO[15]	VDDOP	GPIO[2]	GPIO[5]	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	nSWEX	nSRASX	nSCASX	XD[1]	XD[0]	J
K	GPIO[8]	GPIO[11]	GPIO[12]	GPIO[13]	GPIO[10]	GPIO[1]	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GND	SDQM0	VDDI	SDQM3	SDQM1	SDQM2	K
L	GPIO[7]	GPIO[4]	GPIO[8]	GPIO[5]	GPIO[9]	VDDI	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GND	GPIO[5]	GPIO[1]	GPIO[2]	GPIO[3]	GPIO[0]	L
M	GPIO[2]	GPIO[0]	GPIO[1]	VDDALIVE2	VDDOP	GPIO[3]	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPIO[0]	GPIO[4]	GPIO[1]	VDDOP	GPIO[7]	GPIO[4]	M
N	GPIO[14]	GPIO[13]	GPIO[10]	GPIO[11]	GPIO[12]	GPIO[7]	GND	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPIO[10]	GPIO[8]	GPIO[5]	VDDI	GPIO[2]	GPIO[6]	N
P	GPIO[9]	GPIO[8]	GPIO[5]	VDDI	GPIO[3]	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDI	GPIO[12]	GPIO[13]	GPIO[14]	GPIO[3]	VDDALIVE2	P
R	GPIO[5]	GPIO[4]	GPIO[0]	GPIO[1]	GPIO[4]	VDDA920	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND	GPIOI[4]	GPIOI[5]	GPIOI[2]	GPIO[9]	GPIO[6]	R
T	GPIO[2]	GPIO[8]	GPIO[1]	GPIO[2]	VDDA920	GPIO[6]	NC	NC	NC	GND	GND	GND	GND	NC	NC	NC	GND	VDDA940	GPIOI[7]	GPIOI[6]	GPIO[15]	GPIO[7]	T
U	GPIO[7]	GPIO[5]	GPIO[6]	GPIO[4]	GPIO[5]	GND	GND	GND	VDDALIVE2	GND	GND	GPIO[9]	GPIO[0]	GND	GND	GND	GND	VDDOP	GPIOI[13]	GPIOI[12]	GPIOI[0]	GPIO[11]	U
V	GPIO[3]	GPIO[0]	GPIO[3]	nGRESETO	GND	GND	GPIO[9]	SDA	GPIO[14]	GPIO[10]	GPIO[2]	GPIO[12]	GPIO[4]	GPIO[7]	VDDA940	VDDI	GPIO[11]	GND	GPIO[2]	GPIOI[15]	GPIOI[3]	VDDOP	V
W	GPIO[7]	GPIO[2]	GPIO[0]	GND	GND	GND	GPIO[5]	VDDA920	VDDA920	GPIO[5]	VDDI	GPIO[13]	VDDI	GPIO[1]	GPIO[5]	GPIO[14]	GPIO[10]	GND	GPIO[5]	GPIOI[14]	GPIOI[8]	GPIOI[1]	W
Y	GPIO[1]	OM0	TDI	TCK	TMS	GPIO[2]	GPIO[4]	SCL	GPIO[13]	VDDOP	GPIO[15]	VDDOP	GPIO[6]	VDDALIVE2	VDDOP	GPIO[15]	GPIO[9]	GPIO[8]	GPIO[4]	GPIO[3]	GPIOI[11]	GPIOI[9]	Y
AA	TDO	VDDOP	TRST	GPIO[0]	GPIO[4]	EXTCLKIN	GPIO[12]	GPIO[9]	GPIO[8]	GPIO[4]	GPIO[0]	GPIO[10]	GPIO[7]	GPIO[3]	GPIO[5]	GPIO[4]	GPIO[1]	GPIO[0]	GPIO[7]	GPIO[6]	GPIO[1]	GPIOI[10]	AA
AB	GPIO[3]	GPIO[1]	GPIO[6]	GPIO[1]	GPIO[15]	GPIO[11]	GPIO[8]	GPIO[7]	GPIO[3]	GPIO[1]	GPIO[14]	GPIO[11]	GPIO[9]	GPIO[5]	GPIO[2]	GPIO[8]	GPIO[6]	GPIO[3]	GPIO[2]	GPIO[13]	GPIO[12]	GPIO[0]	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 2-2. MP2520F Package FBGA Ball Map

Signal Name	Type	GPIO	Descriptions
Memory Controller Signals			
SDCLK_X	O	-	SDRAM clock
XA[14:0]	O	-	SDRAM address bus. This bus signals the address requested for memory accesses.
XD[15:0]	B	-	SDRAM data bus. XD[15:0] is used for 16-bit data mode.
XD[31:16]	B	-	SDRAM data bus. These data bits are used for 32-bit memory.
SCKEx	O	-	SDRAM clock enable.
nSCSx0	O	-	SDRAM CS for bank 0. This signal should be connected to the chip select (CS) pins for SDRAM.
nSCSx1	O	-	SDRAM CS for bank 1. This signal should be connected to the chip select (CS) pins for SDRAM.
NSRASx	O	-	SDRAM RAS. This signal should be connected to the row address strobe (RAS) pins for all banks of SDRAM.
NSCASx	O	-	SDRAM CAS. This signal should be connected to the column address strobe (CAS) pins for all banks of SDRAM.
NSWEx	O	-	SDRAM write enable. This signal should be connected to the write enables of SDRAM.
SDQMx[3:0]	O	-	SDRAM DQM for data bytes 0 through 3. These signals should be connected to the data output mask enables (DQM) for SDRAM
Display Controller Pins			
VD[23:8]	O	GPIOA[15:0]	Video output data (RGB, Multiplexed-RGB, YCbCr)
VD[7:0]	O	GPIOB[15:8]	Video output data (RGB, Multiplexed-RGB, YCbCr)
CLKH	O	GPIOB[7]	Pixel Clock Output
DE	O	GPIOB[6]	Data Enable
HSYNC	O	GPIOB[5]	Horizontal Sync
VSYNC	O	GPIOB[4]	Vertical Sync
POL	O	GPIOB[3]	Data reverse signal of source driver
CLKV	O	GPIOB[2]	Vertical Clock output
PS	O	GPIOB[1]	Power Save
FG	O	GPIOB[0]	Clock signal of gate driver
XDOFF	O	GPIOH[6]	Gate-OFF Control signal for gate driver
VCLKIN	I	GPIOH[5]	Video Clock Input
STVD	B	GPIOK[7]	Shift clock output for Gate Driver IC

Signal Name	Type	GPIO	Descriptions
STHR	B	GPIOK[3]	Start Pulse of source Driver IC
Image Signal Processor Pins			
ID[15:0]	I	GPIOC[15:0]	Image Capture Data Input
ICLKIN	I	GPIOH[4]	Image Clock In
IHSYNC	B	GPIOH[3]	Image HSYNC
IVSYNC	B	GPIOH[2]	Image VSYNC
ICLKOUT	O	GPIOH[1]	Image Clock Out
UART Pins			
TX0	O	GPIOD[0]	UART0 Transmit Pin
RX0	I	GPIOD[1]	UART0 Receive Pin
nRIO	I	GPIOD[2]	UART1, UART2 Ring Indicator Pin
nDCD	I	GPIOD[3]	UART1, UART2 Data-Carrier-Detect Pin
nDSR	I	GPIOD[4]	UART1, UART2 Data-Set-Ready Pin
nDTR	O	GPIOD[5]	UART1, UART2 Data-Terminal-Ready Pin
nCTS	I	GPIOD[6]	UART1, UART2 Clear-To-Send Pin
nRTS	O	GPIOD[7]	UART1, UART2 Ready-To-Send Pin
TX1	O	GPIOD[8]	UART1 Transmit Pin
RX1	I	GPIOD[9]	UART1 Receive Pin
RX2	I	GPIOD[10]	UART2 Receive Pin
TX2	O	GPIOD[11]	UART2 Transmit Pin
RX3	I	GPIOD[12]	UART3 Receive Pin
TX3	O	GPIOD[13]	UART3 Transmit Pin
SIR **Pins**			
SIR **RX**	I	GPIOD[10]	SIR Receive Pin (SIR Mode)
SIR **TX**	O	GPIOD[11]	SIR Transmit Pin (SIR Mode)
PPM Pin			
PPM	I	GPIOL[13]	PPM Interface Pin
Non DRAM Controller Pins			
CD[15:0]	B	GPIOE[15:0]	Non DRAM Data Bus
CA[25:23](OM[3:1])	O	GPIOF[9:7]	Non DRAM Address Bus

Signal Name	Type	GPIO	Descriptions
CA[22:16]	O	GPIOF[6:0]	Non DRAM Address Bus
CA[15:1]	O	GPIOG[15:1]	Non DRAM Address Bus
CA[0](DQMz[0],BTENB0)	O	GPIOG[0]	Non DRAM Address Bus, Negative byte enable. This signal should be connected to the low byte enable for 16bit SRAM.
nPWAIT	I	GPIOI[13]	Wait Control for PCMCIA /CF/IDE/Static Memory. This signal is an input and is driven low by the PCMCIA/CF/IDE/ Static Memory to extend the length of the transfers to/from applications processor.
nPCS[1]	O	GPIOI[7]	PCMCIA/CF Chip Select, This is used to select PCMCIA card, and enable the low byte lane.
nPCS[0]	O	GPIOI[6]	PCMCIA/CF Chip Select. This is used to select PCMCIA card, and enable the High byte lane.
POE	O	GPIOJ[12]	PCMCIA/CF/SM Output Enable. This signal is an output and performs reads from memory and attribute space.
nPWE	O	GPIOJ[11]	PCMCIA/CF/SM Write Enable. This signal is an output and performs writes to memory and attribute space.
nPIOR	O	GPIOJ[10]	PCMCIA/CF/IDE I/O Read Enable. This signal is an output and performs read transactions from the PCMCIA I/O space.
nPIOW	O	GPIOJ[9]	PCMCIA/CF/IDE I/O Write Enable. This signal is an output and performs write transactions to the PCMCIA I/O space.
PSKSEL	O	GPIOJ[8]	PCMCIA/CF Socket Select. This signal is an output and is used by external steering logic to route control, address and data signals to one of the two PCMCIA sockets.
nPREG	O	GPIOJ[7]	PCMCIA/CF Register Select. This signal is an output and indicates that, on a memory transaction, the target address is attribute space. This signal has the same timing as address.
nPIOIS16	I	GPIOJ[6]	PCMCIA/CF/IDE Select 16bit Access. This signal is an input and is an acknowledgement from the PCMCIA card that the current address is a valid 16 bit wide I/O address.
RDnWR	O	GPIOJ[5]	Buffer Direction Control. Read/Write for static interface. Intended for use as a steering signal for buffering logic.
nBUFOE	O	GPIOJ[4]	Buffer Output Enable Intended for use as a buffer direction control for data bus buffering logic.
nBUFENB	O	GPIOJ[3]	Buffer Enable. Intended for use as a buffer enable for data bus buffering logic.
Static Memory Pins			
DQMz[1] (BTENB1)	O	GPIOI[12]	Negative Byte Enable, This signal should be connected to the high byte enable for 16bit SRAM.
nSCS[3]	O	GPIOI[11]	Static Memory Chip Select. This signal is chip selects to static memory devices such as ROM and Flash
nSCS[2]	O	GPIOI[10]	Static Memory Chip Select. This signal is chip selects to static memory devices such as

Signal Name	Type	GPIO	Descriptions
			ROM and Flash
nSCS[1]	O	GPIOI[9]	Static Memory Chip Select. This signal is chip selects to static memory devices such as ROM and Flash
nSCS[0]	O	GPIOI[8]	Static Memory Chip Select. This is the chip select for the boot memory.
IDE Pins			
nICS[1]	O	GPIOI[5]	IDE Chip Select. This is used to select PCMCIA card, and enable the High byte lane.
nICS[0]	O	GPIOI[4]	IDE Chip Select. This is used to select PCMCIA card, and enable the low byte lane.
Nand Flash Pins			
nNFCE[3]	O	GPIOI[3]	NAND Chip Select. This is chip selects to NAND Flash memory.
nNFCE[2]	O	GPIOI[2]	NAND Chip Select This is chip selects to NAND Flash memory.
nNFCE[1]	O	GPIOI[1]	NAND Chip Select This is chip selects to NAND Flash memory.
nNFCE[0]	O	GPIOI[0]	NAND Chip Select This is chip selects to NAND Flash memory for NAND boot memory.
nPIOW/ALE	O	GPIOJ[9]	NAND ALE. This is address latch enable to NAND Flash memory
nPIOR/CLE	O	GPIOJ[10]	NAND CLE. This is command latch enable to NAND Flash memory
RnB	I	GPIOJ[2]	NAND Ready & Busy. This is Ready/Busy signal of NAND Flash memory.
nNFOE	O	GPIOJ[1]	NAND Output Enable
nNFWE	O	GPIOJ[0]	NAND Write Enable
External DMA Pins			
DREQ[3:0]	I	GPIOK[7:4]	DMA Request. This should be used as IDE DMA Request and Flyby DMA request.
DVAL[3:0]	O	GPIOK[3:0]	DMA Validate. This should be used as Flyby DMA data valid strobes and IDE DMA Acknowledge signal.
PWM Pins			
PWMOUT[3:0]	O	GPIOL[14:11]	Pulse Width Modulation channel
AC97 **Controller Pins**			
ABITCLK	I	GPIOL[10]	AC97 Audio Port bit clock
ADATAIN	I	GPIOL[9]	AC97 Audio Port data in
ASYNC	O	GPIOL[8]	AC97 Audio Port sync signal
nARST	O	GPIOL[7]	AC97 Audio Port reset signal
ADATOUT	O	GPIOL[6]	AC97 Audio Port data out
I^2S Controller Pins			
I^2S CLK	O	GPIOL[10]	I^2S Clock(QCLK_I^2S)

Signal Name	Type	GPIO	Descriptions
I^2S DATAIN	I	GPIOL[9]	I^2S SDATA IN
I^2S SYNC	O	GPIOL[8]	I^2S SYNC
I^2S ACLK	O	GPIOL[7]	I^2S System clock(ACLK_ I^2S)
I^2S DATAOUT	O	GPIOL[6]	I^2S DATA OUT
MMC/SD Controller Pins			
SDICLK	O	GPIOL[5]	MMC/SD Clock
SDICMD	B	GPIOL[4]	MMC/SD Command
SDIDAT[3:0]	B	GPIOL[3:0]	MMC/SD Data
656 Type Video Pins			
VD656[7:0]	B	GPIOM[8:1]	656 Type Video Data
VDCLKIN	B	GPIOM[0]	656 Type Video Clock
Transport Stream I/F Pins			
TSISYNC	I	GPIOM[8]	MPEG I/F Sync
TSIDP	I	GPIOM[7]	MPEG I/F Data Valid
TSIERR	I	GPIOM[6]	MPEG I/F Error
TSIDI0	I	GPIOM[5]	MPEG I/F Data bus (Serial Mode)
TSIDI[7:0]	I	GPIOM[7:0]	MPEG I/F Data bus (Parallel Mode)
TSICLK	I	GPIOM[4]	MPEG I/F Clock
Memory Stick Controller Pins			
MSBS	O	GPIOL[3]	Memory Stick BS
MSDAT	B	GPIOL[2]	Memory Stick SDAT
MSINS	I	GPION[2]	Memory Stick INS
MSCLK	O	GPION[1]	Memory Stick Clock
CDROM Controller Pins			
BCLK	I	GPIOM[7]	CD I/F BCLK
LRCK	I	GPIOM[8]	CD I/F LRCK
SDAT	I	GPIOM[6]	CD I/F SDAT
SPDIF In/Out Pins			
SPDIFIN	I	GPIOO[5]	SPDIF In
SPDIFOUT	O	GPIOO[4]	SPDIF Out

Signal Name	Type	GPIO	Descriptions
SSP Pins			
SSPCLK	O	GPIOO[3]	Synchronous Serial Port Clock
SSPFRM	O	GPIOO[2]	Synchronous Serial Port Frame Signal
SSPTXD	O	GPIOO[1]	Synchronous Serial Port Data
SSPRXD	I	GPIOL[14]	Synchronous Serial Transmit Data
SSPEXTCLKIN	I	GPIOD[12]	Synchronous Serial Port external clock input
One Wire Master Pin			
1WIRE	O	GPIOO[0]	1-wire Master Output
Miscellaneous Pins			
EXTCLKO	O	GPIOH[0]	External Clock Out
OM[3:0]	I	GPIOF[9:7], OM0	Test Mode (External Clock selection)
TEST_EN	I	-	Test Mode Enable
nPORSEL	I	-	POWER On Reset Selection. This signal determines whether the internal POR circuit or nRESET isto be used. If nPORSEL is 0, the internal POR circuit would be used.
nRESET	I	-	Global Reset In. Active low input. nRESET is a level-sensitive input which is used to start the processor from a known address. A LOW level will cause the current instruction to terminate abnormally, and all on-chip state to be reset. When nRESET is driven HIGH, the processor will re-start from address 0.
nGRESETOut	O	-	Global Reset Out
nPWRRGLTOn	O	-	Active Low Power Control stop : 1 run : 0
EXTCLK	I	-	External Clock In
EXTIN0	I	-	Wake-up Control input #0
EXTIN1	I	-	Wake-up Control Input #1
nBATTF	I	-	Battery Fault. Active low input. Signals MP2520F that the main power source is failing (battery is low or is removed from the system.)
Crystal Pins			
XTI	I	-	7.3728Mhz Crystal In
XTO	O	-	7.3728Mhz Crystal Out
XTIRTC	I	-	32.768Khz RTC Crystal input
XTORTC	O	-	32.768Khz RTC Crystal output
JTAG Pins			
TCK	I	-	Clock input for the JTAG Logic

Signal Name	Type	GPIO	Descriptions
nTRST	I	-	Reset input for the JTAG Logic
TDO	O	-	Serial output for test instructions and data for JTAG
TMS	I	-	TMS controls the sequence of the TAP controller's state
TDI	I	-	Serial Data input for JTAG
Dedicated GPIO			
GPIOI[15]	B		GPIO : Dedicated GPIO(CBBUSREQ) ALT2 : 656IN[7]
GPIOI[14]	B		GPIO : Dedicated GPIO(CBBUSGNT) ALT2 : 656IN[6]
GPIOJ[15]	B		GPIO : Dedicated GPIO(CBREQ) ALT2 : 656IN[2]
GPIOJ[14]	B		GPIO : Dedicated GPIO(CBACK) ALT2 : 656IN[1]
GPIOJ[13]	B		GPIO : Dedicated GPIO(CBRDY) ALT2 : 656IN[0]
Power and Ground Pins			
VDDA920	SUP		ARM920T power supply
VDDA940	SUP		ARM940T power supply
VDDADC	SUP		ADC power supply
VDDALIVE1	SUP		Alive1 block power supply
VDDALIVE2	SUP		Alive2 block power supply
VDDAPLL	SUP		APLL power supply
VDDFPLL	SUP		FPLL power supply
VDDUPLL	SUP		UPLL power supply
VDDI	SUP		Internal logic power supply
VDDOP	SUP		I/O power supply
VDDOPALIVE	SUP		SDRAM I/O power supply
VDDRTC	SUP		RTC power supply
VSSADC	SUP		ADC ground
VSSAPLL	SUP		APLL ground
VSSFPLL	SUP		FPLL ground
VSSUPLL	SUP		UPLL ground
VSSRTC	SUP		RTC ground

TABLE 2-1. SIGNAL DESCRIPTIONS FOR MP2520F

GPIO Pins	Alternate Function1/Function2
GPIOA[15:0]	VD[23:8]
GPIOB[15:8]	VD[7:0]
GPIOB[7]	CLKH
GPIOB[6]	DE
GPIOB[5]	HSYNC
GPIOB[4]	VSYNC
GPIOB[3]	POL
GPIOB[2]	CLKV
GPIOB[1]	PS
GPIOB[0]	FG
GPIOC[15:0]	ID[15:0]
GPIOD[0]	TX0
GPIOD[1]	RX0
GPIOD[2]	nRIO
GPIOD[3]	nDCD
GPIOD[4]	nDSR
GPIOD[5]	nDTR
GPIOD[6]	nCTS
GPIOD[7]	nRTS
GPIOD[8]	TX1
GPIOD[9]	RX1
GPIOD[10]	RX2
GPIOD[11]	TX2
GPIOD[12]	RX3/SSPEXTCLKIN
GPIOD[13]	TX3
GPIOE[15:0]	CD[15:0]
GPIOF[9:7]	CA[25:23](OM[3:1])
GPIOF[6:0]	CA[22:16]
GPIOG[15:1]	CA[15:1]
GPIOG[0]	CA[0](DQMz[0], BTENB0)
GPIOH[6]	XDOFF
GPIOH[5]	VCLKIN
GPIOH[4]	ICLKIN
GPIOH[3]	IHSYNC
GPIOH[2]	IVSYNC

GPIO Pins	Alternate Function1/Function2
GPIOH[1]	ICLKOUT
GPIOH[0]	EXTCLKO
GPIOI[15]	Dedicated GPIO(CBBUSREQ)/ /656IN[7]
GPIOI[14]	Dedicated GPIO(CBBUSGNT)/ /656IN[6]
GPIOI[13]	nPWAIT
GPIOI[12]	DQMz[1] (BTENB1)
GPIOI[11]	nSCS[3]
GPIOI[10]	nSCS[2]
GPIOI[9]	nSCS[1]
GPIOI[8]	nSCS[0]
GPIOI[7]	nPCS[1]
GPIOI[6]	nPCS[0]
GPIOI[5]	nICS[1]
GPIOI[4]	nICS[0]
GPIOI[3]	nNFCE[3]/656IN[5]
GPIOI[2]	nNFCE[2]/656IN[4]
GPIOI[1]	nNFCE[1]/656IN[3]
GPIOI[0]	nNFCE[0]
GPIOJ[15]	Dedicated GPIO (CBREQ)/ /656IN[2]
GPIOJ[14]	Dedicated GPIO (CBACK)/ /656IN[1]
GPIOJ[13]	Dedicated GPIO (CBRDY)/ /656IN[0]
GPIOJ[12]	NPOE
GPIOJ[11]	NPWE
GPIOJ[10]	NPIOR
GPIOJ[9]	NPIOW
GPIOJ[8]	PSKSEL
GPIOJ[7]	NPREG
GPIOJ[6]	nPIOIS16
GPIOJ[5]	RDnWR
GPIOJ[4]	NBUFOE
GPIOJ[3]	nBUFENB
GPIOJ[2]	RnB
GPIOJ[1]	NNFOE
GPIOJ[0]	NNFWE
GPIOK[7]	DREQ3/STVD
GPIOK[6]	DREQ2
GPIOK[5]	DREQ1
GPIOK[4]	DREQ0

GPIO Pins	Alternate Function1/Function2
GPIOK[3]	DVAL3/STHR
GPIOK[2]	DVAL2/V656CLK
GPIOK[1]	DVAL1
GPIOK[0]	DVAL0
GPIOL[14]	PWMOUT3/SSPRXD
GPIOL[13]	PWMOUT2/PPM
GPIOL[12]	PWMOUT1
GPIOL[11]	PWMOUT0
GPIOL[10]	ABITCLK/ I^2S CLK
GPIOL[9]	ADATAIN/ I^2S DATAIN
GPIOL[8]	ASYNC/ I^2S SYNC
GPIOL[7]	nARST/ I^2S ACLK
GPIOL[6]	ADATOUT/ I^2S DATAOUT
GPIOL[5]	SDICLK
GPIOL[4]	SDICMD
GPIOL[3]	SDIDAT[3]/MSBS
GPIOL[2]	SDIDAT[2]/MSDAT
GPIOL[1]	SDIDAT[1]
GPIOL[0]	SDIDAT[0]
GPIOM[8]	VD656[7]/TSISYNC (LRCK)
GPIOM[7]	VD656[6]/TSIDP (BCLK)
GPIOM[6]	VD656[5]/TSIERR (SDAT)
GPIOM[5]	VD656[4]/TSIDI0
GPIOM[4]	VD656[3]/TSICLK
GPIOM[3]	VD656[2]
GPIOM[2]	VD656[1]
GPIOM[1]	VD656[0]
GPIOM[0]	VDCLKIN
GPION[7]	TSIDI[7]/TSISYNC
GPION[6]	TSIDI[6]/TSIDP
GPION[5]	TSIDI[5]/TSIERR (LRCK)
GPION[4]	TSIDI[4]/TSIDI0 (BCK)
GPION[3]	TSIDI[3]/TSICLK (SDAT)
GPION[2]	TSIDI[2]/MSINS
GPION[1]	TSIDI[1]/MSCLK
GPION[0]	TSIDI[0]
GPIOO[5]	SPDIFIN

GPIO Pins	Alternate Function1/Function2
GPIOO[4]	SPDIFOUT
GPIOO[3]	SSPCLK
GPIOO[2]	SSPFRM
GPIOO[1]	SSPTXD
GPIOO[0]	1WIRE

TABLE 2-2. MP2520F GPIO PIN MAP

2.3 MP2520F I/O PIN LISTING

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
A1	**VDDADC**	SUP				
A2	**VDDOP**	SUP				
A3	**DP1**	IAOA	DP1	DP1	-	-
A4	**GPIOO[4]/SPDIFOUT**	ISOSZP	GPIOO[4]	GPIOO[4]	SPDIFOUT	-
A5	**GPIOO[5]/SPDIFIN**	ISOSZP	GPIOO[5]	GPIOO[5]	SPDIFIN	
A6	**GPIOD[5]/nDTR**	ISOSZP	GPIOD[5]	GPIOD[5]	nDTR	-
A7	**GPIOD[7]/nRTS**	ISOSZP	GPIOD[7]	GPIOD[7]	nRTS	-
A8	**nRESET**	IS	nRESET	nRESET	-	-
A9	**nPORSEL**	IS	nPORSEL	nPORSEL	-	-
A10	**XA[1]**	OS	XA[1]	XA[1]	-	-
A11	**XA[4]**	OS	XA[4]	XA[4]	-	-
A12	**XA[9]**	OS	XA[9]	XA[9]	-	-
A13	**XD[31]**	ISOS	XD[31]	XD[31]	-	-
A14	**XD[29]**	ISOS	XD[29]	XD[29]	-	-
A15	**XD[27]**	ISOS	XD[27]	XD[27]	-	-
A16	**XD[25]**	ISOS	XD[25]	XD[25]	-	-
A17	**XD[23]**	ISOS	XD[23]	XD[23]	-	-
A18	**XD[21]**	ISOS	XD[21]	XD[21]	-	-
A19	**XD[19]**	ISOS	XD[19]	XD[19]	-	-
A20	**XD[17]**	ISOS	XD[17]	XD[17]	-	-
A21	**GND**	SUP				
A22	**GND**	SUP				
B1	**VDDAPLL**	SUP				
B2	**ADCIN1**	IA	ADCIN1	ADCIN1	-	-
B3	**ADCIN3**	IA	ADCIN3	ADCIN3	-	-
B4	**ADCIN4**	IA	ADCIN4	ADCIN4	-	-
B5	**DP0**	IAOA	DP0	DP0	-	-
B6	**GPIOD[1]/RX0**	ISOSZP	GPIOD[1]	GPIOD[1]	RX0	-
B7	**GPIOD[6]/nCTS**	ISOSZP	GPIOD[6]	GPIOD[6]	nCTS	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
B8	**GPIOD[9]/RX1**	ISOSZP	GPIOD[9]	GPIOD[9]	RX1	-
B9	**GPIOD[10]/RX2**	ISOSZP	GPIOD[10]	GPIOD[10]	RX2	-
B10	**SDCLK**	OS	SDCLK	SDCLK	-	-
B11	**XA[0]**	OS	XA[0]	XA[0]	-	-
B12	**XA[5]**	OS	XA[5]	XA[5]	-	-
B13	**XD[30]**	ISOS	XD[30]	XD[30]	-	-
B14	**XD[28]**	ISOS	XD[28]	XD[28]	-	-
B15	**XD[26]**	ISOS	XD[26]	XD[26]	-	-
B16	**XD[24]**	ISOS	XD[24]	XD[24]	-	-
B17	**XD[22]**	ISOS	XD[22]	XD[22]	-	-
B18	**XD[20]**	ISOS	XD[20]	XD[20]	-	-
B19	**XD[18]**	ISOS	XD[18]	XD[18]	-	-
B20	**XD[16]**	ISOS	XD[16]	XD[16]	-	-
B21	**XD[15]**	ISOS	XD[15]	XD[15]	-	-
B22	**XD[14]**	ISOS	XD[14]	XD[14]	-	-
C1	**XTIRTC**	IS	XTIRTC	XTIRTC	-	-
C2	**XTORTC**	OS	XTORTC	XTORTC	-	-
C3	**VSSADC**	SUP				
C4	**ADCIN0**	IA	ADCIN0	ADCIN0	-	-
C5	**ADCIN2**	IA	ADCIN2	ADCIN2	-	-
C6	**DN0**	IAOA	DN0	DN0	-	-
C7	**DP2**	IAOA	DP2	DP2	-	-
C8	**VDDALIVE2**	SUP				
C9	**VDDOP**	SUP				
C10	**GPIOD[11]/TX2**	ISOSZP	GPIOD[11]	GPIOD[11]	TX2	-
C11	**nBATTF**	IS	nBATTF	nBATTF	-	-
C12	**XA[2]**	OS	XA[2]	XA[2]	-	-
C13	**XA[6]**	OS	XA[6]	XA[6]	-	-
C14	**XA[8]**	OS	XA[8]	XA[8]	-	-
C15	**XBA[1]**	OS	XBA[1]	XBA[1]	-	-
C16	**VDDOPALIVE**	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
C17	**GND**	SUP				
C18	**GND**	SUP				
C19	**GND**	SUP				
C20	**GND**	SUP				
C21	**XD[13]**	ISOS	XD[13]	XD[13]	-	-
C22	**XD[12]**	ISOS	XD[12]	XD[12]	-	-
D1	**XTI**	IS	XTI	XTI	-	-
D2	**XTO**	OS	XTO	XTO	-	-
D3	**VDDUPLL**	SUP				
D4	**VSSAPLL**					
D5	**ADCIN5**	IA	ADCIN5	ADCIN5	-	-
D6	**DN1**	IAOA	DN1	DN1	-	-
D7	**VDDOP**	SUP				
D8	**GPIOD[2]/nRIO**	ISOSZP	GPIOD[2]	GPIOD[2]	nRIO	-
D9	**VDDI**	SUP				
D10	**GPIOD[13]/TX3**	ISOSZP	GPIOD[13]	GPIOD[13]	TX3	-
D11	**EXTIN0**	IS	EXTIN0	EXTIN0	-	-
D12	**XA[3]**	OS	XA[3]	XA[3]	-	-
D13	**XA[7]**	OS	XA[7]	XA[7]	-	-
D14	**XA[10]**	OS	XA[10]	XA[10]	-	-
D15	**XBA[0]**	OS	XBA[0]	XBA[0]	-	-
D16	**VDDOPALIVE**	SUP				
D17	**GND**	SUP				
D18	**GND**	SUP				
D19	**GND**	SUP				
D20	**GND**	SUP				
D21	**XD[11]**	ISOS	XD[11]	XD[11]	-	-
D22	**XD[10]**	ISOS	XD[10]	XD[10]	-	-
E1	**GPIOA[9]/VD[17]**	ISOSZP	GPIOA[9]	GPIOA[9]	VD[17]	-
E2	**GPIOA[14]/VD[22]**	ISOSZP	GPIOA[14]	GPIOA[14]	VD[17]	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
E3	**VDDFPLL**	SUP				
E4	**VSSUPLL**	SUP				
E5	**GND**	SUP				
E6	**VREF**	IA	VREF	VREF	-	-
E7	**DN2**	IAOA	DN2	DN2	-	-
E8	**VDDI**	SUP				
E9	**GPIOD[3]/nDCD**	ISOSZP	GPIOD[3]	GPIOD[3]	nDCD	-
E10	**GPIOD[8]/TX1**	ISOSZP	GPIOD[8]	GPIOD[8]	TX1	-
E11	**VDDI**	SUP				
E12	**EXTIN1**	IS	EXTIN1	EXTIN1	-	-
E13	**VDDALIVE1**	SUP				
E14	**XA[11]**	OS	XA[11]	XA[11]	-	-
E15	**XA[12]**	OS	XA[12]	XA[12]	-	-
E16	**GND**	SUP				
E17	**GND**	SUP				
E18	**GND**	SUP				
E19	**GND**	SUP				
E20	**VDDOPALIVE**	SUP				
E21	**XD[9]**	ISOS	XD[9]	XD[9]	-	-
E22	**XD[8]**	ISOS	XD[8]	XD[8]	-	-
F1	**GPIOA[7]/VD[15]**	ISOSZP	GPIOA[7]	GPIOA[7]	VD[15]	-
F2	**GPIOA[11]/VD[19]**	ISOSZP	GPIOA[11]	GPIOA[11]	VD[19]	-
F3	**VDDRTC**	SUP				
F4	**VSSRTC**					
F5	**VSSFPLL**	SUP				
F6	**GND**	SUP				
F7	**GND**	SUP				
F8	**GPIOD[0]/TX0**	ISOSZP	GPIOD[0]	GPIOD[0]	TX0	-
F9	**GPIOD[4]/nDSR**	ISOSZP	GPIOD[4]	GPIOD[4]	nDSR	-
F10	**GPIOH[0]/EXTCLKO**	ISOSZP	GPIOH[0]	GPIOH[0]	EXTCLKO	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
F11	**VDDI**	SUP				
F12	**nPWRRGLTON**	OS	nPWRRGLT On	nPWRRGLTO n	-	-
F13	**VDDOPALIVE**	SUP				
F14	**GND**	SUP				
F15	**GND**	SUP				
F16	**GND**	SUP				
F17	**GND**	SUP				
F18	**GND**	SUP				
F19	**GND**	SUP				
F20	**VDDOPALIVE**	SUP				
F21	**XD[7]**	ISOS	XD[7]	XD[7]	-	-
F22	**XD[6]**	ISOS	XD[6]	XD[6]	-	-
G1	**GPIOA[3]/VD[11]**	ISOSZP	GPIOA[3]	GPIOA[3]	VD[11]	-
G2	**GPIOA[8]/VD[16]**	ISOSZP	GPIOA[8]	GPIOA[8]	VD[16]	-
G3	**GPIOA[12]/VD[20]**	ISOSZP	GPIOA[12]	GPIOA[12]	VD[20]	-
G4	**GPIOA[13]/VD[21]**	ISOSZP	GPIOA[13]	GPIOA[13]	VD[21]	-
G5	**VDDOP**	SUP				
G6	**GPIOA[15]/VD[23]**	ISOSZP	GPIOA[15]	GPIOA[15]	VD[23]	-
G10	**GND**	SUP				
G11	**GPIOD[12]/RX3/SSPEXTCLKIN**	ISOSZP	GPIOD[12]	GPIOD[12]	RX3	SSPEXT CLKIN
G12	**TEST_EN**	IS	TEST_EN	TEST_EN	-	-
G13	**VDDOPALIVE**	SUP				
G17	**GND**	SUP				
G18	**GND**	SUP				
G19	**SCKEX**	OS	SCKEx	SCKEx	-	-
G20	**VDDALIVE1**	SUP				
G21	**XD[5]**	ISOS	XD[5]	XD[5]	-	-
G22	**XD[4]**	ISOS	XD[4]	XD[4]	-	-
H1	**GPIOA[0]/VD[8]**	ISOSZP	GPIOA[0]	GPIOA[0]	VD[8]	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
H2	**GPIOA[4]/VD[12]**	ISOSZP	GPIOA[4]	GPIOA[4]	VD[12]	-
H3	**GPIOA[6]/VD[14]**	ISOSZP	GPIOA[6]	GPIOA[6]	VD[14]	-
H4	**VDDI**	SUP				
H5	**GPIOA[10]/VD[18]**	ISOSZP	GPIOA[10]	GPIOA[10]	VD[18]	-
H6	**GND**	SUP				
H17	**GND**	SUP				
H18	**nSCSX1**	OS	nSCSX1	nSCSX1	-	-
H19	**nSCSX0**	OS	nSCSX0	nSCSX0	-	-
H20	**VDDOPALIVE**	SUP				
H21	**XD[3]**	ISOS	XD[3]	XD[3]	-	-
H22	**XD[2]**	ISOS	XD[2]	XD[2]	-	-
J1	**GPIOB[14]/VD[6]**	ISOSZP	GPIOB[14]	GPIOB[14]	VD[6]	-
J2	**GPIOB[15]/VD[7]**	ISOSZP	GPIOB[15]	GPIOB[15]	VD[7]	-
J3	**VDDOP**	SUP				
J4	**GPIOA[2]/VD[10]**	ISOSZP	GPIOA[2]	GPIOA[2]	VD[10]	-
J5	**GPIOA[5]/VD[13]**	ISOSZP	GPIOA[5]	GPIOA[5]	VD[13]	-
J6	**GND**	SUP				
J17	**GND**	SUP				
J18	**nSWEX**	OS	nSWEx	nSWEx	-	-
J19	**nSRASX**	OS	nSRASx	nSRASx	-	-
J20	**nSCASX**	OS	nSCASx	nSCASx	-	-
J21	**XD[1]**	ISOS	XD[1]	XD[1]	-	-
J22	**XD[0]**	ISOS	XD[0]	XD[0]	-	-
K1	**GPIOB[8]/VD[0]**	ISOSZP	GPIOB[8]	GPIOB[8]	VD[0]	-
K2	**GPIOB[11]/VD[3]**	ISOSZP	GPIOB[11]	GPIOB[11]	VD[3]	-
K3	**GPIOB[12]/VD[4]**	ISOSZP	GPIOB[12]	GPIOB[12]	VD[4]	-
K4	**GPIOB[13]/VD[5]**	ISOSZP	GPIOB[13]	GPIOB[13]	VD[5]	-
K5	**GPIOB[10]/VD[2]**	ISOSZP	GPIOB[10]	GPIOB[10]	VD[2]	-
K6	**GPIOA[1]/VD[9]**	ISOSZP	GPIOA[1]	GPIOA[1]	VD[9]	-
K7	**GND**	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
K16	**GND**	SUP				
K17	**GND**	SUP				
K18	**SDQMX0**	OS	SDQMx0	SDQMx0	-	-
K19	**VDDI**	SUP				
K20	**SDQMX3**	OS	SDQMx3	SDQMx3	-	-
K21	**SDQMX1**	OS	SDQMx1	SDQMx1	-	-
K22	**SDQMX2**	OS	SDQMx2	SDQMx2	-	-
L1	**GPIOB[7]/CLKH**	ISOSZP	GPIOB[7]	GPIOB[7]	CLKH	-
L2	**GPIOB[4]/VSYNC**	ISOSZP	GPIOB[4]	GPIOB[4]	VSYNC	-
L3	**GPIOB[6]/DE**	ISOSZP	GPIOB[6]	GPIOB[6]	DE	-
L4	**GPIOB[5]/HSYNC**	ISOSZP	GPIOB[5]	GPIOB[5]	HSYNC	-
L5	**GPIOB[9]/VD[1]**	ISOSZP	GPIOB[9]	GPIOB[9]	VD[1]	-
L6	**VDDI**	SUP				
L7	**GND**	SUP				
L16	**GND**	SUP				
L17	**GND**	SUP				
L18	**GPIOK[5]/DREQ1**	ISOSZP	GPIOK[5]	GPIOK[5]	DREQ1	-
L19	**GPIOK[1]/DVAL1**	ISOSZP	GPIOK[1]	GPIOK[1]	DVAL1	-
L20	**GPIOK[2]/DVAL2/V656CLK**	ISOSZP	GPIOK[2]	GPIOK[2]	DVAL2	V656CLK
L21	**GPIOK[3]/ DVAL3/STHR**	ISOSZP	GPIOK[3]	GPIOK[3]	DVAL3	STHR
L22	**GPIOK[0]/ DVAL0**	ISOSZP	GPIOK[0]	GPIOK[0]	DVAL0	-
M1	**GPIOB[2]/CLKV**	ISOSZP	GPIOB[2]	GPIOB[2]	CLKV	-
M2	**GPIOB[0]/FG**	ISOSZP	GPIOB[0]	GPIOB[0]	FG	-
M3	**GPIOB[1]/PS**	ISOSZP	GPIOB[1]	GPIOB[1]	PS	-
M4	**VDDALIVE2**	SUP				
M5	**VDDOP**	SUP				
M6	**GPIOB[3]/POL**	ISOSZP	GPIOB[3]	GPIOB[3]	POL	-
M7	**GND**	SUP				
M16	**GND**	SUP				
M17	**GPIOJ[0]/nNFWE**	ISOSZP	GPIOJ[0]	GPIOJ[0]	nNFWE	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
M18	**GPIOJ[4]/nBUFOE**	ISOSZP	GPIOJ[4]	GPIOJ[4]	nBUFOE	-
M19	**GPIOJ[1]/nNFOE**	ISOSZP	GPIOJ[1]	GPIOJ[1]	nNFOE	-
M20	**VDDOP**	SUP				
M21	**GPIOK[7]/DREQ3/STVD**	ISOSZP	GPIOK[7]	GPIOK[7]	DREQ3	STVD
M22	**GPIOK[4]/DREQ0**	ISOSZP	GPIOK[4]	GPIOK[4]	DREQ0	-
N1	**GPIOL[14]/PWMOUT3/SSPRXD**	ISOSZP	GPIOL[14]	GPIOL[14]	PWMOUT3	SSPRXD
N2	**GPIOL[13]/PWMOUT2/PPM**	ISOSZP	GPIOL[13]	GPIOL[13]	PWMOUT2	PPM
N3	**GPIOL[10]/ABITCLK/ I^2S CLK**	ISOSZP	GPIOL[10]	GPIOL[10]	ABITCLK	-
N4	**GPIOL[11]/PWMOUT0**	ISOSZP	GPIOL[11]	GPIOL[11]	PWMOUT0	-
N5	**GPIOL[12]/PWMOUT1**	ISOSZP	GPIOL[12]	GPIOL[12]	PWMOUT1	-
N6	**GPIOL[7]/nARST/ I^2S ACLK**	ISOSZP	GPIOL[7]	GPIOL[7]	nARST	-
N7	**GND**	SUP				
N16	**GND**	SUP				
N17	**GPIOJ[10]/nPIOR**	ISOSZP	GPIOJ[10]	GPIOJ[10]	nPIOR	-
N18	**GPIOJ[8]/PSKSEL**	ISOSZP	GPIOJ[8]	GPIOJ[8]	PSKSEL	-
N19	**GPIOJ[5]/RDNWR**	ISOSZP	GPIOJ[5]	GPIOJ[5]	RDNWR	-
N20	**VDDI**	SU				
N21	**GPIOJ[2]/RNB**	ISOSZP	GPIOJ[2]	GPIOJ[2]	RnB	-
N22	**GPIOK[6]/DREQ2**	ISOSZP	GPIOK[6]	GPIOK[6]	DREQ2	-
P1	**GPIOL[9]/ADATAIN/ I^2S DATAIN**	ISOSZP	GPIOL[9]	GPIOL[9]	ADATAIN	-
P2	**GPIOL[8]/ASYNC/ I^2S SYNC**	ISOSZP	GPIOL[8]	GPIOL[8]	ASYNC	-
P3	**GPIOL[5]/SDICLK**	ISOSZP	GPIOL[5]	GPIOL[5]	SDICLK	-
P4	**VDDI**	SUP				
P5	**GPIOL[3]/SDIDAT[3]/MSBS**	ISOSZP	GPIOL[3]	GPIOL[3]	SDIDAT[3]	MSBS
P6	**GND**	SUP				
P17	**VDDI**	SUP				
P18	**GPIOJ[12]/nPOE**	ISOSZP	GPIOJ[12]	GPIOJ[12]	nPOE	-
P19	**GPIOJ[13](CBRDY)/ /656IN[0]**	ISOSZP	GPIOJ[13]	GPIOJ[13] (CBRDY)		656IN[0]
P20	**GPIOJ[14](CBACK)/ /656IN[1]**	ISOSZP	GPIOJ[14]	GPIOJ[14] (CBACK)		656IN[1]

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
P21	**GPIOJ[3]/nBUFENB**	ISOSZP	GPIOJ[3]	GPIOJ[3]	nBUFENB	-
P22	**VDDALIE2**	SUP				
R1	**GPIOL[6]/ADATOUT/ I^2S DATAOUT**	ISOSZP	GPIOL[6]	GPIOL[6]	ADATOUT	-
R2	**GPIOL[4]/SDICMD**	ISOSZP	GPIOL[4]	GPIOL[4]	SDICMD	-
R3	**GPIOL[0]/SDIDAT[0]**	ISOSZP	GPIOL[0]	GPIOL[0]	SDIDAT[0]	-
R4	**GPIOL[1]/SDIDAT[1]**	ISOSZP	GPIOL[1]	GPIOL[1]	SDIDAT[1]	-
R5	**GPIOM[4]/VD656[3]/TSICLK**	ISOSZP	GPIOM[4]	GPIOM[4]	VD656[3]	TSICLK
R6	**VDDA920**	SUP				
R17	**GND**	SUP				
R18	**GPIOI[4]/nICS[0]**	ISOSZP	GPIOI[4]	GPIOI[4]	nICS[0]	-
R19	**GPIOI[5]/nICS[1]**	ISOSZP	GPIOI[5]	GPIOI[5]	nICS[1]	-
R20	**GPIOI[2]/nNFCE[2]/656IN[4]**	ISOSZP	GPIOI[2]	GPIOI[2]	nNFCE[2]	656IN[4]
R21	**GPIOJ[9]/nPIOW**	ISOSZP	GPIOJ[9]	GPIOJ[9]	nPIOW	-
R22	**GPIOJ[6]/nPIOIS16**	ISOSZP	GPIOJ[6]	GPIOJ[6]	nPIOIS16	-
T1	**GPIOL[2]/SDIDAT[2]/MSDAT**	ISOSZP	GPIOL[2]	GPIOL[2]	SDIDAT[2]	MSDAT
T2	**GPIOM[8]/VD656[7]/TSISYNC(LRCK)**	ISOSZP	GPIOM[8]	GPIOM[8]	VD656[7]	TSISYNC (LRCK)
T3	**GPIOM[1]/VD656[0]**	ISOSZP	GPIOM[1]	GPIOM[1]	VD656[0]	-
T4	**GPIOM[2]/VD656[1]**	ISOSZP	GPIOM[2]	GPIOM[2]	VD656[1]	-
T5	**VDDA920**	SUP				
T6	**GPIOM[6]/VD656[5]/TSIERR(SDAT)**	ISOSZP	GPIOM[6]	GPIOM[6]	VD656[5]	TSIERR (SDAT)
T10	**GND**	SUP				
T11	**GND**	SUP				
T12	**GND**	SUP				
T13	**GND**	SUP				
T17	**GND**	SUP				
T18	**VDDA940**	SUP				
T19	**GPIOI[7]/nPCS[1]**	ISOSZP	GPIOI[7]	GPIOI[7]	nPCS[1]	-
T20	**GPIOI[6]/nPCS[0]**	ISOSZP	GPIOI[6]	GPIOI[6]	nPCS[0]	-
T21	**GPIOJ[15] (CBREQ)/ /656IN[2]**	ISOSZP	GPIOJ[15]	GPIOJ[15]		656IN[2]

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
				(CBREQ)		
T22	**GPIOJ[7]/nPREG**	ISOSZP	GPIOJ[7]	GPIOJ[7]	nPREG	-
U1	**GPIOM[7]/VD656[6]/TSIDP (BCLK)**	ISOSZP	GPIOM[7]	GPIOM[7]	VD656[6]	TSIDP (BCLK)
U2	**GPIOM[5]/VD656[4]/TSIDI0**	ISOSZP	GPIOM[5]	GPIOM[5]	VD656[4]	TSIDI0
U3	**GPION[6]/TSIDI[6]/TSIDP**	ISOSZP	GPION[6]	GPION[6]	TSIDI[6]	TSIDP
U4	**GPION[4]/TSIDI[4]/TSIDI0 (BCLK)**	ISOSZP	GPION[4]	GPION[4]	TSIDI[4]	TSIDI0 (BCLK)
U5	**GPION[5]/TSIDI[5]/TSIERR (LRCK)**	ISOSZP	GPION[5]	GPION[5]	TSIDI[5]	TSIERR (LRCK)
U6	**GND**	SUP				
U7	**GND**	SUP				
U8	**GND**	SUP				
U9	**VDDALIVE2**	SUP				
U10	**GND**	SUP				
U11	**GND**	SUP				
U12	**GPIOE[8]/ZD[8]**	ISOSZP	GPIOE[8]	GPIOE[8]	CD[8]	-
U13	**GPIOE[0]/ZD[0]**	ISOSZP	GPIOE[0]	GPIOE[0]	CD[0]	-
U14	**GND**	SUP				
U15	**GND**	SUP				
U16	**GND**	SUP				
U17	**GND**	SUP				
U18	**VDDOP**	SUP				
U19	**GPIOI[13]/nPWAIT**	ISOSZP	GPIOI[13]	GPIOI[13]	nPWAIT	-
U20	**GPIOI[12]/DQMZ1(BTENB1)**	ISOSZP	GPIOI[12]	GPIOI[12]	DQMZ1 (BTENB1)	-
U21	**GPIOI[0]/nNFCE[0]**	ISOSZP	GPIOI[0]	GPIOI[0]	nNFCE[0]	-
U22	**GPIOJ[11]/nPWE**	ISOSZP	GPIOJ[11]	GPIOJ[11]	nPWE	-
V1	**GPIOM[3]/VD656[2]**	ISOSZP	GPIOM[3]	GPIOM[3]	VD656[2]	-
V2	**GPIOM[0]/VDCLKIN**	ISOSZP	GPIOM[0]	GPIOM[0]	VDCLKIN	-
V3	**GPION[3]/TSIDI[3]/TSICLK (SDAT)**	ISOSZP	GPION[3]	GPION[3]	TSIDI[3]	TSICLK (SDAT)

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
V4	**nGRESETOut**	OS	nGRESETOut	nGRESETOut	-	-
V5	**GND**	SUP				
V6	**GND**	SUP				
V18	**GND**	SUP				
V7	**GPIOH[3]/IHSYNC**	ISOSZP	GPIOH[3]	GPIOH[3]	IHSYNC	-
V8	**SDA**	OD	SDA	SDA	-	-
V9	**GPIOC[14]/ID[14]**	ISOSZP	GPIOC[14]	GPIOC[14]	ID[14]	-
V10	**GPIOC[10]/ID[10]**	ISOSZP	GPIOC[10]	GPIOC[10]	ID[10]	-
V11	**GPIOC[2]/ID[2]**	ISOSZP	GPIOC[2]	GPIOC[2]	ID[2]	-
V12	**GPIOE[12]/ZD[12]**	ISOSZP	GPIOE[12]	GPIOE[12]	CD[12]	-
V13	**GPIOE[4]/ZD[4]**	ISOSZP	GPIOE[4]	GPIOE[4]	CD[4]	-
V14	**GPIOF[7]/ZA[23]/OM[1]**	ISOSZP	GPIOF[7]	GPIOF[7]	CA[23]	OM[1]
V15	**VDDA940**	SUP				
V16	**VDDI**	SUP				
V17	**GPIOG[11]/ZA[11]**	ISOSZP	GPIOG[11]	GPIOG[11]	CA[11]	-
V19	**GPIOG[2]/ZA[2]**	ISOSZP	GPIOG[2]	GPIOG[2]	CA[2]	-
V20	**GPIOI[15] (CBBUSREQ)/ /656IN[7]**	ISOSZP	GPIOI[15]	GPIOI[15] (CBBUSREQ)		656IN[7]
V21	**GPIOI[3]/nNFCE[3]/656IN[5]**	ISOSZP	GPIOI[3]	GPIOI[3]	nNFCE[3]	656IN[5]
V22	**VDDOP**	SUP				
W1	**GPION[7]/TSIDI[7]/TSISYNC**	ISOSZP	GPION[7]	GPION[7]	TSIDI[7]	TSISYNC
W2	**GPION[2]/TSIDI[2]/MSINS**	ISOSZP	GPION[2]	GPION[2]	TSIDI[2]	MSINS
W3	**GPION[0]/TSIDI[0]**	ISOSZP	GPION[0]	GPION[0]	TSIDI[0]	-
W4	**GND**	SUP				
W5	**GND**	SUP				
W6	**GND**	SUP				
W7	**GPIOH[5]/VCLKIN**	ISOSZP	GPIOH[5]	GPIOH[5]	VCLKIN	-
W8	**VDDA920**	SUP				
W9	**VDDA920**	SUP				
W10	**GPIOC[5]/ID[5]**	ISOSZP	GPIOC[5]	GPIOC[5]	ID[5]	-
W11	**VDDI**	SUP				

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
W12	**GPIOE[13]/ZD[13]**	ISOSZP	GPIOE[13]	GPIOE[13]	CD[13]	-
W13	**VDDI**	SUP				
W14	**GPIOE[1]/ZD[1]**	ISOSZP	GPIOE[1]	GPIOE[1]	CD[1]	-
W15	**GPIOF[5]/ZA[21]**	ISOSZP	GPIOF[5]	GPIOF[5]	CA[21]	-
W16	**GPIOG[14]/ZA[14]**	ISOSZP	GPIOG[14]	GPIOG[14]	CA[14]	-
W17	**GPIOG[10]/ZA[10]**	ISOSZP	GPIOG[10]	GPIOG[10]	CA[10]	-
W18	**GND**	SUP				
W19	**GPIOG[5]/ZA[5]**	ISOSZP	GPIOG[5]	GPIOG[5]	CA[5]	-
W20	**GPIOI[14] (CBBUSGNT)/ /656IN[6]**	ISOSZP	GPIOI[14]	GPIOI[14] (CBBUSGNT)		656IN[6]
W21	**GPIOI[8]/nSCS[0]**	ISOSZP	GPIOI[8]	GPIOI[8]	nSCS[0]	-
W22	**GPIOI[1]/nNFCE[1]/656IN[3]**	ISOSZP	GPIOI[1]	GPIOI[1]	nNFCE[1]	656IN[3]
Y1	**GPION[1]/TSIDI[1]/MSCLK**	ISOSZP	GPION[1]	GPION[1]	TSIDI[1]	MSCLK
Y2	**OM0**	OS	OM0	OM0	-	-
Y3	**TDI**	IS	TDI	TDI	-	-
Y4	**TCK**	IS	TCK	TCK	-	-
Y5	**TMS**	IS	TMS	TMS	-	-
Y6	**GPIOO[2]/SSPFRM**	ISOSZP	GPIOO[2]	GPIOO[2]	SSPFRM	-
Y7	**GPIOH[4]/ICLKIN**	ISOSZP	GPIOH[4]	GPIOH[4]	ICLKIN	
Y8	**SCL**	OD	SCL	SCL	-	-
Y9	**GPIOC[13]/ID[13]**	ISOSZP	GPIOC[13]	GPIOC[13]	ID[13]	-
Y10	**VDDOP**	SUP				
Y11	**GPIOE[15]/ZD[15]**	ISOSZP	GPIOE[15]	GPIOE[15]	CD[15]	-
Y12	**VDDOP**	SUP				
Y13	**GPIOE[6]/ZD[6]**	ISOSZP	GPIOE[6]	GPIOE[6]	CD[6]	-
Y14	**VDDALIVE2**	SUP				
Y15	**VDDOP**	SUP				
Y16	**GPIOG[15]/ZA[15]**	ISOSZP	**GPIOG[15]**	**GPIOG[15]**	CA[15]	-
Y17	**GPIOG[9]/ZA[9]**	ISOSZP	GPIOG[9]	GPIOG[9]	CA[9]	-
Y18	**GPIOG[8]/ZA[8]**	ISOSZP	GPIOG[8]	GPIOG[8]	CA[8]	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
Y19	**GPIOG[4]/ZA[4]**	ISOSZP	GPIOG[4]	GPIOG[4]	CA[4]	-
Y20	**GPIOG[3]/ZA[3]**	ISOSZP	GPIOG[3]	GPIOG[3]	CA[3]	-
Y21	**GPIOI[11]/nSCS[3]**	ISOSZP	GPIOI[11]	GPIOI[11]	nSCS[3]	-
Y22	**GPIOI[9]/nSCS[1]**	ISOSZP	GPIOI[9]	GPIOI[9]	nSCS[1]	-
AA1	**TDO**	OSZ	TDO	TDO	-	-
AA2	**VDDOP**	SUP				
AA3	**NTRST**	IS	nTRST	nTRST	-	-
AA4	**GPIOO[0]/1WIRE**	OD	GPIOO[0]	GPIOO[0]	1WIRE	-
AA5	**GPIOH[2]/IVSYNC**	ISOSZP	GPIOH[2]	GPIOH[2]	IVSYNC	-
AA6	**EXTCLKIN**	IS	**EXTCLKIN**	**EXTCLKIN**		-
AA7	**GPIOC[12]/ID[12]**	ISOSZP	GPIOC[12]	GPIOC[12]	ID[12]	-
AA8	**GPIOC[9]/ID[9]**	ISOSZP	GPIOC[9]	GPIOC[9]	ID[9]	-
AA9	**GPIOC[6]/ID[6]**	ISOSZP	GPIOC[6]	GPIOC[6]	ID[6]	-
AA10	**GPIOC[4]/ID[4]**	ISOSZP	GPIOC[4]	GPIOC[4]	ID[4]	-
AA11	**GPIOC[0]/ID[0]**	ISOSZP	GPIOC[0]	GPIOC[0]	ID[0]	-
AA12	**GPIOE[10]/ZD[10]**	ISOSZP	GPIOE[10]	GPIOE[10]	CD[10]	-
AA13	**GPIOE[7]/ZD[7]**	ISOSZP	GPIOE[7]	GPIOE[7]	CD[7]	-
AA14	**GPIOE[3]/ZD[3]**	ISOSZP	GPIOE[3]	GPIOE[3]	CD[3]	-
AA15	**GPIOF[9]/ZA[25]/OM[3]**	ISOSZP	GPIOF[9]	GPIOF[9]	CA[25]	OM[3]
AA16	**GPIOF[4]/ZA[20]**	ISOSZP	GPIOF[4]	GPIOF[4]	CA[20]	-
AA17	**GPIOF[1]/ZA[17]**	ISOSZP	GPIOF[1]	GPIOF[1]	CA[17]	-
AA18	**GPIOF[0]/ZA[16]**	ISOSZP	GPIOF[0]	GPIOF[0]	CA[16]	-
AA19	**GPIOG[7]/ZA[7]**	ISOSZP	GPIOG[7]	GPIOG[7]	CA[7]	-
AA20	**GPIOG[6]/ZA[6]**	ISOSZP	GPIOG[6]	GPIOG[6]	CA[6]	-
AA21	**GPIOG[1]/ZA[1]**	ISOSZP	GPIOG[1]	GPIOG[1]	CA[1]	-
AA22	**GPIOI[10]/nSCS[2]**	ISOSZP	GPIOI[10]	GPIOI[10]	nSCS[2]	-
AB1	**GPIOO[3]/SSPCLK**	ISOSZP	GPIOO[3]	GPIOO[3]	SSPCLK	-
AB2	**GPIOO[1]/SSPTXD**	ISOSZP	GPIOO[1]	GPIOO[1]	SSPTXD	-
AB3	**GPIOH[6]/XDOFF**	ISOSZP	GPIOH[6]	GPIOH[6]	XDOFF	-
AB4	**GPIOH[1]/ICLKOUT**	ISOSZP	GPIOH[1]	GPIOH[1]	ICLKOUT	-

Ball#	Name	Type	Func. After Reset	Primary Function	Alternate Function 1	Alternate Function 2
AB5	**GPIOC[15]/ID[15]**	ISOSZP	GPIOC[15]	GPIOC[15]	ID[15]	-
AB6	**GPIOC[11]/ID[11]**	ISOSZP	GPIOC[11]	GPIOC[11]	ID[11]	-
AB7	**GPIOC[8]/ID[8]**	ISOSZP	GPIOC[8]	GPIOC[8]	ID[8]	-
AB8	**GPIOC[7]/ID[7]**	ISOSZP	GPIOC[7]	GPIOC[7]	ID[7]	-
AB9	**GPIOC[3]/ID[3]**	ISOSZP	GPIOC[3]	GPIOC[3]	ID[3]	-
AB10	**GPIOC[1]/ID[1]**	ISOSZP	GPIOC[1]	GPIOC[1]	ID[1]	-
AB11	**GPIOE[14]/ZD[14]**	ISOSZP	GPIOE[14]	GPIOE[14]	CD[14]	-
AB12	**GPIOE[11]/ZD[11]**	ISOSZP	GPIOE[11]	GPIOE[11]	CD[11]	-
AB13	**GPIOE[9]/ZD[9]**	ISOSZP	GPIOE[9]	GPIOE[9]	CD[9]	-
AB14	**GPIOE[5]/ZD[5]**	ISOSZP	GPIOE[5]	GPIOE[5]	CD[5]	-
AB15	**GPIOE[2]/ZD[2]**	ISOSZP	GPIOE[2]	GPIOE[2]	CA[24]	-
AB16	**GPIOF[8]/ZA[24]/OM[2]**	ISOSZP	GPIOF[8]	GPIOF[8]	CA[24]	OM[2]
AB17	**GPIOF[6]/ZA[22]**	ISOSZP	GPIOF[6]	GPIOF[6]	CA[22]	-
AB18	**GPIOF[3]/ZA[19]**	ISOSZP	GPIOF[3]	GPIOF[3]	CA[19]	-
AB19	**GPIOF[2]/ZA[18]**	ISOSZP	GPIOF[2]	GPIOF[2]	CA[18]	-
AB20	**GPIOG[13]/ZA[13]**	ISOSZP	GPIOG[13]	GPIOG[13]	CA[13]	-
AB21	**GPIOG[12]/ZA[12]**	ISOSZP	GPIOG[12]	GPIOG[12]	CA[12]	-
AB22	**GPIOG[0]/ZA[0] (DQMz[0], BTENB0)**	ISOSZP	GPIOG[0]	GPIOG[0]	CA[0] (DQMz[0],BTENB0)	-

TABLE 2-3. MP2520F PIN OUT – BALLPAD NUMBER ORDER

- IA : Analog Input
- OA : Analog Output
- IAOA : Analog Input/Output
- IS : Schmitt trigger Input
- OS : Schmitt trigger Output
- ISOS : Schmitt trigger Input/Output
- ISOSZP : Schmitt trigger Input/Output Tri-state Pull-up enable
- OD : Open Drain
- SUP : Supply

2.4 SYSTEM CONFIGURATION

Pin Name	Ball	Function Name	Description
GPIOA[14]/VD[22]	E2	RstCfgNFBoot	Nand Boot Enable
GPIOA[13]/VD[21]	G4	RstCfgNFBSize	Nand Boot Size : 0 : 2048byte, 1 : 4096byte
GPIOA[12]/VD[20]	G3	RstCfgNFBUSWidth	Nand flash Bus Width : 0 : 8bit, 1 : 16bit
GPIOA[11]/VD[19]	F2	RstCfgNFType	Nand flash Type : 0 : 3 Address, 1 : 4 Address
GPIOA[10]/VD[18]	H5	RstCfgSR0BUSWidth	SRAM Bus Width : 0 : 8bit, 1 : 16 bit
GPIOA[9]/VD[17]	E1	RstCfgSDRTYPE	SDRAM Type 0 : Full up / Full Down
GPIOA[8]/VD[16]	G2	RstCfgBUSCBW	SDRAM Total Bus Width 0 : 16 bit 1 : 32 bit
GPIOA[7]/VD[15]	F1	RstCfgSDRBW[1]	SDRAM Bus Width 00 : 4bit, 01 : 8bit, 10 : 16bit
GPIOA[6]/VD[14]	H3	RstCfgSDRBW[0]	
GPIOA[5]/VD[13]	J5	RstCfgSDRCAP[1]	SDRAM Capacity 00 : 64Mbit, 01 : 128Mbit, 10 : 256 Mbit, 11 : 512 Mbit
GPIOA[4]/VD[12]	H2	RstCfgSDRCAP[0]	
GPIOA[3]/VD[11]	G1	RstCfgShadow	SDRAM Shadow Enable,
GPIOA[1]/VD[9]	K6	RstCfgUARTBootClk	UART Boot Clock : 0 : PLL clock, 1 : ABITCLK
GPIOA[0]/VD[8]	H1	RstCfgBootDown	UART Boot Enable : 0
GPIOB[15]/VD[7]	J2	ARM940T DEBUG Enable	ARM940 ICE Debug Enable : 0
GPIOB[14]/VD[6]	J1	RstCfgSRBuf	SRAM Buffer Enable
GPIOB[13]/VD[5]	K4	RstCfgNFBuf	Nand flash Buffer Enable

TABLE 2-4. SYSTEM CONFIGURATION

2.5 TEST MODE PINS

Pin Name	Ball	Function Name	Description
TEST_EN	G12	Test Enable	0 : Normal mode 1 : Test mode
OM0	Y2	External Clock Enable for FCLK	0 : PLL clock enable 1 : External Clock enable
GPIOF[9]/ZA[25]	AA15	OM[3]	If TEST_EN is high this signals are used test pins.
GPIOF[8]/ZA[24]	AB16	OM[2]	If TEST_EN is high this signals are used test pins
GPIOF[7]/ZA[23]	V14	OM[1]	If TEST_EN is high this signals are used test pins

TABLE 2-5. TEST MODE PINS

2.6 PIN DESCRIPTION NOTES

GPIO Reset Operation

After reset, all GPIO pins except GPIOD[1:0], GPIOE[15:0], GPIOF[9:0], GPIOG[15:0], GPIOH[0], GPIOI[15:0], GPIOJ[15:0], and GPIOL[10], will be set to input. The default values of the excepted GPIO pins are as follows:

GPIOD[1:0] : Alt Function 1

GPIOE[15:8] : Alt Function 1 for SRAM Boot and the 16bit SRAM Bus Width. Otherwise, the default value will be GPIO input

GPIO[9:0] : Alt Function 1 for SRAM Boot. Otherwise, the default value will be GPIO Input

GPIOG[15:0] : Alt Function 1 for SRAM Boot. Otherwise, the default value will be the GPIO Input

If the GPIO Alt. Function Register is set, the GPIO pins are used as the alternative function.

GPIO Stop Mode Operation

In Stop mode, GPIO states of all pins are determined by the values of GPIO Alt. Function Register and GPIO Output Register, except for the GPIOE, GPIOF, GPIOG, GPIOI, and GPIOJ pins, the states of which are determined by the value of GPIO Alive Register.

CHAPTER 3

MEMORY CONTROLLER

3. MEMORY CONTROLLER

3.1 OVERVIEW

The MP2520F Memory Controller is based on a Unified Memory Architecture (UMA). This Controller consists of three main control units : dynamic memory, static memory, and a PCMCIA/CF interface. Each unit has dedicated control pins, and has the following features:

Unified Memory Architecture (UMA)

- One Bank of SDRAM (16 or 32bit data bus supported)
  - Supports Active Power Down mode automatically
  - Supports Self Refresh mode
- Four Static Memory Chip Selects (16bit data bus supported)
- Card Interface supporting PCMCIA or Compact Flash
- Supports UDMA (Ultra DMA), MDMA (Multiword DMA) for IDE.

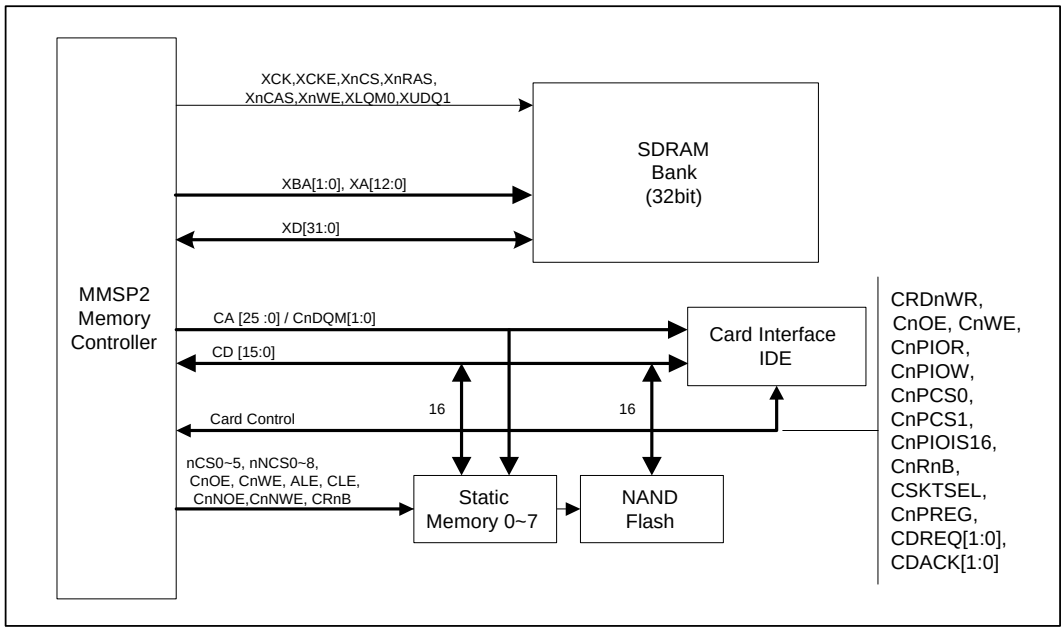


Figure 3-1. Memory Controller Block Diagram

3.2 MEMORY MAP

MP2520F Memory Map after Reset

The SDRAM Bank and the Static Memory Bank can be exchanged by the CfgShadow Pin and the CPU.

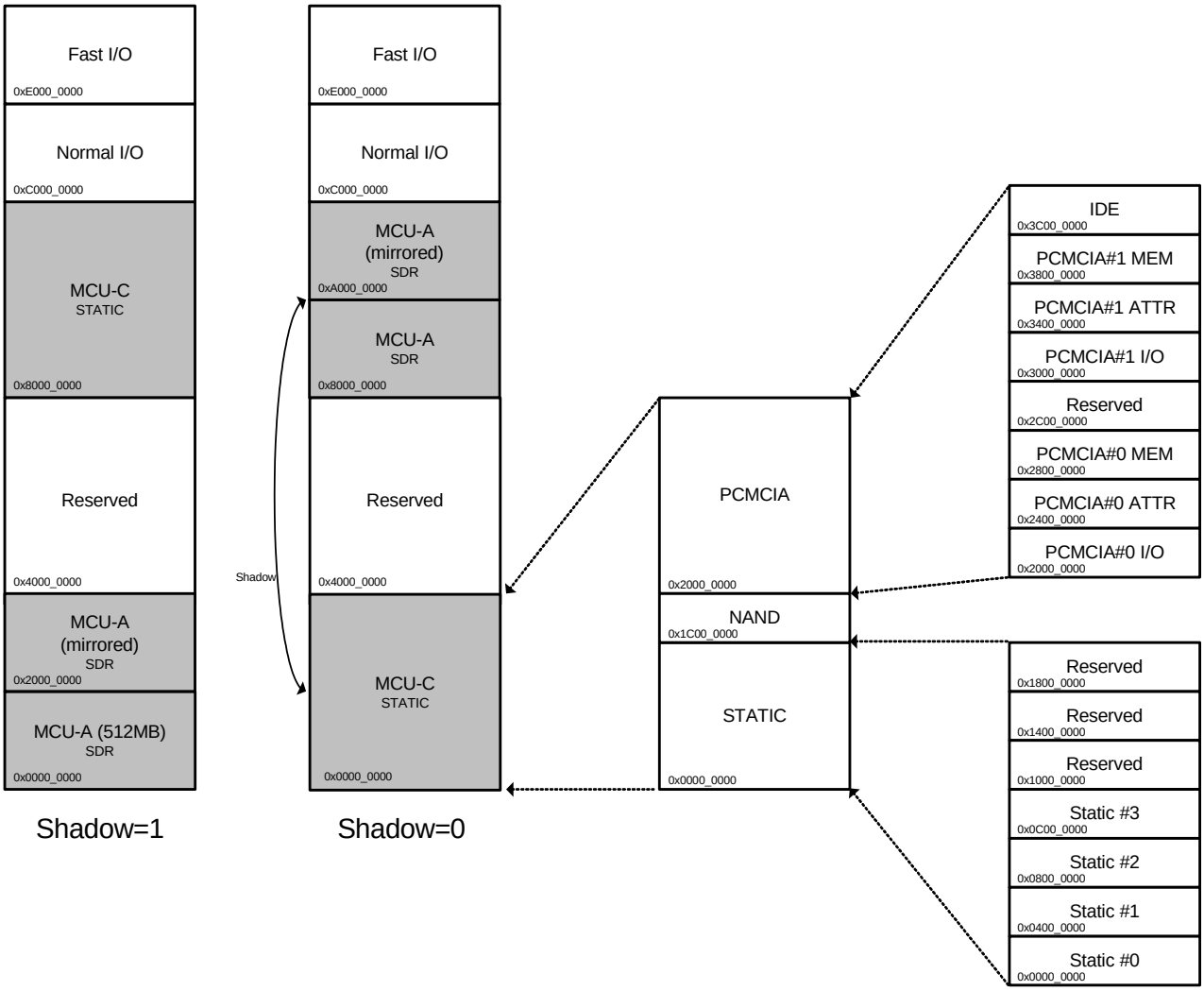


Figure 3-2. SDRAM Bank/Static Memory Bank Exchange

3.2.1 MCU-C BANK (STATIC MEMORY CONTROLLER)

- Memory Master : CPU, DMA, USB Host, 2D Controller, ISP, Display Controller, Stream I/F
- Data Bus Width : 8/16bit Interface
- Address Region : If Shadow=0 then 0x0000_0000 ~ 0x3FFF_FFFF.
  If Shadow=1 then 0x8000_0000 ~ 0xBFFF_FFFF

Supported Memory Type :

- Static Memory : Asynchronous SRAM, ROM, NOR-Flash
- Card Interface : PCMCIA/CF
- IDE Interface : Support MDMA, UDMA for HDD, CD-ROM, DVD-ROM

A. NoWait Static Memory Timing Diagram

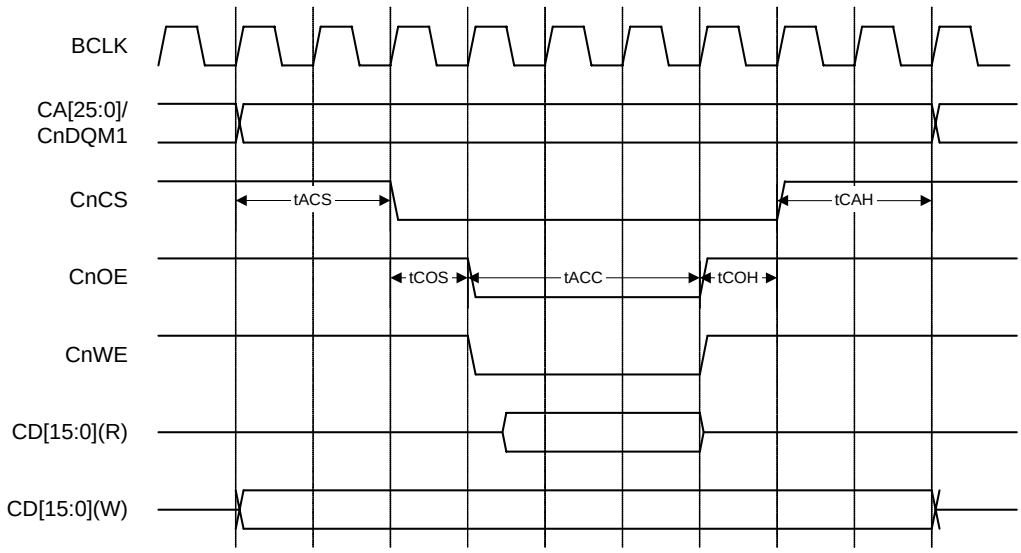


Figure 3-3. No Wait Timing Diagram

B. Wait Static Memory Timing Diagram

If Wait Control corresponding to each static memory bank is enabled. The Access duration should be prolonged by the external RnB (Ready&Busy) pin while the memory bank is active.

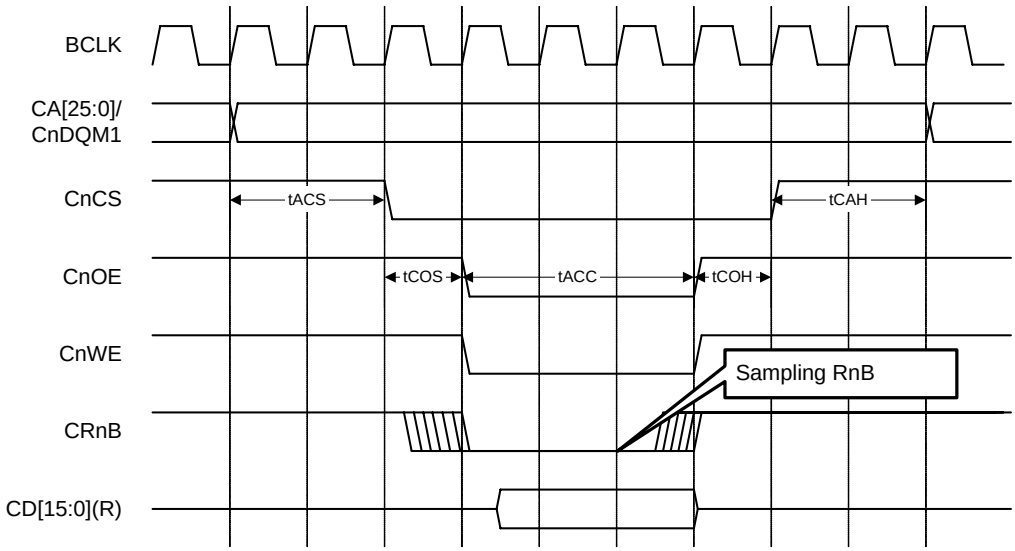


Figure 3-4.Wait Timing Diagram

C. PCMCIA/CF Memory or I/O 16bit Access Timing Diagram

If Wait Control corresponding to each static memory bank is enabled. The Access duration should be prolonged by the external RnB

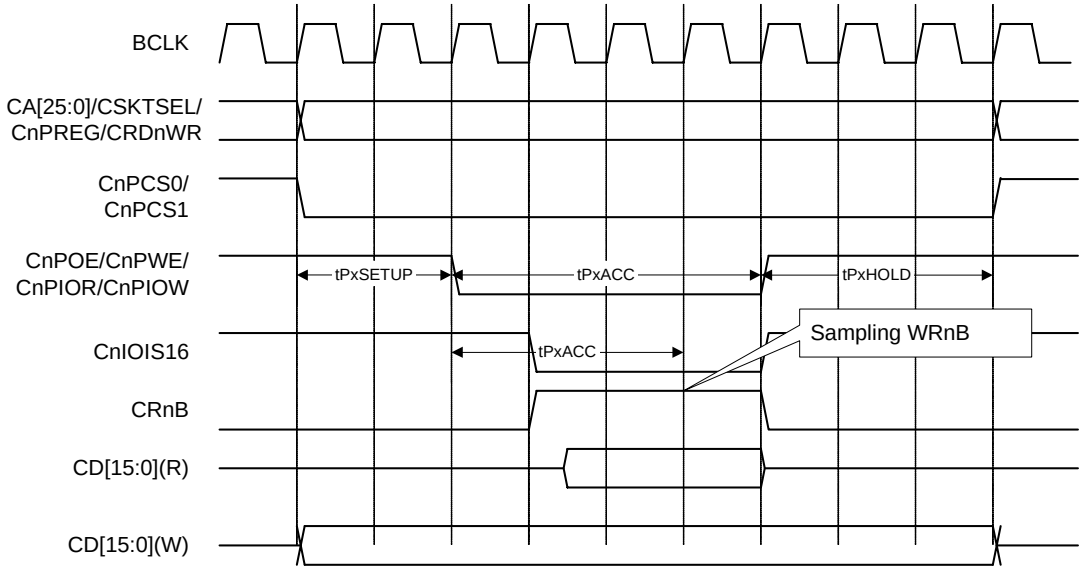


Figure 3-5. PCMCIA/CF Memory or I/O 16bit Access Timing Diagram

D. PCMCIA/CF I/O 16bit Access to 8bit Device Timing Diagram

PCMCIA/CF controller creates 2 sets of 8bit access cycle when memory master accesses 8bit device in the form of 16bit. It creates 4 sets of 8bit access cycle when memory master accesses in the form of 32bit.

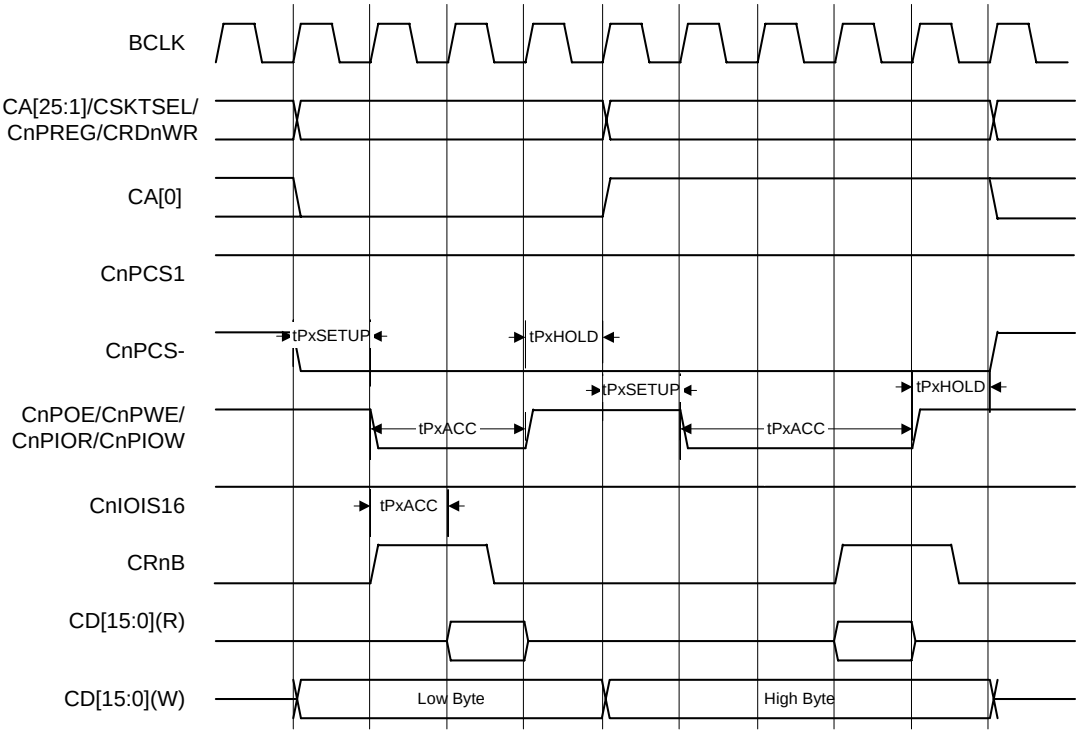


Figure 3-6. PCMCIA/CF 16bit Access to 8bit Device Timing Diagram

E. NAND Flash Timing Diagram

nNFCE[0~3] Signal, which determined by NFBANK[1:0] control bit of MEMNANDCTRLW, is asserted regardless accessing of NAND memory from memory master. Therefore, care must be taken when perform buffer controller using nNFCE.

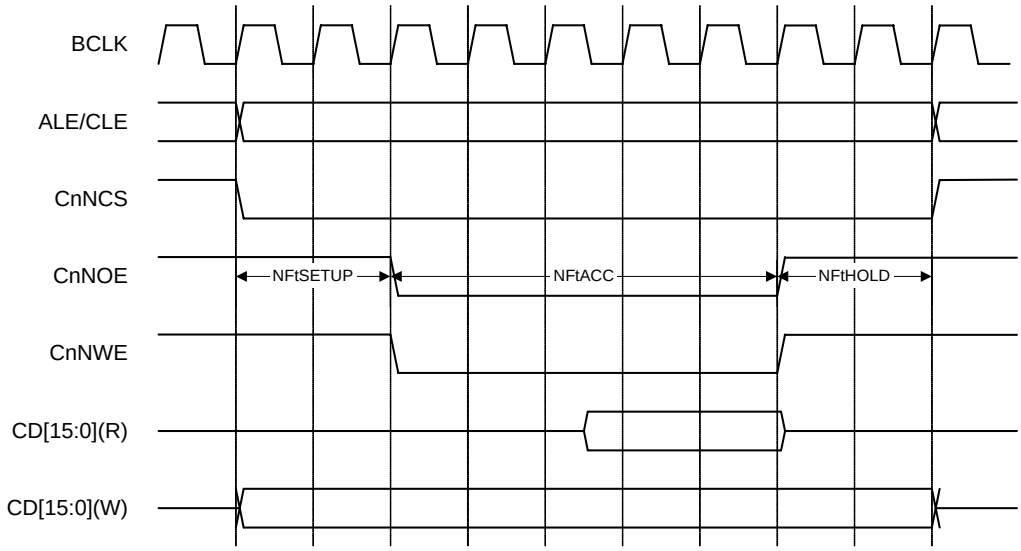


Figure 3-7. NAND Flash Timing Diagram

F. MDMA(Multi-Word DMA) Timing Diagram

MDMA and UDMA transfer mode are supported only at IDE mode. For detailed timing diagram, refer to AT spec.

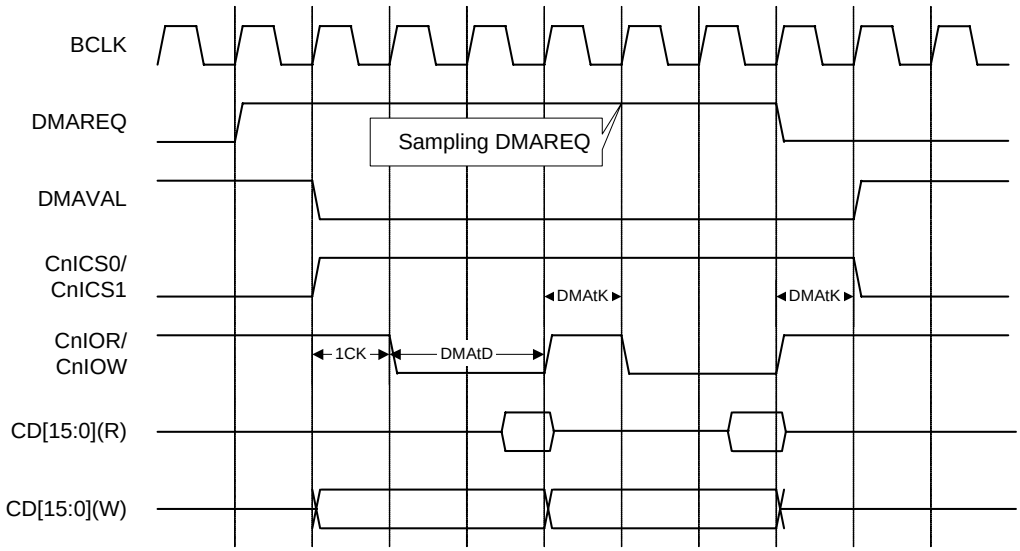


Figure 3-8. MDMA (MultiWord DMA) Timing Diagram

G. IDE UDMA (Ultra DMA) Timing Diagram

MDMA and UDMA transfer mode are supported only at IDE mode. For detailed timing diagram, refer to AT spec.

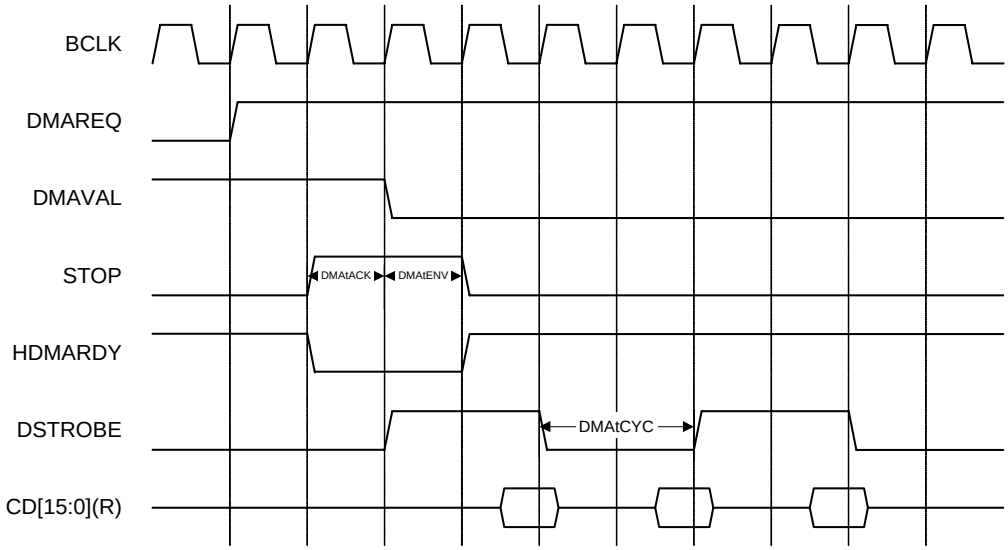


Figure 3-9. UDMA Timing Diagram

3.2.2 MCU-A BANK (SDRAM CONTROLLER)

- **Memory Master** : CPU, DMA,USB Host, 2D Graphic Controller, ISP, Display Controller, Transport Stream I/F
- **Data Bus Width** : 16/32bit Interface
- **Address Region** : 0x8000_0000 ~ 0x9FFF_FFFF
- **Supported Memory Type** : SDRAM
  64Mbit : x8, x16, x32bit
  128Mbit: x8, x16, x32bit
  256Mbit: x8, x16, x32bit
  512Mbit: x8, x16, x32bit

3.3 INTERFACE

3.3.1 DRAM CONNECTION

Regardless of the DRAM capacity and the Data bus width, MP2520F address pin 0 is connected to DRAM Address pin 0,and so on with each MP2520F address pin connected to the respective DRAM Address pin in turn. In the same way, the Bank Address is also connected to the Address pin by turns.

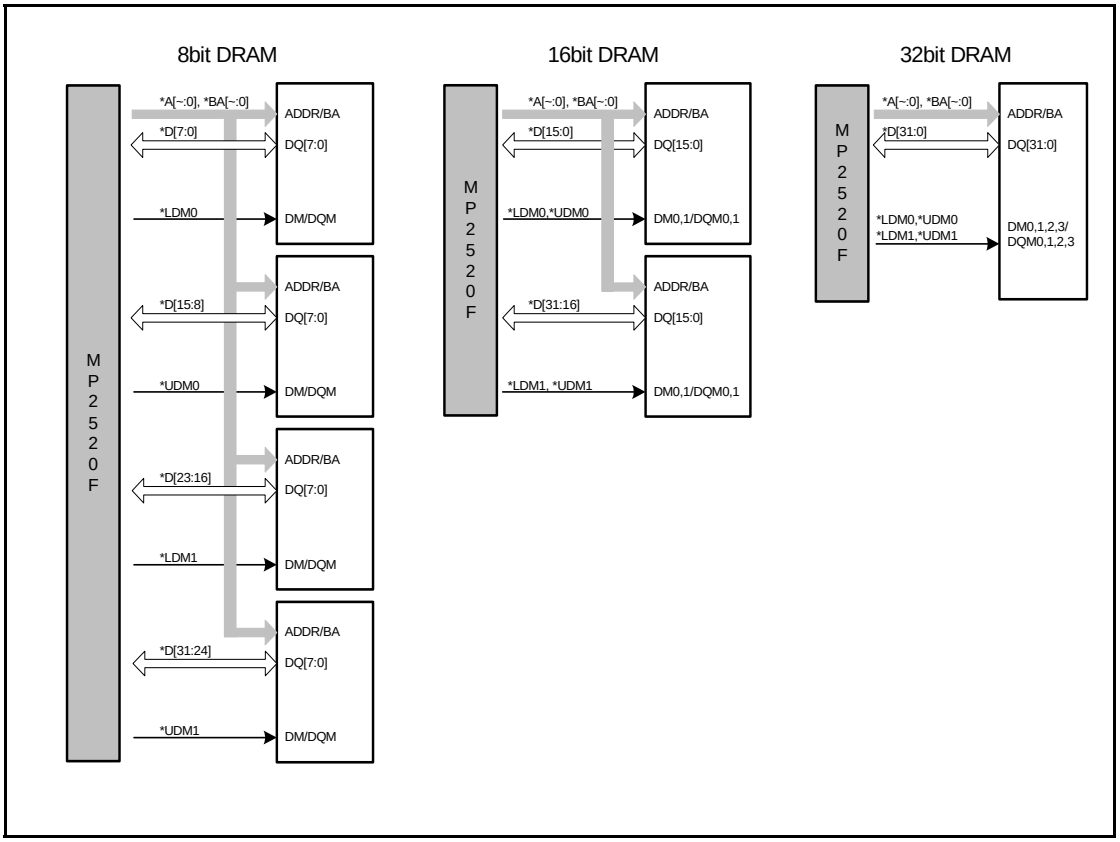


Figure 3-10. DRAM Connection

3.3.2 IDE/PCMCIA INTERFACE

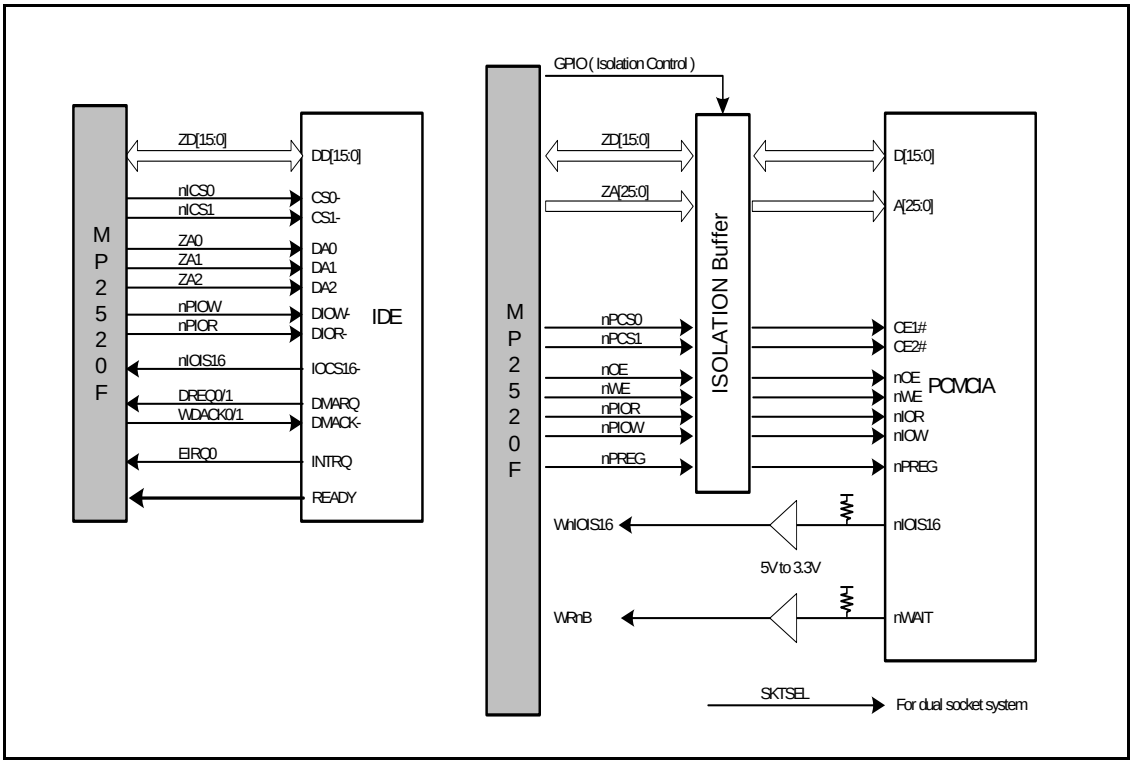


Figure 3-11. IDE/PCMCIA Interface

For the realization of the PCMCIA, the PCMCIA Interface has to be reset and the extra GPIO has to be used to control PCMCIA Power. In addition, a specific signal has to be transferred to the MP2520F via the Buffers because of a voltage property.

3.4 NAND BOOT OVERVIEW

The MP2520F supports the booting function with NAND Flash.

The following figure shows the data path of booting with NAND:

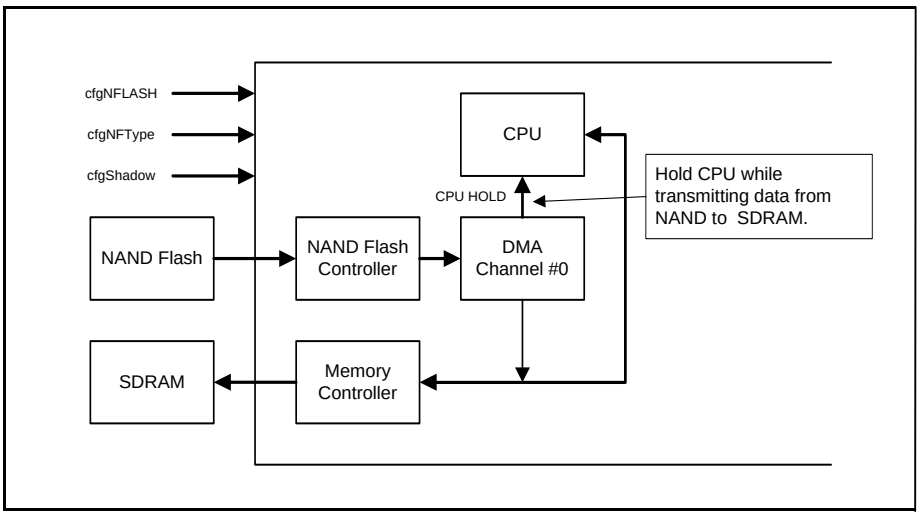


Figure 3-12. NAND Boot Procedure

FEATURES:

- Support 4 NAND Flash Banks. : x8, x16 bit Bus Width
- Contain Hardware ECC Block
- Support NAND Flash Booting : Small Block Only.

NAND BOOT SEQUENCE:

1. In case cfgNFBOOT pin is high, DMA prohibits main memory access since DMA holds CPU.
2. NAND Flash Controller which reads the data of external NAND flash saves at the internal buffer.
3. NAND Flash requests DMA transmission to DMA Channel 0.
4. DMA transmits to main memory.
5. If the transmission is completed, make the CPU become normal operation by lifting CPU hold.

Caution when NAND Boot:

- When NAND Boot, there should be Read/Writable Memory of 512Byte in physical address 0
- Because ECC is not executed when NAND boot, there should be no bit fail in the early 512Byte of flash.

NORMAL ACCESS SEQUENCE

READ Cycle:

1. Write NAND FLASH Command to NFCMD. (Refer to NAND Flash data book)
2. Access address of memory which tries to access to NFADDR register by 3~4 times according to the sort of NAND Flash. (Refer to NAND Flash data book)
3. Check whether NAND Flash is ready or not by reading the PendIRQ bit of the MEMNANDCTRLW Register.
4. Read data through the NFDATA Register.
5. Read the result of ECC through the NFECC01 and NFECC2 Register.

Write Cycle

1. Write the NAND FLASH Command to NFCMD. (Refer to NAND Flash data book).
2. Access address of memory which tries to access to NFADDR register by 3~4 times according to the sort of NAND Flash. (Refer to NAND Flash data book)
3. Write data through the NFDATA Register.
4. Read the result of ECC through the NFECC01 and NFECC2 Register.
5. Write NAND FLASH Command to NFCMD. (Refer to NAND Flash data book)
6. Check whether NAND flash is ready or not by reading the PendIRQ bit of the MEMNANDCTRLW Register. (For the exact sequence of NAND Flash, please refer to NAND Flash data book)

z	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
ECC0	P64	P64'	P32	P32'	P16	P16'	P8	P8'
ECC1	P1024	P1024'	P512	P512'	P256	P256'	P128	P128'
ECC2	P4	P4'	P2	P2'	P1	P1'	P2048	P2048'

TABLE 3-1. 512BYTE ECC PARITY CODE ASSIGNMENT TABLE

Generate only 512Byte ECC Parity Code during Write / Read operating:

ECC Parity Code consists of 3 bytes per 512 byte

24bit ECC Parity Code = 18bit line parity + 6bit Column Parity

ECC generator block executes the following:

1. When the MP2520F writes data to NAND, the ECC Generator Block generates an ECC code.
2. When the MP2520F reads data from NAND, the ECC Generator Block generates an ECC code and compare it with the pre-written ECC code.

3.5 BANK C MEMORY CONTROL REGISTER

Bank C Configuration Register (MEMCFGW)

Address : C000 3A00h

Bit	R/W	Symbol	Description	Reset Value
15 : 12	R	**Reserved**	-	-
11	R/W	**IDEBUF**	Set Buffer usage at IDE Region 0 : Bypass 1 : Buffered	0b
10	R/W	**CDBUF**	Set Buffer usage at PCMCIA/CF Region 0 : Bypass 1 : Buffered	01b
9	R/W	**NFBUF**	Set Buffer usage at NAND Flash Region 0 : Bypass 1 : Buffered	NFBUF
8	R/W	**SRBUF**	Set Buffer usage at Static Region 0 : Bypass 1 : Buffered	SRBUF
7	R/W	**NANDBW**	Set Data Bit Width of NAND Flash 0 : Byte 1 : Half-Word	CfgNFBUSWidth
6 : 4	R	**Reserved**	-	-
3	R/W	**SR3BW**	Set Data Bit Width of STATIC #3 0 : Byte 1 : Half-Word	01b
2	R/W	**SR2BW**	Set Data Bit Width of STATIC #2 0 : Byte 1 : Half-Word	01b
1	R/W	**SR1BW**	Set Data Bit Width of STATIC #1 0 : Byte 1 : Half-Word	01b
0	R/W	**SR0BW**	Set Data Bit Width of STATIC #0 0 : Byte 1 : Half-Word	CfgSR0BUSWidth

TABLE 3-2. BANK C CONFIGURATION REGISTER (MEMCFGW)

Bank C Timing Register #0 (MEMTIMEW0)

Address : C000 3A02h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**Reserved**	-	-
7 : 6	R/W	**tACS3**	tACS(Address Set-up Time before nSCS) of STATIC #3 0 : 0 Cycle 1 : 2 Cycles 2 : 3 Cycles 3 : 4 Cycles	11b
5 : 4	R/W	**tACS2**	tACS of STATIC #2	11b
3 : 2	R/W	**tACS1**	tACS of STATIC #1	11b
1 : 0	R/W	**tACS0**	tACS of STATIC #0	11b

TABLE 3-3. BANK C TIMING REGISTER #0 (MEMTIMEW0)

Bank C Timing Register #1 (MEMTIMEW1)

Address : C000 3A04h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**Reserved**	-	-
7 : 6	R/W	**tCOS3**	tCOS (Chip selection Setup Time before nSOE/nSWE) of STATIC #3 0 : 0 Cycle 1 : 2 Cycles 2 : 3 Cycles 3 : 4 Cycles	11b
5 : 4	R/W	**tCOS2**	tCOS of STATIC #2	11b
3 : 2	R/W	**tCOS1**	tCOS of STATIC #1	11b
1 : 0	R/W	**tCOS0**	tCOS of STATIC #0	11b

TABLE 3-4. BANK C TIMING REGISTER #1 (MEMTIMEW1)

Bank C Timing Register #2 (MEMTIMEW2)

Address : C000 3A06h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**Reserved**	-	-
7 : 6	R/W	**tCOH3**	tOCH (Chip selection Hold Time before nSOE/nSWE) of STATIC #3 0 : 0 Cycle 1 : 2 Cycles 2 : 3 Cycles 3 : 4 Cycles	11b
5 : 4	R/W	**tCOH2**	tOCH of STATIC #2	11b
3 : 2	R/W	**tCOH1**	tOCH of STATIC #1	11b
1 : 0	R/W	**tCOH0**	tOCH of STATIC #0	11b

TABLE 3-5. BANK C TIMING REGISTER #2 (MEMTIMEW2)

Bank C Timing Register #3 (MEMTIMEW3)

Address : C000 3A08h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**Reserved**	-	-
7 : 6	R/W	**tCAH3**	tCAH (Address Hold Time before nSCS) of STATIC #3 0 : 0 Cycle 1 : 2 Cycles 2 : 3 Cycles 3 : 4 Cycles	11b
5 : 4	R/W	**tCAH2**	tCAH of STATIC #2	11b
3 : 2	R/W	**tCAH1**	tCAH of STATIC #1	11b
1 : 0	RW	**tCAH0**	tCAH of STATIC #0	11b

TABLE 3-6. BANK C TIMING REGISTER #3 (MEMTIMEW3)

Bank C Timing Register #4 (MEMTIMEW4)

Address : C000 3A0Ah

Bit	R/W	Symbol	Description	Reset Value
15 :12	R/W	**tACC3**	tACC (Access Time) of STATIC #3 0 : 1 Cycle 1 : 2 Cycles 2 : 3 Cycles ~15 : ~16 Cycles	1111b
11 : 8	R/W	**tACC2**	tACC of STATIC #2	1111b
7 : 4	R/W	**tACC1**	tACC of STATIC #1	1111b
3 : 0	RW	**tACC0**	tACC of STATIC #0	1111b

TABLE 3-7. BANK C TIMING REGISTER #4 (MEMTIMEW4)

Bank C Wait Control Register (MEMWAITCTRLW)

Address : C000 3A0Eh

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**Reserved**	-	-
7 : 6	R/W	**WAITENB3**	Wait Control Enable of STATIC #3 0x : Disable Wait Control 10 : Enable Wait Control, High Active Wait 11: Enable Wait Control, Low Active Wait	01b
5 : 4	R/W	**WAITENB2**	Wait Control Enable of STATIC #2	01b
3 : 2	R/W	**WAITENB1**	Wait Control Enable of STATIC #1	01b
1 : 0	RW	**WAITENB0**	Wait Control Enable of STATIC #0	01b

TABLE 3-8. BANK C WAIT CONTROL REGISTER (MEMWAITCTRLW)

Bank C Page Control Register (MEMPAGEW)

Address : C000 3A10h

Bit	R/W	Symbol	Description	Reset Value
15 :12	R	**Reserved**	-	-
11	R/W	**SRPAGE3**	SRPAGE of STATIC #3	0b
10	R/W	**SRPAGE2**	SRPAGE of STATIC #2	0b
9	R/W	**SRPAGE1**	SRPAGE of STATIC #1	0b
8	R/W	**SRPAGE0**	SRPAGE of STATIC #0	0b
7	R	**Reserved -**	-	-
6	R/W	**IOIS16ENB**	Enable IOIS16 Control of PCMCIA Region	1b
5 : 0	RW	**Reserved -**	-	-

TABLE 3-9. BANK C PAGE CONTROL REGISTER (MEMPAGEW)

Bank C IDE Timing Control Register (MEMIDETIMEW)

Address : C000 3A12h

Bit	R/W	Symbol	Description	Reset Value
15	R	**Reserved**	-	-
14 :10	R/W	**tIHOLD**	Data Hold Time of IDE BUS	10b
9 : 5	R/W	**tISETUP**	Data Setup Time of IDE BUS	10b
4 : 0	RW	**tIACC**	Data Access Time of IDE BUS	10b

TABLE 3-10. BANK C IDE TIMING CONTROL REGISTER (MEMIDETIMEW)

Bank C PCMCIA Memory Timing Control Register (MEMPCMCIAMW)

Address : C000 3A14h

Bit	R/W	Symbol	Description	Reset Value
15	R	**Reserved**	-	-
14 :10	R/W	**tPMHOLD**	Data Hold Time of PCMCIA Memory Region	11b
9 : 5	R/W	**tPMSETUP**	Data Setup Time of PCMCIA Memory Region	11b
4 : 0	RW	**tPMACC**	Data Access Time of PCMCIA Memory Region	11b

TABLE 3-11. BANK C PCMCIA MEMORY TIMING CONTROL REGISTER (MEMPCMCIAMW)

Bank C PCMCIA Attribute Timing Control Register (MEMPCMCIAAW)

Address : C000 3A16h

Bit	R/W	Symbol	Description	Reset Value
15	R	**Reserved**	-	-
14 :10	R/W	**tPAHOLD**	Data Hold Time of PCMCIA Attribute Region	100b
9 : 5	R/W	**tPASETUP**	Data Setup Time of PCMCIA Attribute Region	100b
4 : 0	R/W	**tPAACC**	Data Access Time of PCMCIA Attribute Region	100b

TABLE 3-12. BANK C PCMCIA ATTRIBUTE TIMING CONTROL REGISTER (MEMPCMCIAAW)

Bank C PCMCIA I/O Timing Register (MEMPCMCIAIW)

Address : C000 3A18h

Bit	R/W	Symbol	Description	Reset Value
15	R	**Reserved**	-	-
14 :10	R/W	**tPIHOLD**	Data Hold Time of PCMCIA I/O Region	101b
9 : 5	R/W	**tPISETUP**	Data Setup Time of PCMCIA I/O Region	101b
4 : 0	R/W	**tPIACC**	Data Access Time of PCMCIA I/O Region	101b

TABLE 3-13. BANK C PCMCIA I/O TIMING REGISTER (MEMPCMCIAIW)

Bank C PCMCIA Wait Timing Register #0 (MEMPCMCIAWAITW)

Address : C000 3A1Ah

Bit	R/W	Symbol	Description	Reset Value
15	R	**Reserved**	-	-
14 :10	R/W	**PCMWAITM**	PCMCIA Wait Control for Memory Region	110b
9 : 5	R/W	**PCMWAITA**	PCMCIA Wait Control for Attribute Region	110b
4 : 0	R/W	**PCMWAITI**	PCMCIA Wait Control for I/O Region	110b

TABLE 3-14. BANK C PCMCIA WAIT TIMING REGISTER #0 (MEMPCMCIAWAITW)

Bank C IDE Wait Timing Register #1 (MEMIDEWAITW)

Address : C000 3A1Ch

Bit	R/W	Symbol	Description	Reset Value
15 : 5	R	**Reserved**	-	-
4 : 0	R/W	**IDEWAIT**	IDE Wait Control	10b

TABLE 3-15. BANK C IDE WAIT TIMING REGISTER #1 (MEMIDEWAITW)

Bank C DMA Timeout Register (MEMDTIMEOUTW)

Address : C000 3A20h

Bit	R/W	Symbol	Description	Reset Value
15 : 12	R/W	**DMATIMEOUT**	Perform Host termination automatically in case of no response during TIMEOUT. Unit is 8Cycle(BCLK).-	100b
11 : 10	R	**Reserved**	Reserved	-
9 : 0	R/W	**DMALIMIT**	Maximum Data Transfer number for IDE BUS.	1001b

TABLE 3-16. BANK C DMA TIMEOUT REGISTER (MEMDTIMEOUTW)

Bank C DMA Control Register (MEMDMACTRLW)

Address : C000 3A22h

Bit	R/W	Symbol	Description	Reset Value
15 :14	R	**Reserved**	-	-
13	R/W	**DMAENB1**	DMA Enable Channel 1 0 : Disable 1 : Enable	0b
12	R/W	**DMAENB0**	DMA Enable Channel 0 0 : Disable 1 : Enable	1b
11 :10	R	**Reserved**	-	-
9	R/W	**DMAWIDTH1**	Set DMA Transfer Width Channel 1 0 : 8bit 1 : 16bit	1b
8	R/W	**DMAWIDTH0**	Set DMA Transfer Width Channel 0 0 : 8bit 1 : 16bit	1b
7 : 4	R	**Reserved**	-	-
3 : 2	R/W	**DMAMODE1**	Set DMA Mode Channel 1 00 : Multi-Word DMA Read 01 : Multi-Word DMA Write 10 : Ultra-DMA Read 11 : Ultra-DMA Write	01b
1 : 0	R/W	**DMAMODE0**	Set DMA Mode Channel 0 00 : Multi-Word DMA Read 01 : Multi-Word DMA Write 10 : Ultra-DMA Read 11 : Ultra-DMA Write	11b

TABLE 3-17. BANK C DMA CONTROL REGISTER (MEMDMACTRLW)

Bank C DMA Polarity Register (MEMDMAPOLW)

Address : C000 3A24h

Bit	R/W	Symbol	Description	Reset Value
15 :14	R	**Reserved**	-	-
13	R/W	**DMAREQPOL1**	Set WDREQ1 Polarity Channel 1 0 : Low Active 1 : High Active	1b

Bit	R/W	Symbol	Description	Reset Value
12	R/W	**DMAREQPOL0**	Set WDREQ0 Polarity Channel 0 0 : Low Active 1 : High Active	1b
11 :10	R	**Reserved**	-	-
9	R/W	**DMAACKPOL1**	Set WDACK1 Polarity Channel 1 0 : Low Active 1 : High Active	0b
8	R/W	**DMAACKPOL0**	Set WDACK0 Polarity Channel 0 0 : Low Active 1 : High Active	0b
7 : 4	R	**Reserved**	-	-
3 : 2	R/W	**DMAPATH1**	Set DMA Path Channel 1 00 : Static Memory 01 : IDE 10 : PCMCIA #0 11 : PCMCIA #1	00b
1 : 0	RW	**DMAPATH0**	Set DMA Path Channel 0 00 : Static Memory 01 : IDE 10 : PCMCIA #0 11 : PCMCIA #1	01b

TABLE 3-18. BANK C DMA POLARITY REGISTER (MEMDMAPOLW)

Bank C DMA Timing Register #0 (MEMDMATIMEW0)

Address : C000 3A26h

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtD1**	Set tD(nIOR/nIOW asserted pulse width) Timing Channel 1	100b
4 : 0	RW	**DMAtD0**	Set tD Timing Channel 0	100b

TABLE 3-19. BANK C DMA TIMING REGISTER #0 (MEMDMATIMEW0)

Bank C DMA Timing Register #1 (MEMDMATIMEW1)

Address : C000 3A28h

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtK1**	Set tK(nIOR/nIOW negated pulse width) Timing Channel 1	100b
4 : 0	RW	**DMAtK0**	Set tK Timing of Channel 0	100b

TABLE 3-20. BANK C DMA TIMING REGISTER #1 (MEMDMATIMEW1)

Bank C DMA Timing Register #2 (MEMDMATIMEW2)

Address : C000 3A2Ah

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**		-
9 : 5	R/W	**DMAtACK1**	Set tACK(Setup Time before nDMACK) Timing Channel 1	100b
4 : 0	RW	**DMAtACK0**	Set tACK Timing Channel 0	100b

TABLE 3-21. BANK C DMA TIMING REGISTER #1 (MEMDMATIMEW1)

Bank C DMA Timing Register #3 (MEMDMATIMEW3)

Address : C000 3A2Ch

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtENV1**	Set tENV (Envelope time) Timing Channel 1	100b
4 : 0	RW	**DMAtENV0**	Set tENV Timing Channel 0	100b

TABLE 3-22. BANK C DMA TIMING REGISTER #3 (MEMDMATIMEW3)

Bank C DMA Timing Register #4 (MEMDMATIMEW4)

Address : C000 3A2Eh

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtRP1**	Set tRP (Ready to pause time) Timing Channel 1	100b
4 : 0	RW	**DMAtRP0**	Set tRP Timing Channel 0	100b

TABLE 3-23. BANK C DMA TIMING REGISTER #4 (MEMDMATIMEW4)

Bank C DMA Timing Register #5 (MEMDMATIMEW5)

Address : C000 3A30h

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtSS1**	Set tSS (Time from DSTROVE edge to negation of DMARQ) Timing Channel 1	100b
4 : 0	RW	**DMAtSS0**	Set tSS Timing Channel 0	100b

TABLE 3-24. BANK C DMA TIMING REGISTER #5 (MEMDMATIMEW5)

Bank C DMA Timing Register #6 (MEMDMATIMEW6)

Address : C000 3A32h

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 5	R/W	**DMAtMLI1**	Set tMLI (Interlock time with minimum) Timing Channel 1	100b
4 : 0	RW	**DMAtMLI0**	Set tMLI Timing Channel 0	100b

TABLE 3-25. BANK C DMA TIMING REGISTER #6 (MEMDMATIMEW6)

Bank C DMA Timing Register #7 (MEMDMATIMEW7)

Address : C000 3A34h (Reserved)

Bank C DMA Timing Register #8 (MEMDMATIMEW8)

Address : C000 3A36h

Bit	R/W	Symbol	Description	Reset Value
15 :13	R	**Reserved**	-	-
12	R/W	**DMARST**	Software Reset of DMA 0 : Idle 1 : Reset	0b
11 : 0	R	**Reserved**	-	-

TABLE 3-26. BANK C DMA TIMING REGISTER #8 (MEMDMATIMEW8)

Bank C DMA Strobe Control Register (MEMDMASTRBW)

Address : C000 3A38h

Bit	R/W	Symbol	Description	Reset Value
15 :13	R	**Reserved**	-	-
7 : 4	R/W	**DMAtCYC1**	Set Pulse Width of HSTROBE (1)	10b
3 : 0	RW	**DMAtCYC0**	Set Pulse Width of HSTROBE (0)	10b

TABLE 3-27. BANK C DMA STROBE CONTROL REGISTER (MEMDMASTRBW)

Bank C NAND FLASH CTRL Register (MEMNANDCTRLW)

Address : C000 3A3Ah

Bit	R/W	Symbol	Description	Reset Value
15	R/W	**IRQPEND**	Pending Register of RnB Rising Detect, Set to 1 to clear this bit.	-
14 :8	R	**Reserved**	-	
7	R	**RnB**	NAND Flash Status : RnB PAD의 상태를 읽어 볼 수 있다. 1 : Ready 0 : Busy	

Bit	R/W	Symbol	Description	Reset Value
6	R/W	**IRQENB**	Set Interrupt usage at RnB Signal Rising Edge of NAND Flash 0 : Disable 1: Enable	0b
5	R/W	**NFBOOTENB**	Set NAND Booting Enable 0 : Disable 1 : Enable	CfgNFBOOT
4	R/W	**NFBOOTSIZE**	Set transferring Byte number from NAND Flash at NAND Booting 0 : 2048Bytes 1 : 4096Bytes	CfgNFBSIZE
3	R/W	**NFBUSWIDTH**	Set NAND Flash Bus Width for NAND Booting 0 : 8bit 1 : 16bit	CfgNFBUSWidth
2	R/W	**NFTYPE**	Set NAND Flash Type for NAND Booting 0 : 3 Address NAND 1 : 4 Address NAND	CfgNFType
1 : 0	RW	**NFBANK**	Set NAND Flash Bank to Access	0b

TABLE 3-28. BANK C NAND FLASH CTRL REGISTER (MEMNANDCTRLW)

The RnB output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion.

Bank C NAND FLASH Timing Register (MEMNANDTIMEW)

Address : C000 3A3Ch

Bit	R/W	Symbol	Description	Reset Value
15 :12	R	**Reserved**	-	-
11 : 8	R/W	**NFtSETUP**	Set Data Setup Time of NAND Flash	100b
7 : 4	R/W	**NFtACC**	Set Data Access Time of NAND Flash	10000b
3 : 0	RW	**NFtHOLD**	Set Data Hold Time of NAND Flash	100b

TABLE 3-29. BANK C NAND FLASH TIMING REGISTER (MEMNANDTIMEW)

Bank C NAND FLASH ECC0 Register (MEMNANDECC0W)

Address : C000 3A3Eh

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**ECC0UPPER**	For 16bit NAND Flash, upper 8bit out of 16bit output. For 8bit NAND Flash, this value is ignored.	-
7 : 0	R	**ECC0LOWER**	For 8bit NAND Flash, ECC of 8bit Data output. For 16bit NAND Flash, lower 8bit out of 16bit output.	-

TABLE 3-30. BANK C NAND FLASH ECC0 REGISTER (MEMNANDECC0W)

Bank C NAND FLASH ECC1 Register (MEMNANDECC1W)

Address : C000 3A40h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**ECC1UPPER**	For 16bit NAND Flash, upper 8bit out of 16bit output. For 8bit NAND Flash, this value is ignored.	-
7 : 0	R	**ECC1LOWER**	For 8bit NAND Flash, ECC of 8bit Data output. For 16bit NAND Flash, lower 8bit out of 16bit output.	-

TABLE 3-31. BANK C NAND FLASH ECC1 REGISTER (MEMNANDECC1W)

Bank C NAND FLASH ECC2 Register (MEMNANDECC2W)

Address : C000 3A42h

Bit	R/W	Symbol	Description	Reset Value
15 : 8	R	**ECC1UPPER**	For 16bit NAND Flash, upper 8bit out of 16bit output. For 8bit NAND Flash, this value is ignored.	-
7 : 0	R	**ECC1LOWER**	For 8bit NAND Flash, ECC of 8bit Data output. For 16bit NAND Flash, lower 8bit out of 16bit output.	-

TABLE 3-32. BANK C NAND FLASH ECC2 REGISTER (MEMNANDECC2W)

Bank C NAND FLASH Data Counter Register (MEMNANDCNTW)

Address : C000 3A44h

Bit	R/W	Symbol	Description	Reset Value
15 :10	R	**Reserved**	-	-
9 : 0	R	**DATACNT**	Read currently transferred data number.	-

TABLE 3-33. BANK C NAND FLASH DATA COUNTER REGISTER (MEMNANDCNTW)

NAND Flash Data Register (NFDATA)

Address : 1C00 0000h (CfgShadow=0)
Address : 9C00 0000h (CfgShadow=1)

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	**NFDATA**	Data Register	00000000h

TABLE 3-35. NAND FLASH DATA REGISTER (NFDATA)

This will be connected to data bus of NAND flash.
In case of 16bit access, NAND Flash will access twice by 8bit automatically.

NAND Flash Command Register (NFCMD)

Address : 1C00 0010h (CfgShadow=0)
Address : 9C00 0010h (CfgShadow=1)

Bit	R/W	Symbol	Description	Reset Value
15:8	R	**Reserved**	-	-
7:0	R	**NFCMD**	Command Register	0b

TABLE 3-36. NAND FLASH COMMAND REGISTER (NFCMD)

This will be connected to data bus of NAND Flash. As CLE becomes high, notify the command cycle. This register will be accessed by a byte different from the NFDATA Register.

NAND Flash Address Register (NFADDR)

Address : 1C00 0018h (CfgShadow=0)
Address : 9C00 0018h (CfgShadow=1)

Bit	R/W	Symbol	Description	Reset Value
15:8	R	**Reserved**	-	-
7:0	W	**NFADDR**	Address Register	0b

TABLE 3-37. NAND FLASH ADDRESS REGISTER (NFADDR)

This will be connected to the data bus of the NAND Flash. As ALE becomes high, notify the address cycle. This resistor will be accessed by a byte different from the NFDATA Register.

3.6 BANK A MEMORY CONTROL REGISTER

Bank A SDRAM Configuration Register (MEMCFGX)

Address : C000 3800h

Bit	R/W	Symbol	Description	Reset Value
15 : 7	R	**Reserved**	-	-
5	R/W	**SDRTYPE**	Set DRAM Type 0 : SDR-SDRAM 1 : DDR-DRAM	CfgSDRTYPE
4	R/W	**SDRBUSBW**	Set data bit width of Bank 0 : 16bit 1 : 32bit	CfgSDRBUSBW
3 : 2	R/W	**SDRBW**	Set SDRAM bit width of DRAM which is used in Bank 00 : 4bit 01 : 8bit 10 : 16bit 11 : Reserved	CfgSDRBW
1 : 0	RW	**SDRCAP**	Set SDRAM Capacity of DRAM which is used in Bank 00 : 64Mbit 01 : 128Mbit 10 : 256Mbit 11 : 512Mbit	CfgSDRType

TABLE 3-38. BANK A SDRAM CONFIGURATION REGISTER (MEMCFGX)

Bank A TIMMING Register #0 (MEMTIMEX0)

Address : C000 3802h

Bit	R/W	Symbol	Description	Reset Value
15 :12	R/W	**tMRD**	tMRD	10b
11 : 8	R/W	**tRFC**	tRFC Time	Fh
7 : 4	R/W	**tRP**	tRP	100b
3 : 0	RW	**tRCD**	tRCD	100b

TABLE 3-39. BANK A TIMMING REGISTER #0 (MEMTIMEX0)

Bank A TIMMING Register #1 (MEMTIMEX1)

Address : C000 3804h

Bit	R/W	Symbol	Description	Reset Value
15	R/W	**ModeSet** **ModeStatus**	**(Write)**: Set 1 to set new SDRAM mode parameter. **(Read)**: Mode Setting Status 0 : Complete 1 : Busy	0b
14 : 13	R	**Reserved**	-	-
12	R	**LAT**	CAS Latency 0 : 2 Cycle 1 : 3 Cycle	1b

Bit	R/W	Symbol	Description	Reset Value
11 : 8	R/W	**tRC**	tRC	Ah
7 : 4	R/W	**tRAS**	tRAS	111b
3 : 0	RW	**tWR**	tWR	10b

TABLE 3-40. BANK A TIMMING REGISTER #1 (MEMTIMEX1)

Bank A Active Power Down Control Register (MEMACTPWDX)

Address : C000 3806h

Bit	R/W	Symbol	Description	Reset Value
15 : 9	R	**Reserved**	-	-
8	R/W	**ACTPWDEN**	Active Power Down Mode Enable 0 : Disable 1 : Enable	0b
7 : 0	RW	**ACTPERD**	Active Power Down Register	FFh

TABLE 3-41. BANK A ACTIVE POWER DOWN CONTROL REGISTER (MEMACTPWDX)

If **ACTPWDEN** is set to 1 and Memory Controller is IDLE, move to Active Power Down Mode. The value of **ACTPERD** determines movement to Active Power down mode after how long on clock the IDLE is maintained.

Bank A Refresh Control Register (MEMREFX)

Address : C000 3808h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	RW	**REFPERD**	Refresh Period (Unit BCLK/2)	0100h

TABLE 3-42. BANK A REFRESH CONTROL REGISTER (MEMREFX)

CHAPTER 4

DUAL CPU I/F

4. Dual CPU I/F

4.1 Overview

The MP2520F provides the Dual CPU I/F that allows two CPUs built in to transfer data to each other. In addition, it provides 32 16-bit Data Registers that enables it to exchange data between the ARM920 CPU and the ARM940 CPU. The Dual CPU I/F has two banks and each bank consist of 16 16-bit Registers. When a Register accesses a CPU, the Dual CPU I/F can produce an interrupt to the other CPU. Every Register can produce an interrupt and provides an Interrupt Source respectively.

The Dual CPU I/F has functions to control the 8-bit upper Address of the ARM940 and to enable the ARM920 CPU to control the ARM 940 reset.

Features

- 32 16-bit Registers
- Programmable Interrupt Generation
- Reset Generation for the ARM940

Block Diagram

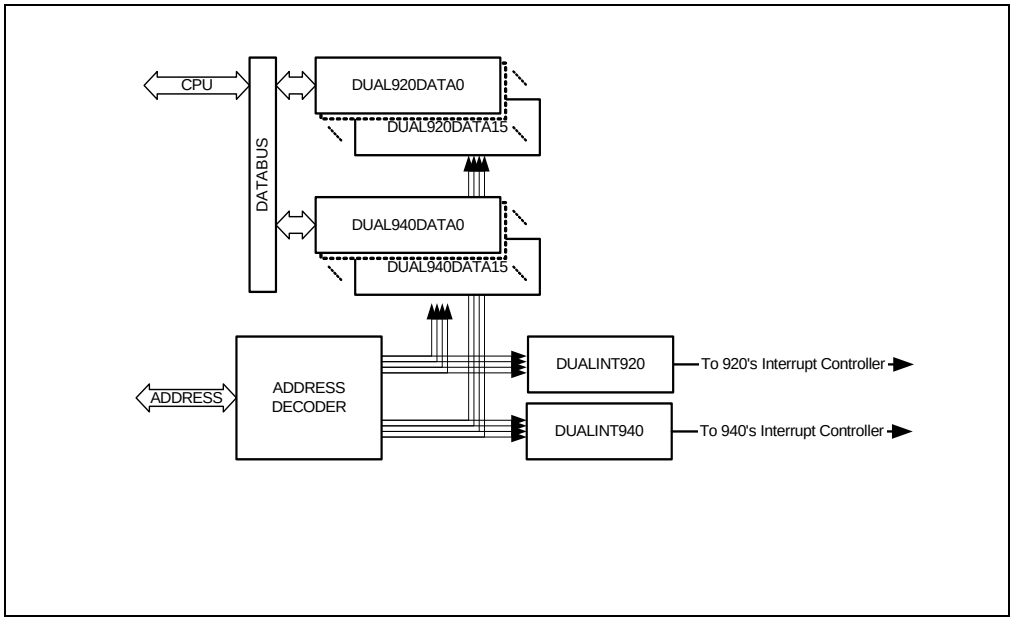


Figure 4-1. Dual CPU Block Diagram

4.2 Operation

If The ARM920 or the ARM940 executes a write operation at a Register between the Dual920Data0 and the Dual920Data15, an Interrupt occurs in the ARM920 CPU, and then the Interrupt informs the ARM920 CPU of the change of the Register value by the ARM940 CPU.

If The ARM920 or the ARM940 executes a write operation at a Register between the Dual940Data0 and the Dual940Data15, an Interrupt occurs in the ARM940 CPU.

The DUALINT920 Register generates an interrupt to each Register between DUAL920DATA0 and DUAL920DATA15.

The DUALINT940 Register generates an interrupt to each Register between DUAL940DATA0 and DUAL924DATA15.

The DUALPEND920 and the DUALPEND940 are the Interrupt Pending Registers that show the interrupt generation status. If the desired bit is set to 1, the desired pending bit is cleared.

The RST940 Bit out of the DUALCTRL940 Registers enables the ARM920 CPU to reset the ARM940. Since the RST940 bit is booted in Reset status, the bit must be set to 1 to converse in operation status before an operation.

The 940BANK out of the DUALCTRL940 Registers has the function to transform the upper address [31:24] of the 940CPU as shown below.

ARM940PhysicalAddress = (ARMCPU Address[31:24] + 940BANK) & 0xFF

The transformed address above is applied when the ARM940 CPU accesses all external Resources.

4.3 Dual-CPU Control Register LIST

Bit	R/W	Symbol	Description	Reset Value
ARM920 Data Register (DUAL920DATA0~15) *Address* : 0xC000 3B00 ~ 0xC000 3B1F				
15 : 0	R/W		Setting Data in this register generating Interrupt to ARM920T	0
ARM940 Data Register (DUAL940DATA0~15) *Address* : 0xC000 3B20 ~ 0xC000 3B3F				
15 : 0	R/W		Setting Data in this register generating Interrupt to ARM940T	0
ARM920 Interrupt Enable Register (DUALINT920) *Address* : 0xC000 3B40				
15 :0	R/W	**DUALINT920**	Controls each Register interrupt Enable of DUAL920DATA0~15 [0] : DUAL920DATA0 ~ [15] : DUAL920DATA15 0 : Disable 1 : Enable	-
ARM940 Interrupt Enable Register (DUALINT940) *Address* : 0xC000 3B42				
15 : 0	R/W	**DUALINT940**	Controls each Register interrupt Enable of DUAL940DATA0~15 [0] : DUAL920DATA0 ~ [15] : DUAL920DATA15 0 : Disable 1 : Enable	-

ARM920 Interrupt Pending Register (DUALPEND920) *Address* : 0xC000 3B44				
15 :0	R/W	**DUALPEND920**	Get each Register Interrupt Pending Bit of DUAL920DATA0~15 [0] : DUAL920DATA0 [15] : DUAL920DATA15	-
ARM920 Interrupt Pending Register (DUALPEND940) *Address* : 0xC000 3B46				
15 : 0	R/W	**DUALPEND940**	Get each Register Interrupt Pending Bit of DUAL940DATA0~15 [0] : DUAL940DATA0 [15] : DUAL940DATA15	-
ARM940 Control Register (DUALCTRL940) *Address* : 0xC000 3B48				
15 : 8	R	**Reserved**		-
7	R/W	**RST940**	Generate Reset of ARM940 [0] : Operation State [1] : Reset State	1
6 : 0	R/W	**940BANK**	Add this value to upper 8bit Address of ARM940	0

TABLE 4-1. DUAL CPU CONTROL REGISTERS LIST

CHAPTER 5

CLOCKS AND POWER MANAGER

5. CLOCKS AND POWER MANAGER

5.1 OVERVIEW

The Clocks and Power Manager block controls the power mode and the clock frequency of each module. This block has two clock sources. One is EXTCLK and the other is XTI that is a Crystal input. One of these two clock sources is multiplexed according to MP2520F operation mode and used for the input clock of the PLL. Then the clock frequency is divided on the CLKGEN block in accordance with the divider register set value. In addition, the divided clock is used for the input clock of the BCLKCTRL, PCLKCTRL and VCLKCTRL blocks, and these blocks divide the clock using the Control Register or cutoff.

The MP2520Fpower mode consists of Normal, Idle, Sleep, Deep Sleep, and Stop Modes. The CPU can execute each Power Mode by setting a PWRMODE register.

BLOCK DIAGRAM

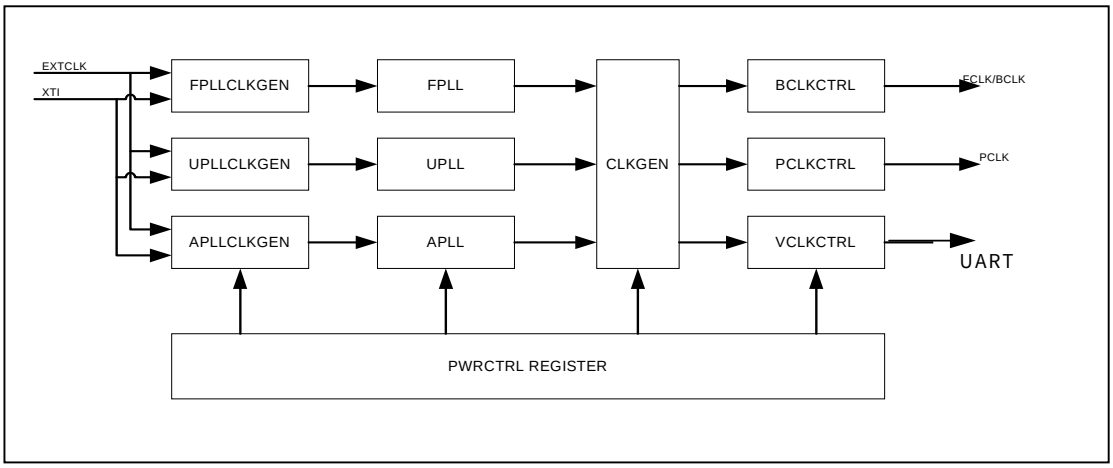


Figure 5-1. Clocks and Power Manager Block Diagram

5.2 CLOCKS AND POWER MANAGER OPERATION

MP2520F recognizes test operation mode and normal operation mode only according to the state of TEST_EN (primary input pin). In other words, when TEST_EN = 1, the test operation mode is effected. In state of TEST_EN =1, three GPIO[9:7] pins are set as OM[3:1] (i.e. input source). OM[0] is used as the pin to determine the input clock source regardless of the type of the operation mode.

5.2.1 Clocks

The external input clock sources that generate the MS2520F system clock are XTI, EXTCLK, ICLK and ABITCLK. The ICLK generates only the clock for the IMAGE Processor, and ABITCLK is exclusively used as the clock for the Audio Processor (AC97, I^2S, SPDIF in, SPDIF out) and the alternative 32.768 KHz clock for Test. Therefore, only XTI and EXTCLK are used to create various system clocks. The MS2520F has three PLLs that are FPLL, UPLL, and APLL. The types of basic System clocks are FCLK, UCLK and ACLK. A total of 8 basic clocks, including DCLK, BCLK, PCLK created by FCLK and XTI, and EXTCLK create a lot of clocks required by a variety of devices in the MS2520. However, the XTI clock is exclusively used as a 3-PLL input clock (FPLLInCLK, UPLLInCLK, APLLInCLK) and the Timer block source clock. In addition, since Deep Sleep and Stop Modes do not need to generate a clock, the operations in these modes are not executed.

PLL input clock sources and FCLKCTRL/UCLKCTRL/ACLKCTRL source clocks in accordance with MP2520F operation mode are listed below:

Normal Operation Mode : TEST_EN = 0							
OM [3:0]	OPER_ MODE	FPLL Input Clock	UPLL Input Clock	APLL Input Clock	FCLKCTRL Source Clock	UCLKCTRL Source Clock	ACLKCTRL Source Clock
XXX	NORMAL	XTI*1	XTI	XTI	FPLL Output	UPLL Output	APLL Output
XXX	NORMAL	0	0	0	EXTCLK	EXTCLK	EXTCLK
Test Operation Mode : TEST_EN = 1							
0000	TEST_FUN	XTI	XTI	XTI	FPLL Output	UPLL Output	APLL Output
0001	TEST_FUN	CLKMGRREG	XTI	XTI	CLKMGRREG	UPLL Output	APLL Output
0010	TEST_FUN	XTI	CLKMGRREG	XTI	FPLL Output	CLKMGRREG	APLL Output
0011	TEST_FUN	CLKMGRREG	CLKMGRREG	XTI	CLKMGRREG	CLKMGRREG	APLL Output
0100	TEST_FUN	XTI	XTI	CLKMGRREG	FPLL Output	UPLL Output	CLKMGRREG
0101	TEST_FUN	CLKMGRREG	XTI	CLKMGRREG	CLKMGRREG	UPLL Output	CLKMGRREG
0110	TEST_FUN	XTI	CLKMGRREG	CLKMGRREG	FPLL Output	CLKMGRREG	CLKMGRREG
0111	TEST_FUN	CLKMGRREG	CLKMGRREG	CLKMGRREG	CLKMGRREG	CLKMGRREG	CLKMGRREG
1000	ADC test	0	0	0	EXTCLK	EXTCLK	EXTCLK
1001	A920 test	0	0	0	EXTCLK	EXTCLK	EXTCLK
1010	A940 test	0	0	0	EXTCLK	EXTCLK	EXTCLK
1011	BIST test	0	0	0	EXTCLK	EXTCLK	EXTCLK
1100	SCAN test	0	0	0	EXTCLK	EXTCLK	EXTCLK
1101	NAND Tree	0	0	0	EXTCLK	EXTCLK	EXTCLK
1110	Reserved						
1111	PLL test	0	0	0	EXTCLK	EXTCLK	EXTCLK

TABLE 5-1. CLOCK SOURCE TABLE

5.2.2 Reference

FCLKin : FCLKCTRL block input clock
UCLKin : UCLKCTRL block input clock
ACLKin : ACLKCTRL block input clock
FCLKpll : FPLL output clock
UCLKpll : UPLL output clock
ACLKpll : APLL output clock
FPLLCLKin : FPLL input clock
UPLLCLKin : UPLL input clock
APLLCLKin : APLL input clock

*1 - 7.3728MHz

*2 - If CLKMGRREG[4] = 1, then FCLKin = EXTCLKin and FPLLCLKin = 0.
Otherwise, then FCLKin = FCLKpll and FPLLCLKin = EXTCLKin.
Because, if CLKMGRREG[4] = 1, then FCLKin will use EXTCLKin as its input clock instead of FCLKpll. So, FPLLCLKin should be set to 0 in order to save power.

*3 - If CLKMGRREG[5] = 1, then UCLKin = EXTCLKin and UPLLCLKin = 0.
Otherwise, then UCLKin = UCLKpll and UPLLCLKin = EXTCLKin.
Because, if CLKMGRREG[5] = 1, then UCLKin will use EXTCLKin as its input clock instead of UCLKpll. So, UPLLCLKin should be set to 0 in order to save power.

*4 - If CLKMGRREG[6] = 1, then ACLKin = EXTCLKin and APLLCLKin = 0.
Otherwise, then ACLKin = ACLKpll and APLLCLKin = EXTCLKin.
Because, if CLKMGRREG[5] = 1, then UCLKin will use EXTCLKin as its input clock instead of UCLKpll. So, APLLCLKin should be set to 0 in order to save power.

5.2.3 MP2520F Clock Tree structure

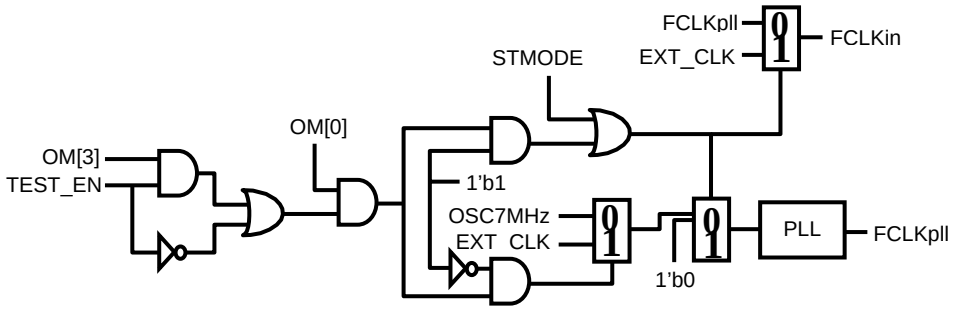


Figure 5-2. FPLLCLKGEN Block

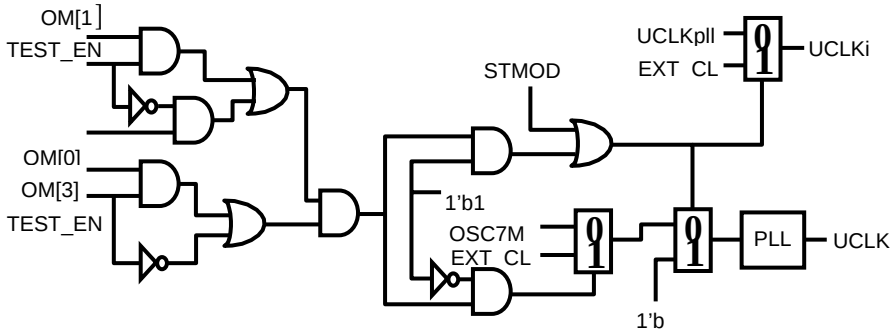


Figure 5-3. UPLLCLKGEN Block

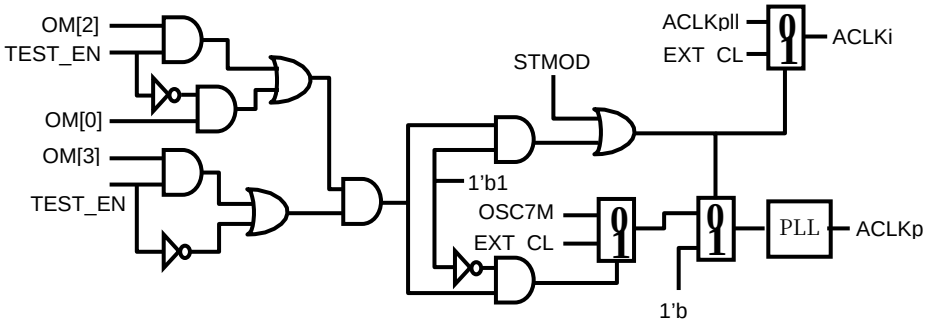


Figure 5-4. APLLCLKGEN Block

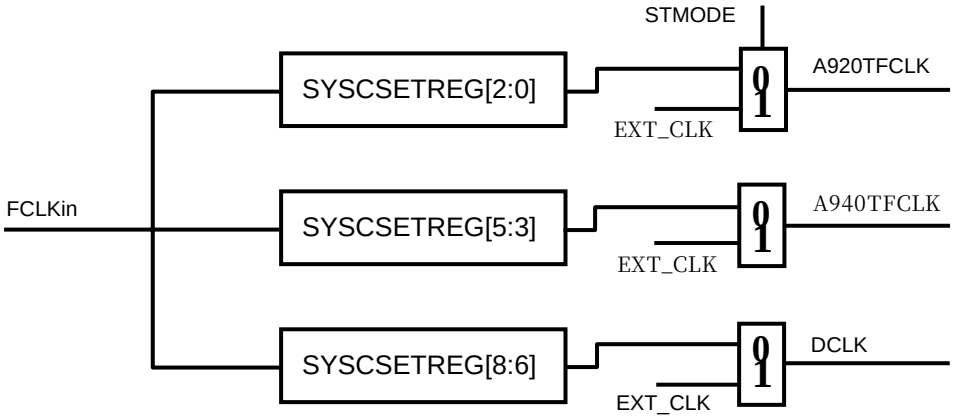


Figure 5-5. System Clock Gen

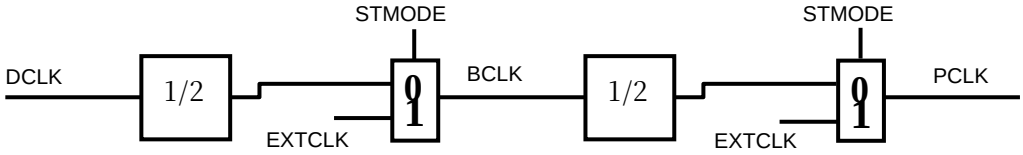


Figure 5-6. System Bus and I/O Bus Clock Generationeration

Figure 5-7. Peripheral Clock Generation

Table 5-1 is schematized as Figure 5-2, 5-3 and 5-4. The FCLK used in the ARM920T is the clock where the FCLKin is divided by SYSCSETREG[2:0] as shown in Figure 5.5. Likewise, ARM940T FCLK is divided by SYSCSETREG[5:3]. The DCLK is the clock for Memory Controller and is divided by SYSCSETREG[8:6].

The BCLK is the clock used for the system bus and the Memory and is the 2-divided clock of the DCLK. The PCLK is the clock used for a variety of peripherals and I/O buses, and is the 2-divided clock of the BCLK. The UCLK and ACLK are clocks used for a variety of peripheral blocks and use the UCLKin and the ACLKin respectively. All clocks are switched to the EXTCLK in Scan Test mode.

MP2520F has a variety of registers to generate clocks required by various devices. These registers are grossly sorted into three groups:

I. The group to be used for the control of the PLL operation itself.
II. The CSETREG (Clock Set Register) group to determine the DVO (Digital Voltage Oscillator) division ratio for the generation of clocks with frequencies by device.
III. The CLKENREG (Clock Enable Register) group to control transferring or cutting off the clocks to be used for various devices.

A. The following register groups are used to control the PLL operation itself:

1) CLKMGRREG (Clock Management Register) : The PLL operation and clock sources are determined.
[0]: The use of UPLL is determined.
[1]: The use of APLL is determined.
[2]: The source of PMRTCCLK (Power Manage & RTC Clock) is determined.
[4~6]: The sources of Three PLL input clock (FPLLInCLK, UPLLInCLK and APLLInCLK) are determined.

2) PWRMODEREG (Power Mode Register) : The PLL operation is temporarily determined.

Address : C000 0900h

Bit	R/W	Symbol	Description	Reset Value
[9]	R/W	**APLLDOWN**	APLL Power down	0x0
[8]	R/W	**UPLLDOWN**	UPLL Power down	0x0
[7:5]	R/W	**Reserved -**	-	-
[4]	R/W	**nBATTFSTOP**	ARM920T CPU STOP Mode Enable when BATT_FAULTn = '0'	0x0
[3]	R/W	**STOPMODE**	ARM920T CPU STOP Mode	0x0
[2]	R/W	**DSLEEPMODE**	ARM920T CPU DEEP SLEEP Mode, OSC7MHz Shut-down in SLEEPMode	0x0
[1]	R/W	**SLEEPMODE**	ARM920T CPU SLEEP Mode	0x0
[0]	R/W	**IDLEMODE**	ARM920T CPU IDLE Mode	0x0

TABLE 5-2. POWER MODE REGISTER (PWMODEREG)

APLLDOWN : The UPLL operation is temporary stopped. As stated before, while the CLKMGRREG is not initiated by the system reset since it is placed at the PWRMAN block where the power is supplied, the PWRMODEREG at the PWRMAN block is initialized to 0 by the system reset.
Therefore, if the CLKMGRREG[0] is set to 0 (i.e. non-use), the UPLL operation is not executed. If the PWRMODEREG[8] is set to 1 (i.e. PLL down), the UPLL operation is temporary stopped.

UPLLDOWN: The APLL operation is temporary stopped. Its function is the same with the UPLL operation above.

NBATTFSTOP : When a battery fault occurs, Stop mode is executed.

STOPMODE : When the bit is set to 1, Stop mode is executed. In the Stop mode, the power is supplied to only the SDRAM pad and the RTC block. When the GPIO power down mode register of the RTC block is set to 1, the power is also supplied to the GPIO register and the GPIO pad.

DSLEEPMODE : When the bit is set to 1, Deep Sleep mode is executed. In the Deep sleep mode, the power is supplied, but the clocks supplied to the CPU and all peripherals are cut off and the 7.3728MHz OSC clock is also locked.

SLEEPMODE : When the bit is set to 1, Sleep mode is executed. In the sleep mode, the power is supplied, but the clocks supplied to the CPU and all peripherals are cut off. Nevertheless, the 7.3728MHz OSC clock is live.

IDLEMODE : Only the clock used for the ARM920T CPU is cut off.

3) The PLLSETVREG(PLL Set Value Register) and PLLVSETREG(PLL Value Set Register) : The PLL operating frequency is determined. Further information will be provided later.

B. The CSETREG (Clock Set Register) group determines the DVO (Digital Voltage Oscillator) division ratio to generate clocks with frequencies by device.

1) **SYSCSETREG(System Clock Set Register)** : The ARM920T CPU, the ARM940T CPU, and the DCLK DVOs are determined.

Address : C000 091ch

Bit	R/W	Symbol	Description	Reset Value
[8:6]	R/W	**DCLKDIV**	DCLK Clock Generation F-PLL Divide Set Value(N-1) DCLK means Double Clock, it is used for the Memory Controller so, BCLK is DCLK * 1/2.	0x0

Bit	R/W	Symbol	Description	Reset Value
[5:3]	R/W	**A940TFDIV**	A940T FCLK Clock Generation F-PLL Divide Set Value(N-1).	0x0
[2:0]	R/W	**A920TFDIV**	A920T FCLK Clock Generation F-PLL Divide Set Value(N-1).	0x0

TABLE 5-3. SYSTEM CLOCK PLL DIVIDE VALUE SET REGISTER (SYSCSETREG)

A920TFDIV : The ARM920TFCLK clock DVO is determined. The division ratio of the FCLK can be set up to 8 in maximum.

A940TFDIV : The ARM940TFCLK clock DVO is determined. The division ratio of the FCLK can be set up to 8 in maximum.

DCLKDIV : The DCLK(Double Clock) DVO is determined. The division ratio of the FCLK can be set up to 8 in maximum.

2) **ESYSCSETREG(External System Clock Set Register)** : The external system clock DVO is determined.

Address : C000 091eh

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**ESYSCLKSRC**	External System Output Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	0x01
[13:8]	R/W	**ESYSDIV**	External System Clock Generation PLL Divide Set Value(N-1)	0x1
[7]	R/W	**ESYSPOL**	External System Clock Output Polarity Inverting Set	0x0
[6:4]	R/W	**ESYSDLY**	External System Clock Output Delay Time Value(N)	0x0
[3]	R/W	**SDRCLKPOL**	SDRAM Clock Output Polarity Inverting Set	0x0
[2:0]	R/W	**SDRCLKDLY**	SDRAM Clock Output Delay Time Value(N)	0x0

TABLE 5-4. EXTERNAL SYSTEM CLOCK TIME SET REGISTER (ESYSCSETREG)

ESYSCLKSRC : The clock sources for the generation of ESYSCLKOut , an external system clock, are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK, 00 - no clock

ESYSDIV : The division ratio of a source clock can be set up to 8 in maximum.

ESYEPOL : When the clock generated after the DVO has come out, a polarity is reversed.

ESYSDLY : When the clock generated above is finally input, the input can be delayed up to 7 ns.

SDRCLKPOL : The BCLK_SDRMA and the BCLK _SDRMB polarities are reversed. The BCLK_SDRMA and the BCLK_SDRMB are SDRAM clocks.

SDRCLKDLY : When the clock generated above is finally input, the input can be delayed up to 7 ns.

3) **UIRMCSETREG(USB /MMC Clock Set Register)** : The USB MMC clock DVO is determined.

Address : C000 0920h

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**MMCCLKSRC**	MMC/SD/MStick Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	0x0502
[13:8]	R/W	**MMCCLKDIV**	MMC/SD/MStick Clock Generation U-PLL Divide Set Value(N-1)	
[7:6]	R/W	**USBIRCLKSRC**	USB Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	
[5:0]	R/W	**USBIRDIV**	USB Clock Generation U-PLL Divide Set Value(N-1)	

TABLE 5-5. USB/MMC CLOCK GENERATION U-PLL DIVIDE VALUE SET REGISTER (UIRMCSETREG)

MMCCLKSRC : The clock sources for the generation of the MMC/SD/Memory Stick clock are determined.
11 = ACLK, 10 = UCLK,“01 = FCLK, 00 = no clock

MMCCLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

USBIRCLKSRC : The clock sources for the generation of the USB clock are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK,“00 = no clock

USBIRDIV : The division ratio of the source clock can be set up to 64 in maximum

3)**SPDIFCSETREG(SPDIF Clock Set Register)** : The SPDIF I/O clock DVO division ratio is determined.

Address : C000 092eh

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**SPDIFINSRC**	SPDIF In Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	0x0000
[13:8]	R/W	**SPDIFINDIV**	SPDIF In Controller Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**SPDIFOUTSRC**	SPDIF Out Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	
[5:0]	R/W	**SPDIFOUTDIV**	SPDIF Out Controller Clock Generation A-PLL Divide Set Value(N-1)	

TABLE 5-6. SPDIF CONTROLLER CLOCK GENERATION PLL DIVIDE VALUE SET REGISTER (SPDICSETREG)

SPDIFINSRC : The clock source used to generate the SPDIF input clock is determined.
11 = ACLK, 10 = UCLK, 01 = FCLK, 00 = ABIT_CLK

SPDIFINDIV : At most 64-division ratio of the source clock is able to be set.

SPDIFOUTSRC : The clock source used to generate the SPDIF output clock is determined.
11 = ACLK, 10 = UCLK, 01 = FCLK,"00 = ABIT_CLK

SPDIFOUTDIV : At most 64-division ratio of the source clock is able to be set.

4) **AUDICSETREG(Audio Clock Set Register)** : The AC97/ I^2S /SPDIF in/out clock DVO is determined.

Address : C000 0922h

Bit	R/W	Symbol	Description	Reset Value
[7:6]	R/W	**AUDCLKSRC**	AC97/ I^2S Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	0x0000
[5:0]	R/W	**AUDCLKDIV**	AC97/ I^2S Controller Clock Generation A-PLL Divide Set Value(N-1)	

TABLE 5-7. AUDIO CONTROLLER CLOCK GENERATION PLL DIVIDE VALUE SET (AUDICSETREG)

AUDCLKSRC : The clock sources of the generation of the AC97/ I^2S clock are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK, 00 = ABIT_CLK

AUDCLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

5) **DISPCSETREG (Display Clock Set Register)** : The DispClk1/2 clock DVO is determined.

Address : C000 0924h

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**DISPCLKSRC**	Display Clock Generation PLL Source Select 11 = APLL_CLK,"10 = UPLL_CLK, 01 = FPLL_CLK, 00 = EXTCLKin	0x0000
[13:8]	R/W	**DISPCLKDIV**	Display Clock Generation PLL Divide Set Value(N-1)	
[7]	R/W	**DISPCLKPOL**	Invert EXTCLKin polarity, when it will be selected by source clock	

TABLE 5-8. DISPLAY CLOCK GENERATION PLL DIVIDE VALUE SET REGISTER (DISPCSETREG)

DISPCLKSRC : The clock source for the generation of the DispClk1, the DispClk2 clocks are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK,"00 = EXTCLKin

DISPCLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

DISPCLKPOL : When the clock generated after the DVO has come out, polarity is reversed.

6) IMAGCSETREG(Image Clock Set Register) : The Image Processor clock DVO is determined.

Address : C000 0926h

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**IMGCLKSRC**	Image Pixel Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = no Clock	0x0000
[13:8]	R/W	IMGCLKDIV	Image Pixel Clock Generation PLL Divide Set Value(N-1)	

TABLE 5-9. IMAGE PIXEL CLOCK GENERATION PLL DIVIDE VALUE SET REGISTER (IMAGCSETREG)

IMGCLKSRC : The clock sources for the generation of the ISPInClk, the ISPOutClk, and CISOutClk DVO clocks are generated.
11 = ACLK, 10 = UCLK, 01 = FCLK, 00 = no clock

IMGCLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

7) URT0CSETREG(UART ch.0/1 Clock Set Register) UART ch.0/1 clock DVO is determined.

Address : C000 0928h

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**URT1CLKSRC**	UART1 Data TX/RX Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	0x0000
[13:8]	R/W	**URT1CLKDIV**	UART1 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**URT0CLKSRC**	UART0 Data TX/RX Clock Generation PLL Source Select	
[5:0]	R/W	**URT0CLKDIV**	UART0 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	

TABLE 5-10. UART0/1 TX/RX CLOCK GENERATION PLL DIVIDE VALUE SET REGISTER (URT0CSETREG)

URT1CLKSRC : The clock sources of the UART ch.1 clock are determined.
11 = ACLK,“10 = UCLK,“01 = FCLK,“00 = no clock

URT1CLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

URT0CLKSRC : The clock sources of the UART ch.0 clock are determined.
11 = ACLK,“10 = UCLK, 01 = FCLK, 00 = no clock

URT0CLKDIV : The division ratio of the source clock can be set up to 64 in maximum..

8) URT1CSETREG(UART ch.2/3 Clock Set Register) : The UART ch.2/3 & SSP clock DVO is determined.

Address : C000 092ah

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**URT3CLKSRC**	UART3 Data TX/RX Clock or SSP Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	0x0000
[13:8]	R/W	**URT3CLKDIV**	UART3 Data TX/RX Clock or SSP Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**URT2CLKSRC**	UART2 Data TX/RX Clock Generation PLL Source Select	
[5:0]	R/W	**URT2CLKDIV**	UART2 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	

TABLE 5-11. UART TX/RX CLOCK GENERATION PLL DIVIDE VALUE SET REGISTER (URT1CSETREG)

URT3CLKSRC : The clock sources of the generation of the UART ch.3 clock or SSP clock are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK, 00 = no clock

URT3CLKDIV : The division ratio of the source clock can be set up to 64 in maximum.

URT2CLKSRC: The clock sources of the UART ch.2 clock are determined.
11 = ACLK, 10 = UCLK, 01 = FCLK,"00 = no clock

URT2CLKDIV : The division ratio of the source clock can be set up to 64 in maximum.
The CLKENREG (Clock Enable Register) group controls transferring or cutting off the clocks to be used for various devices.

1) **PWRMODEREG(Power Mode Register)** : The output of All system clocks is temporary determined. Refer to Table 5-12. Power Mode Register (PWMODEREG).

[0:3] : The system operation modes NORMALMode, IDLEMode, SLEEPMode, DEEP_SLEEPMode, and STOPMode are determined. The IDLEMode[0] cuts off the ARM920TCPU operating clock. SLEEPMode[1], DEEP_SLEEPMode[2], and STOPMode[3] temporary cut off all system clocks and stop three PLL operations too. In addition, The DEEP_SLEEPMode and STOPMode stop even 7MHz of OSC operation. [0:2] bits are initialized to 0 only if an interrupt is triggered or the system is reset . [3] bit is initialized to 0 only if the system is reset. 2) ARM940TMODEREG (ARM940TCPU Mode Register): The outputs of the ARM940T CPU clocks are determined.

Address : C000 092ch

Bit	R/W	Symbol	Description	Reset Value
[0]	R/W	**A940TIDLE**	ARM940T CPU IDLE Mode - this bit should be written by the ARM940T CPU only	0x0

TABLE 5-12. ARM940T CPU POWER MANAGE MODE REGISTER (A940TMODEREG)

A940TIDLE : The outputs of ARM940TFCLK and ARM940TBCLK are determined. However, this register is set by only the ARM940TCPU. If the ARM940TNFIQ or ARM940TNIQ interrupt is triggered, or the system is reset, this register is reset to 0.

3) **SYSCLKENREG (System Clock Enable Register)** : The outputs of the system device clocksiare determined.

Address : C000 0904h

Bit	R/W	Symbol	Description	Reset Value
[15]	R	**Reserved**	-	-
[14]	R/W	**ESYSCLK**	External System Clock	0x1
[13]	R/W	**ADCCLK**	ADC Block	0x1
[12]	R/W	**PWMCLK**	Pulse Width Modulator	0x1
[11]	R/W	**Reserved**	-	-
[10]	R/W	**Reserved**	-	-
[9]	R/W	**DMACLK**	DMA Controller	0x1
[8]	R/W	**DMACLK_GOFF**	DMA Controller Gated Clock Disable bit	0x1
[7]	R/W	**TIMERCLK**	Timer Block Clock	0x1
[6]	R/W	**PERICLK**	Other Co-processor device	0x1
[5]	R/W	**GPIOCLK**	GPIO Controller	0x1
[4]	R/W	**PERICLK_GOFF**	PERICLK Dynamic Clock Control Disable	0x1
[3]	R/W	**MEMCCLK**	Memory Bank C Controller	0x1
[2]	R/W	**Reserved**	-	-
[1]	R/W	**MEMACLK**	Memory Bank A Controller	0x1
[0]	R/W	**A940TCLK**	A940T CPU A940TFCLK, A940TBCLK	0x1

TABLE 5-13. SYSTEM CLOCK ENABLE REGISTER (SYSCLKENGEG)

A940TCLK : The outputs of the ARM940TFCLK and the ARM940TBCLK are determined. This register is determined by the ARM940T main CPU. In other words, if this bit is set to 1, the CPU is not used. Only if the system is reset, is this bit initialized.

MEMACLK : The outputs of DCLK_MEMA, BCLK_MEMA, and BCLK_SDRMA are determined. Here, the DCLK_MEMA, the BCLK_MEMA, and the BCLK_SDRMA are the memory controller A clock. Only if the system is reset, this bit is initialized. MEMCCLK : The output of DCLK_MEMB, BCLK_MEMB and BCLK_SDRMB are determined, Here, the DCLK_MEMB, the BCLK_MEMB and the BCLK_SDRMB are the memory controller B clock. Only if the system is reset, is this bit initialized.

PERICLK_GOFF : The outputs of DCLK_MEMC and BCLK_MEMC are determined. Here, DCLK_MEMC and

BCLK_MEMC are the memory controller C clock. Only if the system is reset, this bit is initialized. GPIOCLK : The output of PCLK_GPIO (GPIO clock) Is determined. Only if the system is reset, is this bit initialized.

PERICLK : The output of PCLK_CORP0/1 is determined. Here, the PCLK_CORP0/1 is the clock used to read or write the registers of video processors, graphic processors, MPEG I/Fs, and various Co-processors. It is important that the co-processor devices using PCLK for only the CPU write/read operation have to be connected to this PCLK_CORP0/1. Therefore, devices using PCLK for only the PCLK operation itself must not use this clock, but use their own clocks. PCLK_CORP0 is generated when the CPU executes the writing operation, not reading operation. This clock can be connected to SCALE, ROTATE, SP (Stream Processor), HUFFMAN, PREDICTION & Q, DCT/IDCT, Q-PEL, GMC, FORMAT CONVERTER, RVLD, DEBLOCKING, MEC, MEF, DVD CSS, IDE I/F, AND MPEG I/F devices. PCLK_CORP1 is generated when the CPU executes the write/read operation. This clock can be connected to DISPLAY, MP/MC, REFWRITE, and IMAGE devices.

TIMERCLK : The output of ESYSCLKOut (external system clock) is determined. The Timer CLK is used for only the 7MHz Oscillator or EXTCLKin (if selected as the primary input clock).

DMACLK_GOFF : The gating of every clock needed for the sub-blocks on DMA channels 0~15 is determined. In other words, BCLK_DMA0, BCLK_DMA1, BCLK_DMA2 and BCLK_DMA3 clocks to be provided in the DMA channels 0~15 are dynamically gated according to the operation of each channel, but this bit controls these clocks via the dynamic gating, not static gating. If the bit is set to 1, the dynamic gating function is disabled.

DMACLK : The outputs of BCLK_DMAT, BCLK_DMA0, BCLK_DMA1, BCLK_DMA2, and BCLK_DMA3 (DMA clocks) are determined. This bit is initialized to 1 only if the system is reset. The BCLK_DMAT is the clock to be provided to the DMA top block and to all registers on DMA channels where the CPU executes the 'write' operation. The BCLK_DMA0, the BCLK_DMA1, the BCLK_DMA_2 and the BCLK_DMA3 clocks are used for channesl 0~3, channels 4~7, channels 8~11 and channels 12~15 separately. If any channel out of the corresponding channels is not executed, the DMA requests the clock gate and then the clock is cut off.

PWMCLK : The output of PCLK_PWM that is PWM (Power Width Modulator clock) is determined.

ADCCLK : The output of PCLK_ADC (ADC clock) is determined.

ESYSCLK : The output of the ESYSCLKOut (external system clock) is determined. The bit is initialized to 1 only if the system is reset. The other way to cut off ESYSCLKOut is to set ESYSCSETREG[15:14] to 00.

4) COMCLKENREG (Communication Clock Enable Register): The outputs of the clocks for communication devices are determined.

Address : C000 0908h

Bit	R/W	Symbol	Description	Reset Value
[9]	R/W	**SSPCLK**	SSP/SDI Block Clock	0x1
[8]	R/W	**I^2C CLK**	I^2C Controller	0x1
[7]	R/W	**UART3CLK**	UART3	0x1
[6]	R/W	**UART2CLK**	UART2	0x1
[5]	R/W	**UART1CLK**	UART1	0x1
[4]	R/W	**UART0CLK**	UART0	0x1
[3]	R/W	**OWMCLK**	OWM Clock	0x1
[2]	R/W	**Reserved**	-	-
[1]	R/W	**UDCCLK**	USB Device Controller Clock	0x1
[0]	R/W	**UHCCLK**	USB Host Processor Clock	0x1

TABLE 5-14. COMMUNICATION DEVICE CLOCK ENABLE REGISTER (COMCLKENREG)

UHCCLK : The outputs of UCLK_UHC and PCLK_UHC (USB host controller clocks) are determined.

UDCCLK : The outputs of UCLK_UDC and PCLK_UDC (USB device controller clocks) are determined.

UART0CLK : The outputs of UART0_CLK and PCLK_UT0 (UART ch.0 device clocks) are determined.

UART1CLK : The outputs of UART1_CLK and PCLK_UT1 (UART ch.1 device clocks) are determined.

UART2CLK : The outputs of UART2_CLK and PCLK_UT2 (UART ch.2 device clock) are determined.

UART3CLK: The output of UART3_CLK and PCLK_UT3 (UART ch.3 device clock) are determined.

I^2C CLK : The out of PCLK_ I^2C (I^2C device clock) is determined.

SSPCLK : The output of PCLK_SSP (SSP/SDI device clock) is determined.

5) VGCLKENREG (Video & Graphic Clock Enable Register): The outputs of clocks for Video & Graphic devices are

determined.

Address : C000 090ah

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**DBLKCLK**	Deblock Enbale	0x1
[14]	R/W	**MPGIFCLK**	MPEG I/F Block	0x1
[13]	R/W	**DECSSCLK**	DVD DeCSS Block	0x1
[12]	R/W	**MECLK**	Motion Estimation Block	0x1
[11]	R/W	**REFWCLK**	RefWrite Block	0x1
[10]	R/W	**RVLDCLK**	RVLD Block	0x1
[9]	R/W	**QGMCCLK**	Q-Pel & GMC	0x1
[8]	R/W	**MPMCCLK**	MP/MC	0x1
[7]	R/W	**PDFCLK**	PRED/Q & DCT & Format Converter	0x1
[6]	R/W	**HUFFCLK**	Stream Processor & Huffman block	0x1
[5]	R/W	**VPCLKGOFF**	Video Processor Gated Clock Disable bit (PRED/Q, DCT, MP/MC, RefWrite, Q-Pel, GMC, Deblocking, MEC, MEF)	0x1
[4]	R/W	**VPTOPCLK**	Video Processor Top block	0x1
[3]	R/W	**ISPCLK**	Image Processor	0x1
[2]	R/W	**GRPCLK**	Graphic & Rotation Processor	0x1
[1]	R/W	**SCALECLK**	Scale Processor	0x1
[0]	R/W	**DISPCLK**	Display Controller	0x1

TABLE 5-15. VIDEO & GRAPHIC DEVICE CLOCK ENABLE REGISTER (VGCLKENREG)

DISPCLK : The outputs of DISP_CLK0, DISP_CLK1 and BCLK_DISP (Display controller clocks) are determined.

SCALECLK : The output of BCLK_SCALE (Scale controller clock) is determined.

GRPCLK : The output of BCLK_GRPH (Graphics & Rotation block clock) is determined.

ISPCLK : The outputs of IMAGE_CLK0 and IMAGE_CLK1 (Image Processor clocks) are determined.

VPTOPCLK : This bit controls the clocks for all Video Processor blocks and determines the output of BCLK_MPEG (Video Processor top block clock) at the same time.

VPCLKGOFF : This bit determines the gating of the clocks of all sub-processors in the Video Processor. In other words, the clocks is to be provided to various video sub-processors that are dynamically gated according to various sub-processor operation, but this bit controls these clocks through static gating, not dynamic gating. When this bit is set to 1, the dynamic gating function is disabled.

HUFFCLK : The output of BCLK_HUFF (SP & HUFFMAN clock) is determined.

PDFCLK : The outputs of BCLK_PREQ, BCLK_ DCT, and BCLK_FMTC (PREDICTION/Q, DCT/IDCT, FORMAT CONVERTER clocks) are determined.

MPMCCLK : The output of BCLK_MPMC (MP/MC and REFWRITE clock) is determined.

QGMCCLK : The output of BCLK_QGMC (Q-PEL and GMC clock) is determined.

RVLDCLK : The output of BCLK_RVLD (RVLD clock) is determined.

REFWCLK : The output of BCLK_DVLCK (DEBLOCKING clock) is determined.

MECLK : The outputs of BCLK_MEF and BCLK_MEC (MEC and MEF clocks) are determined.

DECSSCLK : The output of BCLK_CSS (DVD CSS clock) is determined.

MPGIFCLK : The output of BCLK_MPGIF (MPEG I/F clock) is determined.

DBLKCLK : The output of the Deblock clock is determined.

6) ASCLKENREG (Audio & Storage Clock Enable Register) : The output of the Audio & Storage device clocks is determined.

Address : C000 090ch

Bit	R/W	Symbol	Description	Reset Value
[13]	R/W	**CDROMCLK**	CD-ROM Decoder Block	0x1
[12]	R/W	**IDECLK**	IDE I/F Block	0x1
[11]	R/W	**Reserved**	-	-
[10]	R/W	**Reserved**	-	-
[9]	R/W	**MSTICKCLK**	Memory Stick Controller Clock	0x1
[8]	R/W	**MMCCLK**	MMC/SD Controller Clock	0x1
[7]	R/W	**Reserved**	-	-
[6]	R/W	**Reserved**	-	-
[5]	R/W	**Reserved**	-	-
[4]	R/W	**Reserved**	-	-
[3]	R/W	**SPDIFOCLK**	SPDIF Output Clock	0x1
[2]	R/W	**SPDIFICLK**	SPDIF Input Clock	0x1
[1]	R/W	**I^2S CLK**	I^2S Controller Clock	0x1
[0]	R/W	AC97**CLK**	AC97 Controller Clock	0x1

TABLE 5-16. AUDIO & STORAGE DEVICE CLOCK ENABLE REGISTER (ASCLKENREG)

AC97CLK : The outputs of ACLK_97and PCLK_ AC97 (AC97 controller clock) are determined.

I^2S CLK : The outputs of ACLK_ I^2S, QCLK_ I^2S and PCLK_ I^2S (I^2S controller clock) are determined.

SPDIFICLK: The outputs of ACLK_SPDIFI, QCLK_SPDIFI, and PCLK_SPDIFI (SPDIF INPUT block clocks) are determined.

SPDIFOCLK : The outputs of ACLK_SPDIFO, QCLK_SPDIFO, and PCLK_SPDIFO (SPDIF OUTPUT clock) are determined. This bit is initialized to 0 only if the system is reset MMCCLK: The output of PCLK_MMC (MMC/SD controller clock) is determined.

MSTICKCLK : The outputs of MCLK_STICK and PCLK_STICK (Memory Stick clock) are determined.

IDECLK : The outputs of BCLK_IDEIF (IDE I/F clock) are determined.

CDROMCLK : The output of PCLK_CDROM (CDROM DECODER clock) is determined.

The contents of the registers corresponding to each clock are summarized in the following CLOCK LIST table.

Clock Name	Applied Block	Clock Source	Control Reg.
A920TFCLK	ARM920T CPU	FCLK, SYSCSETREG[2:0]	PWRMODEREG[3:0]
A940TFCLK	ARM940T CPU	FCLK, SYSCSETREG[5:3]	SYSCLKENREG[0]
A920TBCLK	ARM920T CPU, Local Bus Master	FCLK, SYSCSETREG[8:6]	PWRMODEREG[3:0]
A940TBCLK	ARM940T CPU, Local Bus Master	same as above	SYSCLKENREG[0]
DCLK_MEMA	Memory Controller A	same as above, BCLK * 2	SYSCLKENREG[1]
BCLK_MEMA	Memory Controller A	same as above	SYSCLKENREG[1]
DCLK_MEMC	Memory Controller C	same as above, BCLK * 2	SYSCLKENREG[3]
BCLK_MEMC	Memory Controller C	same as above	SYSCLKENREG[3]
BCLK_SDRMA	Ext. SDRAM Device	BCLK_MEMA, ESYSCSETREG[3:0]	SYSCLKENREG[1]
BCLK_SDRMB	Ext. SDRAM Device	BCLK_MEMB, ESYSCSETREG[3:0]	SYSCLKENREG[2]
BCLK_DMAT	DMA Controller Top	FCLK, SYSCSETREG[8:6]	SYSCLKENREG[9]
BCLK_DMA0	DMA Controller[3:0]	FCLK, SYSCSETREG[8:6]	SYSCLKENREG[9]
BCLK_DMA1	DMA Controller[7:4]	FCLK, SYSCSETREG[8:6]	SYSCLKENREG[9]
BCLK_DMA2	DMA Controller[11:8]	FCLK, SYSCSETREG[8:6]	SYSCLKENREG[9]
BCLK_DMA3	DMA Controller[15:12]	FCLK, SYSCSETREG[8:6]	SYSCLKENREG[9]
BCLK_DISP	Display Controller	FCLK, SYSCSETREG[8:6]	VGCLKENREG[0]
BCLK_SCALE	Scale Processor	same as above	VGCLKENREG[1]
BCLK_GRPH	Graphic, Rotate Processor	same as above	VGCLKENREG[2]
BCLK_MPEG	Whole Video Processor	same as above	VGCLKENREG[4]
BCLK_HUFF	SP, Huffman	same as above	VGCLKENREG[6]
BCLK_PREQ	Pred/Q	same as above	VGCLKENREG[7]
BCLK_DCT	DCT/IDCT	same as above	VGCLKENREG[7]
BCLK_FMTC	Format Converter	same as above	VGCLKENREG[7]
BCLK_MPMC	MP/MC, RefWrite	same as above	VGCLKENREG[8]
BCLK_QGMC	Q-PEL, GMC	same as above	VGCLKENREG[9]

Clock Name	Applied Block	Clock Source	Control Reg.
BCLK_QGMC	Q-PEL, GMC	same as above	VGCLKENREG[9]
BCLK_RVLD	RVLD Decoder	same as above	VGCLKENREG[10]
BCLK_DBLCK	Deblocking Processor	same as above	VGCLKENREG[11]
BCLK_MEC	MEC Processor	same as above	VGCLKENREG[12]
BCLK_MEF	MEF Processor	same as above	VGCLKENREG[12]
BCLK_CSS	DVD CSS Block	same as above	VGCLKENREG[13]
BCLK_MPGIF	MPEG I/F Block	same as above	VGCLKENREG[14]
BCLK_IDEIF	IDE Controller Block	same as above	ASCLKENREG[12]
PCLK_IOC	I/O Master, Interrupt Cont	BCLK * 1/2	-
PCLK_PWRMAN	PWRMAN Block	same as above	-
PCLK_PERI	Timer, RTC, MEMA/B/C	same as above	-
PCLK_GPIO	GPIO Block	same as above	SYSCLKENREG[5]
PCLK_CORP0	no clock for CPU read : SCALE, GRPH, ROTATE, SP, HUFFMAN, PRED/Q, DCT, Q-PEL, GMC, Format Converter, RVLD, Deblocking, MEC/F, CSS, IDE, MPEG I/F, DMA	same as above	SYSCLKENREG[6]
PCLK_CORP1	need clock for CPU read : Display, MP, MC, RefWrite, Image	same as above	SYSCLKENREG[6]
PCLK_PWM	Power Width Modulator	same as above	SYSCLKENREG[12]
PCLK_ADC	Touch Panel ADC	same as above	SYSCLKENREG[13]
PCLK_UHC	USB Host Controller	same as above	COMCLKENREG[0]
PCLK_UDC	USB Device Controller	same as above	COMCLKENREG[1]
PCLK_UT0	UART Ch0	same as above	COMCLKENREG[4]]
PCLK_UT1	UART Ch1	same as above	COMCLKENREG[5]]
PCLK_UT2	UART Ch2	same as above	COMCLKENREG[6]]
PCLK_UT3	UART Ch3	same as above	COMCLKENREG[7]
PCLK_ I^2C	I^2C Device	same as above	COMCLKENREG[8]
PCLK_SSP	SSP/SDI Device	same as above	COMCLKENREG[9]
PCLK_ AC97	AC97 Controller	same as above	ASCLKENREG[0]
Clock Name	**Applied Block**	**Clock Source**	**Control Reg.**

PCLK_ I2S	I2S Controller	same as above	ASCLKENREG[1]
PCLK_SPDIFI	SPDIF In Controller	same as above	ASCLKENREG[2]
PCLK_SPDIFO	SPDIF In Controller	same as above	ASCLKENREG[3]
PCLK_MMC	MMC, SD Controller	same as above	ASCLKENREG[8]
PCLK_STICK	Memory Stick Controller	same as above	ASCLKENREG[9]
PCLK_CDROM	CD_ROM Decoder	same as above	ASCLKENREG[13]

(Italic letters above mean dynamic gated clocks.)

TABLE 5-17. CLOCK LIST TABLE.

For MP2520F, in Sleep Mode, all PCLK source clocks are down, but only the 7.3728 MHz Oscillator operates. In DEEP_SLEEP Mode, the 7.3728 MHz Oscillator is also down. In STOP Mode, the RTC, SDRAM control I/O pad, and GPIO I/O pad(when PWRMGRREG[0] = 1) are supplied with live power, but the other blocks are powered off.

In SLEEP Mode, DEEP_SLEEP Mode and STOP Mode, all clocks are shut down. In these modes, external events transferred to the GPIO, the ADC and the UDC indirectly wake up the CPU only by means of the GPIOIn pin of the RTC because the RTC is the unique device that can always operate in any operation mode using 32.768 KHz Oscillator Clock.

Even if SLEEP Mode or DEEP_SLEEP Mode is converted into Normal mode, the contents of the control register controlling all clocks are never changed. If, however, Stop mode is converted into Normal mode, the system is reset and all registers are initialized.

PCLK_CORP0/1 and PCLK_PERI are dynamic gated clocks and are created by the write/read signal of the CPU.

< Various Clock Source List >

Clock Name	Application Block	Clock Source	Control Reg.
TCLK_TIMER	Timer	Oscillator Clock(7.3728MHz)	SYSCLKENREG[7]
UCLK_UHC	USB Host Controller	UCLK, UIRMCSETREG[5:0]	COMCLKENREG[0]
UCLK_UDC	USB Device Controller	same as above	COMCLKENREG[1]
UART0_CLK	UART Ch0	FCLK, UCLK, ACLK URT0CSETREG[7:0]	COMCLKENREG[4]]
UART1_CLK	UART Ch1	URT0CSETREG[15:8]	COMCLKENREG[5]]
UART2_CLK	UART Ch2	URT1CSETREG[7:0]	COMCLKENREG[6]]
UART3_CLK	UART Ch3	URT1CSETREG[15:8]	COMCLKENREG[7]
Clock Name	**Application Block**	**Clock Source**	**Control Reg.**

SSP_CLK	SSP 20MHz clock	URT1CSETREG[15:8]	COMCLKENREG[9]
DispClk1, DispClk2	Display Controller	FCLK, UCLK, ACLK, EXT_CLK DISPCSETREG[7:0]	VGCLKENREG[0]
ISPInClk, ISPOutClk, CISOutClk	Image Processor	FCLK, UCLK, ACLK, ICLKin, BCLK, IMAGCSETREG[15:0]	VGCLKENREG[3]
ACLK_ AC97	AC97 Controller	FCLK, UCLK, ACLK, AUDIO_CLK AUDICSETREG[7:0]	ASCLKENREG[0]
ACLK_I2S	I2S Controller	same as above	ASCLKENREG[1]
QCLK_I2S	I2S Controller	ACLK_I2S * 1/4	ASCLKENREG[1]
ACLK_SPDIFI	SPDIF IN Controller	FCLK, UCLK, ACLK, AUDIO_CLK AUDICSETREG[15:8]	ASCLKENREG[2]
ACLK_SPDIFO	SPDIF OUT Controller	same as above	ASCLKENREG[3]
QCLK_SPDIFI	SPDIF In Controller	ACLK_SPDIF * 1/4	ASCLKENREG[2]
QCLK_SPDIFO	SPDIF In Controller	ACLK_SPDIF * 1/4	ASCLKENREG[3]
MCLK_STICK	Memory Stick Controller	UCLK, UIRMCSETREG[13:8]	ASCLKENREG[9]
ESYSCLKOut	External System Clock	FCLK, UCLK, ACLK ESYSCSETREG[15:4]	SYSCLKENREG[14]

TABLE 5-18. VARIOUS CLOCK SOURCE LIST

5.2.4 Power Modes

In Normal Mode, the power is supplied to all clocks, and the clock control register controls a variety of clocks.

In Idle Mode, the power is supplied to all clocks and only the clocks of the ARM920T and ARM940T are cut off. Since, however, interrupt requests are always being monitored, the MP2520F can quickly return to Normal Mode if an interrupt occurs.

In SLEEP Mode and DEEP_SLEEP Mode, all source clocks of FCLK and BCLK are shut down. In these modes, internal and external events indirectly wake up the CPU by means of the RTC. There are six types of events to wake up the CPU. Four kinds of the external events are EXTIN0, EXTIN1, nBATTF, and GPIOIn that is transferred via GPIO port. In addition, two kinds of internal events are the alarm function in the RTC and the event by one second production. If these events generate the RTC interrupt, each of the interrupt enable bits [15:9] of the RTCSTREG (RTC Status Register) has to be set. The CPU, waked up by the RTC interrupt, can know the event generating the interrupt by reading the RTCSTREG [7:1].

In Stop Mode, the power is supplied to only the RTC block and the PAD related to SDRAM. At this time, all clocks,

except for the RTC clock, are shut down. If, however, the registers in RTS are set, the GPIO Alive clock and GPIO PAD can be supplied with power. In Stop Mode, internal and external events wake up the CPU by the reset of the RTC. Five kinds of events can wake up the CPU via RTC in Stop Mode. 4 kinds of internal events are EXTIN0, EXTIN1, nBATTF, and GPIOIn transferred via the GPIO port. The internal event is generated by the alarm function in the RTC. The CPU, waked up by the reset, can know the event generating the reset by reading the RTCSTREG (Reset Status Register). RSTSTREG[7:0] memorizes 8 events, and they are nRESET and WDT resets generated in power-on status in addition to the 6 events stated before.

When IDLEMode or SLEEPMode is converted into NORMAL Mode, only the PWRMODEREG value is changed and the other registers keep the previous values. If the CPU is waked up in STOP Mode or by any reset, every register is initialized. A matter to be attended is that all registers in the RTC are initialized only by the power-on reset (PORRSTn), not nRESET, WDT reset, or RTC reset.

The PWRMODE register setting to convert each Power Mode will be further explained in the Register map.

The summary for the MP2520 Power Mode is listed in the following table

	NORMALMode	IDLEMode	SLEEP/DEEP SLEEP Mode	STOPMode
Core Power	ON	ON	ON	OFF*1
Alive Power	ON	ON	ON	ON*2
RTC Power	ON	ON	ON	ON
OSC7MHz	Alive	Alive	PWRMODEREG*3	Dead
FPLL	Alive	Alive	Dead	Dead
UPLL	CLKMGRREG	CLKMGRREG	Dead	Dead
APLL	CLKMGRREG	CLKMGRREG	Dead	Dead
FCLK	Up to 266MHz	None	None	None
BCLK	Up to 133MHz	Up to 133MHz	None	None
PCLK	Up to 66MHz	Up to 66MHz	None	None
Power-On Reset	Depends on nPORSEL*4	N/A	N/A	N/A
nRESET	Reset	Reset	Reset	N/A*5
WDT Reset	Reset	Reset	N/A*5	N/A
Ext. Event	ITC's Interrupt	ITC's Interrupt	RTC's Interrupt	RTC's RESET
RTC Event	ITC's Interrupt	ITC's Interrupt	RTC's Interrupt	RTC's RESET

TABLE 5-19. SYSTEM OPERATION MODE

Reference :

*1 - Core Power & I/O Power are controlled by the POWEROFF signal(RTC).

*2 - Live Power is used for only SDRAM_MA and wake up control pin.

*3 - PWRMODEREG[2] determines whether the Oscillator should be dead or not.

*4 - Power-On Reset occurs only when nPORSEL = 0 and POWER changes from 'OFF' to 'ON'.

*5 - nRESET and WDT reset are valid only in 'POWER-ON' state.

STOPMode could be used to save power when Battery voltage is low.

Power Mode Sequence Table

Description of Action	Normal	Idle	Sleep	Deep Sleep	Stop	Freq Change
Software writes bits in RSTCTRLREG	X					
Software clears bits in RSTSTREG	X					
Software writes bits in BOOTCTRLREG	X					
Software writes bits in LOCKTIMEREG	X					
Software writes bits in RSTTIMEREG	X					
Software writes bits in EXTCTRLREG	X					
Software writes bits in PWRMGRREG	X					
Software writes bits in PWRMODEREG	X					
Software writes bits in FPLLSETVREG						X
Set bits in CLKCHGSTREG						X
Wait for CPU to complete the current operation		X	X	X	X	X
Wait for Memory Controller to complete the current operation			X	X	X	X
Wait for IO Master Controller to complete the current operation			X	X	X	X
Wait for Display/Image Processor to complete the current operation			X	X	X	X
The Memory Controller places SDRAMs in Self Refresh			X	X	X	X
SLEEPMode/DSLEEPMode signal is generated			X	X		
STOPMode signal is generated					X	
OPERPWROn signal is negated					X	
IntOperPwrOn signal is negated					X	
POWEROFF signal is generated					X	
CPU clock is disabled		X	X	X	X	X
PLL is disabled			X	X	X	X
7MHz Oscillator is disabled				X	X	
PWRRGLTOn signal is de-initialized					X	
Core supply power is cut off					X	
GPIO supply power is cut off based on the state of PWRMGRREG[0] bit					X	
Wake-up source or Interrupt is received		X	X	X	X	
PWRRGLTOn signal is reasserted					X	

Description of Action	Normal	Idle	Sleep	Deep Sleep	Stop	Freq Change
GPIO supply power is restored					X	
SLEEPMode/DSLEEPMode signal is negated			X	X		
STOPMode signal is negated					X	
OPERPWROn signal is reinitiated					X	
IntOperPwrOn signal is reinitiated					X	
POWEROFF signal is negated					X	
Core supply power is restored					X	
GRESETOut is initiated					X	
Clear bits in PWRMODEREG		X	X	X	X	
Clear bits in CLKCHGSTREG						X
7MHz Oscillator is enabled				X	X	
Wait for 7MHz Oscillator stabilization				X	X	
Enable PLL with new frequency			X	X	X	X
Wait for PLL stabilization			X	X	X	X
CPU clock is enabled			X	X	X	X
Memory Controller clock is enabled			X	X	X	X
GRESETOut is de-initiated					X	
Recover SDRAM from self-refresh			X	X	X	X

TABLE 5-20. POWER MODE SEQUENCE TABLE

5.2.5 Resets

The MP2520F has 4 types of Reset, which are nPORRST, nRESET, WDT reset, and RTC reset.

Out of these, the nPORRST (power-on reset) has the highest priority. If the supplied voltage of the MP2520F is higher than the required level (por_18 cell lib. detection voltage), this bit is set ito 1. Otherwise, it is set to 0. An Internal POP Cell operates when the PORSEL pin is set to 0. Therefore, if any trouble occurs in the operation of the por_18 cell lib, it can be fixed by setting the PORSEL pin to 1 and attaching the power-on reset circuit from the outside via the nRESET pin. As stated before, all registers in the RTC are never initialized, but this nPORRST is the unique exception. However, even in this case, RTCCNTREG (RTC real time counter) is not initialized absolutely.

Next, the reset with the second highest priority is nRESET. The reset is entered to the RTC block by means of the primary input pin of the MP2520F. The reset to be used in the chip test mode (STMODE) is only this nRESET.
The RTC reset is generated by external events in STOP Mode. Four types of external events are EXTIN0, EXTIN1, nBATTF, and GPIOIn. Out of these, the GPIOIn is an internal signal, and the others are primary input pins. In NORMAL Mode, these events produce the RTC interrupt.

The WDT reset is generated by the timer. When S/W is not working normally, it is generated by time out. For further information, refer to “Timer Block.”

Since nRESET and WDT reset are impressed when the MP2520F is power-on, they do not keep the reset state for a long time unlike nPORRST and RTC reset. In other words, nRESET loads the system reset while the reset is impressed from the outside, and WDT reset loads the system reset for only 60 s.

5.3 Clocks and Power REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
Power Mode Register (PWMODEREG) ***Address : C000 0900h***				
[9]	R/W	**APLLDOWN**	APLL Power down	0x0
[8]	R/W	**UPLLDOWN**	UPLL Power down	0x0
[7:5]	R/W	**Reserved**	-	-
[4]	R/W	**nBATTFSTOP**	ARM920T CPU STOP Mode Enable when BATT_FAULTn = '0'	0x0
[3]	R/W	**STOPMODE**	ARM920T CPU STOP Mode	0x0
[2]	R/W	**DSLEEPMODE**	ARM920T CPU DEEP SLEEP Mode, OSC7MHz Shut-down in SLEEPMode	0x0
[1]	R/W	**SLEEPMODE**	ARM920T CPU SLEEP Mode	0x0
[0]	R/W	**IDLEMODE**	ARM920T CPU IDLE Mode	0x0
Clock Change Status Register (CLKCHGSTREG) ***Address : C000 0902h***				
[5]	R/W	**APLLCHG**	ACLK PLL Clock Blocking Status due to Clock Change Operation	0x0
[4]	R/W	**UPLLCHG**	UCLK PLL Clock Blocking Status due to Clock Change Operation	0x0
[3]	R/W	**Reserved**	-	-
[2]	R/W	**APLLCHGST**	ACLK PLL Clock Change Status, maintain '1' until actual change begins	0x0
[1]	R/W	**UPLLCHGST**	UCLK PLL Clock Change Status, maintain '1' until actual change begins	0x0
[0]	R/W	**FPLLCHGST**	FCLK PLL Clock Change Status, maintain '1' until actual change begins	0x0
System Clock Enable Register (SYSCLKENREG) ***Address : C000 0904h***				
[15]	R	**Reserved**	-	-
[14]	R/W	**ESYSCLK**	External System Clock => ESYSCLKOut	0x1
[13]	R/W	**ADCCLK**	ADC Block => PCLK_ADC	0x1
[12]	R/W	**PWMCLK**	Pulse Width Modulator => PCLK_PWM	0x1
[11]	R/W	**Reserved**	-	-
[10]	R/W	**FASTIOCLK**	FASTIO => PCLK_FAST-	0x1
[9]	R/W	**DMACLK**	DMA Controller => BCLK_DMAT, BCLK_DMA0, BCLK_DMA1,BCLK_ DMA2, BCLK_DMA3	0x1
[8]	-	**Reserved**	-	-
[7]	R/W	**TIMERCLK**	Timer Block Clock => TCLK_TIMER(7.3728MHz)	0x1

Bit	R/W	Symbol	Description	Reset Value
[6]	R/W	**PERICLK**	Other Co-processor device => PCLK_CORP0, PCLK_CORP1	0x1
[5]	R/W	**GPIOCLK**	GPIO Controller PCLK_GPIO	0x1
[4]	-	**Reserved**	-	0x1
[3]	R/W	**MEMCCLK**	Memory Bank C Controller => FCLK_MEMC, BCLK_MEMC	0x1
[2]	R/W	**Reserved**	-	-
[1]	R/W	**MEMACLK**	Memory Bank A Controller => FCLK_MEMA, BCLK_MEMA, BCLK_SDRMA	0x1
[0]	R/W	**A940TCLK**	A940T CPU A940TFCLK, A940TBCLK	0x1
Communication Device Clock Enable Register (COMCLKENREG) ***Address : C000 0908h***				
[9]	R/W	**SSPCLK**	SSP/SDI Block Clock => SSP_CLK, PCLK_SSP	0x1
[8]	R/W	**I^2C CLK**	I^2C Controller => PCLK_ I^2C	0x1
[7]	R/W	**UART3CLK**	UART3 => UART3_CLK, PCLK_UT3	0x1
[6]	R/W	**UART2CLK**	UART2 => UART2_CLK, PCLK_UT2	0x1
[5]	R/W	**UART1CLK**	UART1 => UART1_CLK, PCLK_UT1	0x1
[4]	R/W	**UART0CLK**	UART0 => UART0_CLK, PCLK_UT0	0x1
[3]	R/W	**OWMCLK**	OWM Clock => PCLK_OWM	0x1
[2]	R/W	**Reserved**	-	-
[1]	R/W	**UDCCLK**	USB Device Controller Clock => UCLK_UDC[48(47.923)MHz], PCLK_UDC	0x1
[0]	R/W	**UHCCLK**	USB Host Processor Clock => UCLK_UHC[48(47.923)MHz], PCLK_UHC	0x1
Video & Graphic Device Clock Enable Register (VGCLKENREG) ***Address : C000 090ah***				
[15]	R	**DBLKCLK**	Deblock Enable => BCLK_DBLCK	0x1
[14]	R/W	**MPGIFCLK**	MPEG I/F Block => BCLK_MPGIF	0x1
[13]	R/W	**DECSSCLK**	DVD DeCSS Block => PCLK_DECSS	0x1
[12]	R/W	**MECLK**	Motion Estimation Block => BCLK_MEC, BCLK_MEF, PCLK_ME	0x1
[11]	R/W	**REFWCLK**	RefWrite Block => BCLK_REF	0x1
[10]	R/W	**RVLDCLK**	RVLD Block => BCLK_RVLD	0x1
[9]	R/W	**QGMCCLK**	Q-Pel & GMC => BCLK_QGMC	0x1
[8]	R/W	**MPMCCLK**	MP/MC => BCLK_MPMC	0x1
[7]	R/W	**PDFCLK**	PRED/Q & DCT & Format Converter => BCLK_PREQ, BCLK_DCT, BCLK_FMTC	0x1
[6]	R/W	**HUFFCLK**	Stream Processor & Huffman block => BCLK_HUFF	0x1

Bit	R/W	Symbol	Description	Reset Value
[5]	R/W	**VPCLKGOFF**	Video Processor Gated Clock Disable bit (PRED/Q, DCT, MP/MC, RefWrite, Q-Pel, GMC, Deblocking, MEC, MEF)	0x1
[4]	R/W	**VPTOPCLK**	Video Processor Top block => BCLK_MPEG	0x1
[3]	R/W	**ISPCLK**	Image Processor => IMAGE_CLK0, IMAGE_CLK1	0x1
[2]	R/W	**GRPCLK**	Graphic & Rotation Processor => BCLK_GRPH	0x1
[1]	R/W	**SCALECLK**	Scale Processor => BCLK_SCALE	0x1
[0]	R/W	**DISPCLK**	Display Controller => BCLK_DISP, DISP_CLK0, DISP_CLK1	0x1
Audio & Storage Device Clock Enable Register (ASCLKENREG) ***Address : C000 090ch***				
[13]	R/W	**CDROMCLK**	CD-ROM Decoder Block => PCLK_CDROM	0x1
[12]	R/W	**IDECLK**	IDE I/F Block => BCLK_IDEIF	0x1
[11]	R/W	**Reserved**	-	-
[10]	R/W	**Reserved**	-	-
[9]	R/W	**MSTICKCLK**	Memory Stick Controller Clock => MCLK_STICK[20(19.169)MHz], PCLK_STICK	0x1
[8]	R/W	**MMCCLK**	MMC/SD Controller Clock => PCLK_MMC	0x1
[7]	R/W	**Reserved**	-	-
[6]	R/W	**Reserved**	-	-
[5]	R/W	**Reserved**	-	-
[4]	R/W	**Reserved**	-	-
[3]	R/W	**SPDIFOCLK**	SPDIF Output Clock => ACLK_SPDIFO, DCLK_SPDIFO, PCLK_SPDIFO	0x1
[2]	R/W	**SPDIFICLK**	SPDIF Input Clock => ACLK_SPDIFI, DCLK_SPDIFI, PCLK_SPDIFI	0x1
[1]	R/W	**I2SCLK**	I2S Controller Clock => ACLK_I2S(12.288MHz), QCLK_I2S, PCLK_I2S	0x1
[0]	R/W	AC97**CLK**	AC97 Controller Clock => ACLK_ AC97 (12.288MHz), PCLK_ AC97	0x1
FCLK PLL Setting Value Write Register (FPLLSETVREG) ***Address : C000 0910h***				
[15:8]	R/W	**FMDIV**	MDIV of PLL	16'h9407
[7:2]	R/W	**FPDIV**	PDIV of PLL	
[1:0]	R/W	**FSDIV**	SDIV of PLL	
FCLK PLL Value Setting Register (FPLLVSETREG) ***Address : C000 0912h***				
[15:8]	R	**FMDIVR**	MDIV of PLL	16'h9407

Bit	R/W	Symbol	Description	Reset Value
[7:2]	R	**FPDIVR**	PDIV of PLL	
[1:0]	R	**FSDIVR**	SDIV of PLL	
UCLK PLL Setting Value Write Register (UPLLSETVREG) ***Address : C000 0914h***				
[15:8]	R/W	**UMDIV**	MDIV of PLL	16'h6002
[7:2]	R/W	**UPDIV**	PDIV of PLL	
[1:0]	R/W	**USDIV**	SDIV of PLL	
UCLK PLL Value Setting Register (UPLLVSETREG) ***Address : C000 0916h***				
[15:8]	R	**UMDIVR**	MDIV of PLL	16'h6002
[7:2]	R	**UPDIVR**	PDIV of PLL	
[1:0]	R	**USDIVR**	SDIV of PLL	
ACLK PLL Setting Value Write Register (APLLSETVREG) ***Address : C000 0918h***				
[15:8]	R/W	**AMDIV**	MDIV of PLL	16'h9802
[7:2]	R/W	**APDIV**	PDIV of PLL	
[1:0]	R/W	**ASDIV**	SDIV of PLL	
ACLK PLL Value Setting Register (APLLVSETREG) ***Address : C000 091ah***				
[15:8]	R	**AMDIVR**	MDIV of PLL	16'h9802
[7:2]	R	**APDIVR**	PDIV of PLL	
[1:0]	R	**ASDIVR**	SDIV of PLL	
System Clock PLL Divide Value Set Register (SYSCSETREG) ***Address : C000 091ch***				
[8:6]	R/W	**DCLKDIV**	DCLK Clock Generation F-PLL Divide Set Value(N-1) DCLK means Double BCLK clock for DDR, it used for Memory Controller So, BCLK is DCLK * 1/2.	0x0
[5:3]	R/W	**A940TFDIV**	A940T FCLK Clock Generation F-PLL Divide Set Value(N-1)	0x0
[2:0]	R/W	**A920TFDIV**	A920T FCLK Clock Generation F-PLL Divide Set Value(N-1)	0x0
External System Clock Time Set Register (ESYSCSETREG) ***Address : C000 091eh***				
[15:14]	R/W	**ESYSCLKSRC**	External System Output Clock Generation PLL Source Select	0x01

Bit	R/W	Symbol	Description	Reset Value
			11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	
[13:8]	R/W	**ESYSDIV**	External System Clock Generation PLL Divide Set Value(N-1)	0x1
[7]	R/W	**ESYSPOL**	External System Clock Output Polarity Inverting Set	0x0
[6:4]	R/W	**ESYSDLY**	External System Clock Output Delay Time Value(N)	0x0
[3]	R/W	**SDRCLKPOL**	BCLK_SDRMA, BCLK_SDRMB Clock Output Polarity Inverting Set	0x0
[2:0]	R/W	**SDRCLKDLY**	BCLK_SDRMA, BCLK_SDRMB Clock Output Delay Time Value(N)	0x0
USB/ MMC Clock Generation U-PLL Divide Value Set Register (UIRMCSETREG) ***Address : C000 0920h***				
[15:14]	R/W	**MMCCLKSRC**	MMC/SD/MStick Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK,"00 = No Clock	0x0502
[13:8]	R/W	**MMCCLKDIV**	MMC/SD/MStick Clock Generation U-PLL Divide Set Value(N-1)	
[7:6]	R/W	**USBIRCLKSRC**	USB/ Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	
[5:0]	R/W	**USBIRDIV**	USB/ Clock Generation U-PLL Divide Set Value(N-1)	
Audio Controller Clock Generation PLL Divide Value Set (AUDICSETREG) ***Address : C000 0922h***				
[7:6]	R/W	**AUDCLKSRC**	AC97/I2S Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	0x0000
[5:0]	R/W	**AUDCLKDIV**	AC97/I2S Controller Clock Generation A-PLL Divide Set Value(N-1)	
SPDIF Controller Clock Generation PLL Divide Value Set Register (SPDICSETREG) ***Address : C000 092eh***				
[15:14]	R/W	**SPDIFINSRC**	SPDIF In Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	0x0000
[13:8]	R/W	**SPDIFINDIV**	SPDIF In Controller Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**SPDIFOUTSRC**	SPDIF Out Controller Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = ABIT_CLK	
[5:0]	R/W	**SPDIFOUTDIV**	SPDIF Out Controller Clock Generation A-PLL Divide Set Value(N-1)	
Display Clock Generation PLL Divide Value Set Register (DISPCSETREG) ***Address : C000 0924h***				
[15:14]	R/W	**DISPCLKSRC**	Display Clock(DISP_CLK0) Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK,"01 = FPLL_CLK, 00 = EXTCLKin	0x0000
[13:8]	R/W	**DISPCLKDIV**	Display Clock(DISP_CLK0) Generation PLL Divide Set Value(N-1)	

Bit	R/W	Symbol	Description	Reset Value
[7]	R/W	**DISPCLKPOL**	Invert EXTCLKin polarity, when it will be selected by source clock	
Image Pixel Clock Generation PLL Divide Value Set Register (IMAGCSETREG) ***Address : C000 0926h***				
[15:14]	R/W	**IMGCLKSRC**	Image Pixel Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = no Clock	0x0000
[13:8]	R/W	**IMGCLKDIV**	Image Pixel Clock Generation PLL Divide Set Value(N-1)	
UART0/1 TX/RX Clock Generation PLL Divide Value Set Register (URT0CSETREG) ***Address : C000 0928h***				
[15:14]	R/W	**URT1CLKSRC**	UART1 Data TX/RX Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK,"00 = No Clock	0x0000
[13:8]	R/W	**URT1CLKDIV**	UART1 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**URT0CLKSRC**	UART0 Data TX/RX Clock Generation PLL Source Select	
[5:0]	R/W	**URT0CLKDIV**	UART0 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	
UART TX/RX Clock Generation PLL Divide Value Set Register (URT1CSETREG) ***Address : C000 092ah***				
[15:14]	R/W	**URT3CLKSRC**	UART3 Data TX/RX Clock or SSP Clock Generation PLL Source Select 11 = APLL_CLK, 10 = UPLL_CLK, 01 = FPLL_CLK, 00 = No Clock	0x0000
[13:8]	R/W	**URT3CLKDIV**	UART3 Data TX/RX Clock or SSP Clock Generation PLL Divide Set Value(N-1)	
[7:6]	R/W	**URT2CLKSRC**	UART2 Data TX/RX Clock Generation PLL Source Select	
[5:0]	R/W	**URT2CLKDIV**	UART2 Data TX/RX Clock Generation PLL Divide Set Value(N-1)	
ARM940T CPU Power Manage Mode Register (A940TMODEREG) ***Address : C000 092ch***				
[0]	R/W	**A940TIDLE**	ARM940T CPU IDLE Mode, this bit should be written by ARM940T CPU only	0x0

TABLE 5-21. CLOCK AND POWER REGISTERS LIST

CHAPTER 6

REAL TIME CLOCK(RTC)

6. REAL TIME CLOCK(RTC)

6.1 OVERVIEW

The real-time clock (RTC) provides a general-purpose real-time reference. It is a free running counter and starts incrementing the count value after the de-assertion of reset. The counter is incremented on rising edges of the 1Hz clock. Set this counter to the desired value.

The RTC incorporates a 32-bit RTC Alarm register. This may be programmed with a value that is compared against the RTC Time Counter register. On each rising edge of the 1Hz clock, the counter is incremented and then compared to the RTC Time Counter register. This status bit is also routed to the interrupt controller and may be unmasked in the interrupt controller to generate a processor interrupt.

The clock is generated by dividing clock source : 32.768KHz. The divide logic is programmable as unit time is 32.768KHz.

FEATURES

- 32-bit RTC Time Counter register with 1Hz unit clock
- 32-bit RTC Alarm register : Alarm interrupt or wake-up from power down mode
- Wake-up condition : Low Battery Fault, Two External Input, Alarm interrupt, 1Hz interrupt, GPIO interrupt

6.2 RTC OPERATION

RTC Counter Set Register (RTCTSETREG)

The RTCTSETREG is the register that sets a RTC counter value in 1 KHz unit. It is initialized when the power is reset. If the CPU writes a value to the register, the value is written to the RTCTCNTREG after one second.
When you try to write new value to RTCSETREG, new written value can be lost without being updated. To avoid this problem, do not write new value at 1Hz clock edge. You can check if current RTC value is near to 1Hz edge by reading sub-second time count register (RTCSTCNTREG).

Address : C000 0C00h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**RTCTSETREG**	RTC Counter Set Register. Unit Time is 1Hz. Initialized by PORRSTn(power-on reset) only. RTCTSETREG will be written when either RTCTCNTREG or RTCTSETREG is written by CPU. And when RTCTSETREG is updated, then its new value will be written into RTCTCNTREG in 1sec later.	0

TABLE 6-1. RTC COUNTER SET REGISTER

RTC Time Count Register (RTCTCNTREG)

The RTCTCNTREG is the counter register that indicates the RTC Time. The count value increments one by one every 1 second.

Address : C000 0C04h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R	**RTCTCNTREG**	RTC Time Count Register. Read Only. Unit Time is 1Hz. Never be initialized at all. RTCTCNTREG couldn't be written by CPU directly, but RTCTSETREG will be written instead, and the value of RTCTSETREG will be written into RTCTCNTREG indirectly at 1Hz clock rising edge. Therefore the new value of RTCTCNTREG will be updated in 1 sec later approximately, after writing a new RTC Time value to RTCTCNTREG[31:16].	unknown

TABLE 6-2. RTC TIME COUNT REGISTER

RTC Sub-Second Time Count Register (RTCSTCNTREG)

The RTCSTCNTREG is the Sub second time counter register. The count value increments in 1/1024 second unit. It is initialized into '0' when the power is reset.

Address : C000 0C08h

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R	**RTCSTCNTREG**	RTC Sub-Second Time Count Register. Read Only. Same as 1Hz clock counter[15:6]. Unit Time is 1/1,024 second. Initialized by PORRSTn only.	0

TABLE 6-3. RTC SUB-SECOND TIME COUNT REGISTER

RTC Time Tick Set Register (TICKSETREG)

The TICKSETREG is the register that establishes the Sub-second timer. When the RTCSTCNTREG value coincides with its value, an interrupt can be initiated.

Address : C000 0C0Ah

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**TICKSETREG**	RTC Time Tick Set Register. Ref. Time is RTCSTCNTREG. Initialized by PORRSTn only	0

TABLE 6-4. RTC TIME TICK SET REGISTER

ALARM Time Set Register (ALARMTREG)

The ALARMTREG is the register that sets an alarm time in a second unit.

Address : C000 0C0Ch

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ALARMTREG**	ALARM Time Set Register. Unit Time is 1Hz. Initialized by PORRSTn only	0

TABLE 6-5. ALARM TIME SET REGISTER

Power Manage Register (PWRMGRREG)

The PWRMGRREG is the register that sets the Power mode of a GPIO module.

Address : C000 0C10h

Bit	R/W	Symbol	Description	Reset Value
[0]	R/W	**PWRMGRREG**	1-MP2520F GPIO Power On at STOPMode 0-MP2520F GPIO Power Off at STOPMode	0

TABLE 6-6. POWER MANAGE REGISTER

Clock Manage Register (CLKMGRREG)

The CLKMGRREG is the register that sets the Operation mode of the UPLL and the APLL and sets a PMRTCCLK source.

Address : C000 0C12h

Bit	R/W	Symbol	Description	Reset Value
[2]	R/W	**PMRTCCLK_SEL**	1-Use ABIT_CLK as PMRTCCLK. 0-Use OSC32KHz as PMRTCCLK.	0
[1]	R/W	**APLL_USE**	1-ACLKPLLUse, ACLK PLL Usage	0
[0]	R/W	**UPLL_USE**	1-UCLKPLLUse, UCLK PLL Usage	0

TABLE 6-7. CLOCK MANAGE REGISTER

Reset Enable Control Register (RSTCTRLREG)

The RSTCTRLREG is the register that enables a variety of reset.

Address : C000 0C14

Bit	R/W	Symbol	Description	Default Value
[9]	R/W	**ESOFTRST_ENB**	Reset Enable for RTC External1 Soft Reset Event	0
[8]	R/W	**SOFTRST**	Software Reset Assertion	0
[7]	R/W	**GPIORST_ENB**	Reset Enable for GPIO Reset Event	0
[6]	R/W	**Reserved**	-	-
[5]	R/W	**BATTFnRST_ENB**	Reset Enable for BATT_FAULTn Reset Event	0
[4]	R/W	**EXTIN1RST_ENB**	Reset Enable for RTC External1 Reset Event	0
[3]	R/W	**EXTIN0RST_ENB**	Reset Enable for RTC External0 Reset Event	0
[2]	R/W	**ALARMRST_ENB**	Reset Enable for RTC Alarm Reset Event	0
[1]	R/W	**STWATCHRST_ENB**	Reset Enable for RTC Stop Watch Reset Event	0
[0]	R/W	**Reserved**	-	-

TABLE 6-8. RESET ENABLE CONTROL REGISTER

Reset Event Status Register (RSTSTREG)

The RSTSTREG is the register that shows the types of the reset when the MP2520F is initialized by a reset.

Address : C000 0C16h

Bit	R/W	Symbol	Description	Reset Value
[9]	R/W	**ESOFTRST**	RTC External1 Soft Reset Event Status	0
[8]	R/W	**WDOGRST**	Watchdog Timer Reset Event Status	0
[7]	R/W	**GPIORST**	GPIO Reset Event Status	0
[6]	R/W	**Reserved**	-	-
[5]	R/W	**BATTFnRST**	BATT_FAULTn Reset Event Status	0
[4]	R/W	**EXTIN1RST**	RTC External1 Reset Event Status	0
[3]	R/W	**EXTIN0RST**	RTC External0 Reset Event Status	0
[2]	R/W	**ALARMRST**	RTC Alarm Reset Event Status	0
[1]	R/W	**STWATCHRST**	RTC Stop Watch Reset Event Status	0
[0]	R/W	**HRST**	Hard Reset Event Status	0

TABLE 6-9. RESET EVENT STATUS REGISTER

Boot Operation Control Register (BOOTCTRLREG)

The BOOTCTRLREG determines the reboot when the system is initialized by a reset such as Stop mode wake up, Watch dog timer reset, Soft reset, nRESET, etc.

Address : C000 0C18h

Bit	R/W	Symbol	Description	Reset Value
[2]	R/W	**WAKE_DISABLE**	Boot Operation Disable in STOPMode wake-up procedure	1
[1]	R/W	**WDTSFT_DISABLE**	Boot Operation Disable in WDT/Soft reset procedure	0
[0]	R/W	**HRST_DISABLE**	Boot Operation Disable in nRESET reset procedure	0

TABLE 6-10. BOOT OPERATION CONTROL REGISTER

Clock Locking Time Set Register (LOCKTIMEREG)

When a PLL input frequency is changed or the Wake-up occurs in Sleep mode or Deep sleep mode, the PLL output frequency is locked as much time as this register has been set into.

Address : C000 0C1Ah

Bit	R/W	Symbol	Description	Reset Value
[15:12]	R/W	**LOCKTIME1**	Clock Locking Time during PLL Setting Value Change or when MP2520F become NORMALMode from SLEEPMode. Max Value = 480us	A
[11:0]	R/W	**LOCKTIME0**	Clock Locking Time when MP2520F become NORMALMode from DEEP SLEEPMode(OSC7MHzOFF = '1' condition). Max Value = 120ms	064

TABLE 6-11. CLOCK LOCKING TIME SET REGISTER

Reset Width Time Set Register (RSTTIMEREG)

When reset occurs, the RSTTIMEREG increases the reset period as much as the reset time has been internally set into. The unit of a reset time value is about 30s.

Address : C000 0C1Ch

TABLE 6-12. RESET WIDTH TIME SET REGISTER

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**RSTTIME**	Reset Width Time when MP2520F become NORMALMode from STOPMode or power-on reset operation. Max Value = 480ms	FFF

Ext. Input 0/1 Pin State Control Register (EXTCTRLREG)

The EXTCTRLREG is the register that sets the event types of the GPIO pin and the external input 0/1 pin to be used for a Wake up event.

Address : C000 0C1Eh

Bit	R/W	Symbol	Description	Reset Value
[9:8]	R/W	**GPIO_EVENT_MODE**	GPIO Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b01
[5:4]	R/W	**EXTIN1_EVENT_MODE**	Ext. Input1 Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b11
[1:0]	R/W	**EXT0IN_EVENT_MODE**	Ext. Input0 Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b01

TABLE 6-13. EXT. INPUT 0/1 PIN STATE CONTROL REGISTER

Stop Watch Time Set Register (STOPTSETREG)

Address : C000 0C20h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**STOPTIME**	Stop Watch Time	0

TABLE 6-14. STOP WATCH TIMER REGISTER

RTC Control Register (RTCCTRLREG)

Address : C000 0C22h

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**LVLENB**	Level shifter enable	1
[14]	R/W	**RTCTENB1**	1Hz clock generation quick test enable mode 1 If '1', 32.768KHz clock will be inserted into 11th Reg. out of 16bit Sub-Second Counter.	0
[13]	R/W	**RTCTENB2**	1Hz clock generation quick test enable mode 0 If '1', 32.768KHz clock will be inserted into 6th Reg. out of 16bit Sub-Second Counter.	0

Bit	R/W	Symbol	Description	Reset Value
[12:10]	-	**Reserved**	-	-
[9]	R/W	**TICKALLINT_ENB**	Interrupt Enable for Time TICK All Value Equal Event detect	0
[8]	R/W	**TICKINDINT_ENB**	Interrupt Enable for Time TICK Individual Vale Equal Event detect	0
[7]	R/W	**GPIOINT_ENB**	Interrupt Enable for GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-
[5]	R/W	**BATTFINT_ENB**	Interrupt Enable for Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_ENB**	Interrupt Enable for External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_ENB**	Interrupt Enable for External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_ENB**	Interrupt Enable for RTC ALARM Time Detect	0
[1]	R/W	**STWINT_ENB**	Interrupt Enable for RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_ENB**	Interrupt Enable for 1Hz Detect	

TABLE 6-15. RTC CONTROL REGISTER

RTC Interrupt Status Register (RTCSTREG)

Address : C000 0C24h

ㄴBit	R/W	Symbol	Description	Reset Value
[9]	R/W	**TICKALLINT_PEND**	Time TICK All Value Equal Event detect	0
[8]	R/W	**TICKINDINT_PEND**	Time TICK Individual Vale Equal Event detect	
[7]	R/W	**GPIOINT_PEND**	GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-
[5]	R/W	**BATTFINT_PEND**	Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_PEND**	External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_PEND**	External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_PEND**	RTC ALARM Time Detect	0
[1]	R/W	**STWINT_PEND**	RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_PEND**	1Hz Detect	

TABLE 6-16. RTC INTERRUPT STATUS REGISTER

6.3 RTC REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
RTC Counter Set Register (RTCTSETREG) ***Address : C000 0C00h***				
[31:0]	R/W	**RTCTSETREG**	RTC Counter Set Register. Unit Time is 1Hz. Initialized by PORRSTn(power-on reset) only. RTCTSETREG will be written when either RTCTCNTREG or RTCTSETREG is written by CPU. And when RTCTSETREG is updated, then its new value will be written into RTCTCNTREG in 1sec later.	0
RTC Time Count Register (RTCTCNTREG) ***Address : C000 0C04h***				
[31:0]	R	**RTCTCNTREG**	RTC Time Count Register. Read Only. Unit Time is 1Hz. Never be initialized at all. RTCTCNTREG couldn't be written by CPU directly, but RTCTSETREG will be written instead, and the value of RTCTSETREG will be written into RTCTCNTREG indirectly at 1Hz clock rising edge. Therefore the new value of RTCTCNTREG will be updated in 1 sec later approximately, after writing a new RTC Time value to RTCTCNTREG[31:16].	unknown
RTC Sub-Second Time Count Register (RTCSTCNTREG) ***Address : C000 0C08h***				
[9:0]	R	**RTCSTCNTREG**	RTC Sub-Second Time Count Register. Read Only. Same as 1Hz clock counter[15:6]. Unit Time is 1/1,024 second. Initialized by PORRSTn only.	0
RTC Time Tick Set Register (TICKSETREG) ***Address : C000 0C0Ah***				
[9:0]	R/W	**TICKSETREG**	RTC Time Tick Set Register. Ref. Time is RTCSTCNTREG. Initialized by PORRSTn only	0
ALARM Time Set Register (ALARMTREG) ***Address : C000 0C0Ch***				
[9:0]	R/W	**ALARMTREG**	ALARM Time Set Register. Unit Time is 1Hz. Initialized by PORRSTn only	0
Power Manage Register (PWRMGRREG) ***Address : C000 0C10h***				
[0]	R/W	**PWRMGRREG**	1-MP2520F GPIO Power On at STOPMode 0-MP2520F GPIO Power Off at STOPMode	0
Clock Manage Register (CLKMGRREG) ***Address : C000 0C12h***				
[2]	R/W	**PMRTCCLK_SEL**	1-Use ABIT_CLK as PMRTCCLK. 0-Use OSC32KHz as PMRTCCLK.	0
[1]	R/W	**APLL_USE**	1-ACLKPLLUse, ACLK PLL Usage	0

Bit	R/W	Symbol	Description	Reset Value
[0]	R/W	**UPLL_USE**	1-UCLKPLLUse, UCLK PLL Usage	0
Reset Enable Control Register (RSTCTRLREG) **Address : C000 0C14h**				
[9]	R/W	**ESOFTRST_ENB**	Reset Enable for RTC External1 Soft Reset Event	0
[8]	R/W	**SOFTRST**	Software Reset Assertion	0
[7]	R/W	**GPIORST_ENB**	Reset Enable for GPIO Reset Event	0
[6]	R/W	**Reserved**	-	-
[5]	R/W	**BATTFnRST_ENB**	Reset Enable for BATT_FAULTn Reset Event	0
[4]	R/W	**EXTIN1RST_ENB**	Reset Enable for RTC External1 Reset Event	0
[3]	R/W	**EXTIN0RST_ENB**	Reset Enable for RTC External0 Reset Event	0
[2]	R/W	**ALARMRST_ENB**	Reset Enable for RTC Alarm Reset Event	0
[1]	R/W	**STWATCHRST_ENB**	Reset Enable for RTC Stop Watch Reset Event	0
[0]	R/W	**Reserved**	-	-
Reset Event Status Register (RSTSTREG) **Address : C000 0C16h**				
[9]	R/W	**ESOFTRST**	RTC External1 Soft Reset Event Status	0
[8]	R/W	**WDOGRST**	Watchdog Timer Reset Event Status	0
[7]	R/W	**GPIORST**	GPIO Reset Event Status	0
[6]	R/W	**Reserved**	-	-
[5]	R/W	**BATTFnRST**	BATT_FAULTn Reset Event Status	0
[4]	R/W	**EXTIN1RST**	RTC External1 Reset Event Status	0
[3]	R/W	**EXTIN0RST**	RTC External0 Reset Event Status	0
[2]	R/W	**ALARMRST**	RTC Alarm Reset Event Status	0
[1]	R/W	**STWATCHRST**	RTC Stop Watch Reset Event Status	0
[0]	R/W	**HRST**	Hard Reset Event Status	0
Boot Operation Control Register (BOOTCTRLREG) **Address : C000 0C18h**				
[2]	R/W	**WAKE_DISABLE**	Boot Operation Disable in STOPMode wake-up procedure	1
[1]	R/W	**WDTSFT_DISABLE**	Boot Operation Disable in WDT/Soft reset procedure	0
[0]	R/W	**HRST_DISABLE**	Boot Operation Disable in nRESET reset procedure	0
Clock Locking Time Set Register (LOCKTIMEREG) ***Address : C000 0C1Ah***				

Bit	R/W	Symbol	Description	Reset Value
[15:12]	R/W	**LOCKTIME1**	Clock Locking Time during PLL Setting Value Change or when MP2520F become NORMALMode from SLEEPMode. Max Value = 480us	0
[11:0]	R/W	**LOCKTIME0**	Clock Locking Time when MP2520F become NORMALMode from DEEP SLEEPMode(OSC7MHzOFF = '1' condition). Max Value = 120ms	0
Reset Width Time Set Register (RSTTIMEREG) ***Address : C000 0C1Ch***				
[13:0]	R/W	**RSTTIME**	Reset Width Time when MP2520F become NORMALMode from STOPMode or power-on reset operation. Max Value = 480ms	0
Ext. Input0/1 Pin State Control Register (EXTCTRLREG) ***Address : C000 0C1Eh***				
[9:8]	R/W	**GPIO_EVENT_MODE**	GPIO Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b01
[5:4]	R/W	**EXTIN1_EL-VENT_MODE**	Ext. Input1 Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b11
[1:0]	R/W	**EXT0IN_EVENT_MODE**	Ext. Input0 Pin Interrupt/Reset Detect Mode "00"-Low Level, "01"-High Level, "10"-Falling Edge, "11"-Rising Edge	2'b01
Stop Watch Time Register (STOPTSETREG) ***Address : C000 0C20h***				
[15:0]	R/W	**StopTime**	Stop Watch Time	0
RTC STOPTIME Control Register (RTCCTRLREG) ***Address : C000 0C22h***				
[15]	R/W	**LVLENB**	Level shifter enable	1
[14]	R/W	**RTCTENB1**	1Hz clock generation quick test enable mode 1 If '1', 32.768KHz clock will be inserted into 11th Reg. out of 16bit Sub-Second Counter.	0
[13]	R/W	**RTCTENB2**	1Hz clock generation quick test enable mode 0 If '1', 32.768KHz clock will be inserted into 6th Reg. out of 16bit Sub-Second Counter.	0
[12:10]	-	**Reserved**	-	-
[9]	R/W	**TICKALLINT_ENB**	Interrupt Enable for Time TICK All Value Equal Event detect	0
[8]	R/W	**TICKINDINT_ENB**	Interrupt Enable for Time TICK Individual Vale Equal Event detect	0
[7]	R/W	**GPIOINT_ENB**	Interrupt Enable for GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-

Bit	R/W	Symbol	Description	Reset Value
[5]	R/W	**BATTFINT_ENB**	Interrupt Enable for Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_ENB**	Interrupt Enable for External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_ENB**	Interrupt Enable for External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_ENB**	Interrupt Enable for RTC ALARM Time Detect	0
[1]	R/W	**STWINT_ENB**	Interrupt Enable for RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_ENB**	Interrupt Enable for 1Hz Detect	
RTC Interrupt Status Register (RTSTRLREG) ***Address : C000 0C24h***				
[9]	R/W	**TICKALLINT_PEND**	Time TICK All Value Equal Event detect	0
[8]	R/W	**TICKINDINT_PEND**	Time TICK Individual Vale Equal Event detect	
[7]	R/W	**GPIOINT_PEND**	GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-
[5]	R/W	**BATTFINT_PEND**	Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_PEND**	External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_PEND**	External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_PEND**	RTC ALARM Time Detect	0
[1]	R/W	**STWINT_PEND**	RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_PEND**	1Hz Detect	
Stop Watch Time Set Register (STOPTSETREG) ***Address : C000 0C20h***				
[15:0]	R/W	STOPTIME	Stop Watch Time	0
RTC Control Register (RTCCTRLREG) ***Address : C000 0C22h***				
[15]	R/W	**LVLENB**	Level shifter enable	1
[14]	R/W	**RTCTENB1**	1Hz clock generation quick test enable mode 1 If '1', 32.768KHz clock will be inserted into 11th Reg. out of 16bit Sub-Second Counter.	0
[13]	R/W	**RTCTENB2**	1Hz clock generation quick test enable mode 0 If '1', 32.768KHz clock will be inserted into 6th Reg. out of 16bit Sub-Second Counter.	0
[12:10]	-	**reserved**	-	-
[9]	R/W	**TICKALLINT_ENB**	Interrupt Enable for Time TICK All Value Equal Event detect	0

Bit	R/W	Symbol	Description	Reset Value
[8]	R/W	**TICKINDINT_ENB**	Interrupt Enable for Time TICK Individual Vale Equal Event detect	0
[7]	R/W	**GPIOINT_ENB**	Interrupt Enable for GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-
[5]	R/W	**BATTFINT_ENB**	Interrupt Enable for Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_ENB**	Interrupt Enable for External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_ENB**	Interrupt Enable for External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_ENB**	Interrupt Enable for RTC ALARM Time Detect	0
[1]	R/W	**STWINT_ENB**	Interrupt Enable for RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_ENB**	Interrupt Enable for 1Hz Detect	
RTC Interrupt Status Register (RTCSTREG) ***Address : C000 0C24h***				
[9]	R/W	**TICKALLINT_PEND**	Time TICK All Value Equal Event detect	0
[8]	R/W	**TICKINDINT_PEND**	Time TICK Individual Vale Equal Event detect	
[7]	R/W	**GPIOINT_PEND**	GPIO Input Pin Event Detect	0
[6]	-	**Reserved**	-	-
[5]	R/W	**BATTFINT_PEND**	Low Battery Fault Detect	0
[4]	R/W	**EXTIN1INT_PEND**	External Input Pin1 Event Detect	0
[3]	R/W	**EXTIN0INT_PEND**	External Input Pin0 Event Detect	0
[2]	R/W	**ALARMINT_PEND**	RTC ALARM Time Detect	0
[1]	R/W	**STWINT_PEND**	RTC STOP Watch Time Detect	0
[0]	R/W	**ONEHZINT_PEND**	1Hz Detect	

TABLE 6-17. RTC REGISTERS LIST

CHAPTER 7

DMA CONTROLLER

7. DMA CONTROLLER

7.1 OVERVIEW

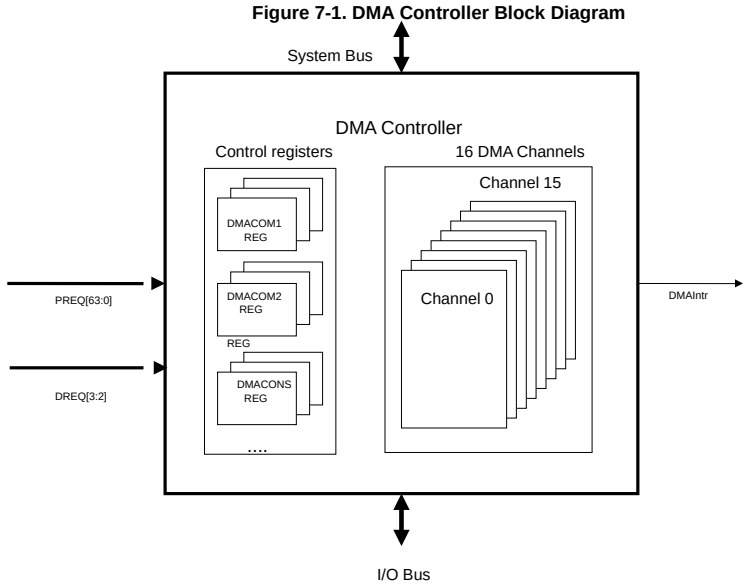
The DMA controller has 16 Channels and 4 words or 8 words of burst transmission. In addition, each channel has 8 EA of 32-bit buffers.

MP2520F supports the 16-channel DMA controller between system buses and peripheral buses. Each channel of the DMA controller can unrestrictedly transmit Data to each device connected to a system bus or a peripheral bus. Therefore, each channel allows devices to transfer data under the following conditions: 1) when the source and the destination are system buses, 2) when the source is a system bus and the destination is a peripheral bus, 3) when the source is a peripheral bus and the destination is a system bus, 4) when the source and the destination are peripheral buses.

The best advantage of the DMA controller is that it can perform the transfer of Data without CPU intervention. The DMA controller performs DMA operation by software, an internal peripheral request or external request.

BLOCK DIAGRAM

Figure 7-1. DMA Controller Block Diagram



7.2 PERIPHERAL INDEX TABLE

Index	Description	Index	Description
0	UART0 Receive	32	Reserved
1	UART0 Transmit	33	Reserved
2	UART1 Receive	34	Reserved
3	UART1 Transmit	35	Reserved
4	UART2 Receive	36	SPDIF Input
5	UART2 Transmit	37	SPDIF Output
6	UART3 Receive	38	SSP Read
7	UART3 Transmit	39	SSP Write
8	Reserved	40	Reserved
9	Reserved	41	Reserved
10	Reserved	42	Reserved
11	Reserved	43	Reserved
12	USB endpoint1 Device	44	Reserved
13	USB endpoint2 Device	45	Reserved
14	USB endpoint3 Device	46	Reserved
15	USB endpoint4 Device	47	Reserved
16	Reserved	48	Reserved
17	Reserved	49	Reserved
18	DeCSS (Read)	50	Reserved
19	DeCSS (Write)	51	Reserved
20	MMC/SD Receive	52	Reserved
21	MMC/SD Transmit	53	Reserved
22	Memory Stick	54	MPEG I/F
23	Reserved	55	SP (Stream Processor)
24	AC97 Audio LR PCM Out	56	Reserved
25	AC97 Audio S-LR PCM Out	57	Reserved
26	AC97 Audio C/W PCM Out	58	Reserved
27	AC97 Microphone In	59	Reserved
28	AC97 Audio L/R PCM In	60	Huffman

Index	Description	Index	Description
29	Touch PAD	61	RVLD
30	I2S Receive	62	Reserved
31	I2S Transmit	63	Reserved

TABLE 7-1. PERIPHERAL INDEX TABLE

DMA request numbers are allocated for internal peripherals of the MP2520F as shown in Table 7-1.

7.3 OPERATION

DMA Control Registers

DMA Channel	Base Address(DMA_CH_BASE)
CH0	0x0200
CH1	0x0210
CH2	0x0220
CH3	0x0230
CH4	0x0240
CH5	0x0250
CH6	0x0260
CH7	0x0270
CH8	0x0280
CH9	0x0290
CH10	0x02a0
CH11	0x02b0
CH12	0x02c0
CH13	0x02d0
CH14	0x02e0
CH15	0x02f0

TABLE 7-2. CHANNEL BASE ADDRESS

Data transfers between an internal peripheral and a memory and between a memory and a memory use “Flow-through” Mode. In addition, the DREQ[3:2] for external devices uses “Fly-by” mode or “Flow-through” mode. The DMA has an 8 word buffer per channel and supports 4 word burst and 8 word burst modes. When the 4 word burst mode is used and a source and a target for Data transfer are peripheral/memory or memory/peripheral respectively, the use of Dual mode enhances the performance because DMA read/write operations are simultaneously executed. For the priority of 16 channels in DMA, the 16 channels are divided into 4 groups. The group0 has the highest priority and the next groups have lower priorities in turn. Therefore, the group3 has the lowest priority.

If all channels run concurrently, the group0 is served four times out of 8 services of DMA and the group1 are served twice. In addition, the group2 and the group3 get the DMA service once respectively. The priorities among channels in each group are determined by the round robin method.

Group	Channels	Priority (service percentage)
0	0, 1, 2, 3	50%
1	4, 5, 6, 7	25%
2	8, 9, 10, 11	12.5%
3	12, 13, 14, 15	12.5%

TABLE 7-3. CHANNEL PRIORITY

7.4 DMA REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
DMA Command Register 0 (DMACOM0) ***Address : C000 0200h***				
[15:14]	R/W	**BURSTSIZE**	Burst operator request size 00 : No Burst 01 : 4 word 10 : 8 word	00
[13]	R/W	**SRCADDRINC**	Source Address Increment Setting 0 : Disable 1 : Enable Increment/Decrement Source address will be increased/decreased per DMACOM1[15:8] (SRCADDRSTEP) value.	0
[12]	R/W	**FLOWSRC**	0 : No Wait, Start the data transfer immediately 1 : Wait for the request signal before initiating the data transfer This bit is effective when the Source is I/O.	0
[11:10]	R/W	**SRCMEMFMT**	Source Memory Data Format 00 : Word 01 : LS Half Word (Lower 16-bit only), the higher 16-bit is ignored 10 : MS Half Word (Higher 16-bit only), the lower 16-bit is ignored	01
[9:8]	R/W	**SRCPERIWD**	Source IO Device Data Width 00 : Byte 01 : Half Word	00
[7:6]	-	**Reserved**	-	-
[5]	R/W	**TRGADDRINC**	Target Address Increment/Decrement Setting 0 : Disable 1 : Enable Increment/Decrement	0
[4]	R/W	**FLOWTRG**	0 : No Wait 1 : Wait for the request signal before initiating the data transfer This bit is effective when the Target is I/O.	0

Bit	R/W	Symbol	Description	Reset Value
[3:2]	R/W	**TRGMEMFMT**	In case of target is memory set the '0' BURSTSIZE of DMACOM0 register. Target Memory Data Format 00 : Word 01 : LS Half Word (Lower 16-bit only) 10 : MS Half Word (Higher 16-bit only)	00
[1:0]	R/W	**TRGPERIWD**	Target IO Device Data Width 00 : Byte 01 : Half Word	00
DMA Command Register_1 (DMACOM1) ***Address : C000 0202h***				
[15:8]	R/W	**SRCADDRSTEP**	Source Address Increment/Decrement by Word -1 : Decrement a Word 0 : Address count disable 1 : Increment a Word Write this bit with 0 when SRCADDRINC is 0.	0x00
[7:0]	R/W	**TRGADDRSTEP**	Target Address Increment/Decrement by Word -1 : Decrement a Word 0 : Address count disable 1 : Increment a Word Write this bit with 0 when TRGADDRINC is 0.	0x00
DMA Command Register_2 (DMACOM2) ***Address : C000 0204h***				
[15:0]	R/W	**DMACOM2**	Request length in byte: Memory transfer quantity. Maximum 64kB (0xFFFF)	0x0000
DMA Control/Status Register (DMACONS) ***Address : C000 0206h***				
[15:11]	-	**Reserved**	-	00000
[10]	R/W	**DMARUN**	1 : DMA Start 0 : DMA End	0
[9]	R/W	**ENDIRQEN**	End Interrupt Enable Indicates that the interrupt is enabled as soon as the data transfer is completed.	0
[8]	-	**Reserved**	-	0
[7:5]	-	**Reserved**	-	000
[4]	R/W	**FLYBYS**	0 : Flow-through 1 : Fly-By for Memory Read Operation	0
[3]	R/W	**FLYBYT**	0 : Flow-through 1 : Fly-By for Memory Write Operation	0
[2]	R	**REQPEND**	0 : No pending request	0

Bit	R/W	Symbol	Description	Reset Value
			1 : Channel has a pending request Indicates that the DMA channel has a pending request.	
[1]	R/W	**ENDINTR**	Read : 0 : No interrupt is generated. 1 : Interrupt caused because the current transaction was successfully completed. Write : 0 : Clear REQPEND	0
[0]	-	**Reserved**	-	0
DMA Source / Target Address Register (SRCLADDR/SRCHADDR) ***Address : C000 0208h / C000 020Ah***				
[31:16]	R/W	**SRCHADDR**	DMA Source High Address Register	0x0000
[15:0]	R/W	**SRCLADDR**	DMA Source Low Address Register, 4-bytes word align	0x0000
DMA Source / Target Address Register (TRGLADDR/TRGHADDR) ***Address : C000 020Ch / C000 020Eh***				
[31:16]	R/W	**TRGHADDR**	DMA Target High Address Register	0x0000
[15:0]	R/W	**TRGLADDR**	DMA Target Low Address Register, 4-bytes word align	0x0000
DMA Interrupt Status Register (DMAINT) ***Address : C000 0000h***				
[15]	R	**DMAINT15**	DMA Channel15 interrupt status	0
[14]	R	**DMAINT14**	DMA Channel14 interrupt status	0
[13]	R	**DMAINT13**	DMA Channel13 interrupt status	0
[12]	R	**DMAINT12**	DMA Channel12 interrupt status	0
[11]	R	**DMAINT11**	DMA Channel11 interrupt status	0
[10]	R	**DMAINT10**	DMA Channel10 interrupt status	0
[9]	R	**DMAINT9**	DMA Channel9 interrupt status	0
[8]	R	**DMAINT8**	DMA Channel8 interrupt status	0
[7]	R	**DMAINT7**	DMA Channel7 interrupt status	0
[6]	R	**DMAINT6**	DMA Channel6 interrupt status	0
[5]	R	**DMAINT5**	DMA Channel5 interrupt status	s
[4]	R	**DMAINT4**	DMA Channel4 interrupt status	0
[3]	R	**DMAINT3**	DMA Channel3 interrupt status	0
[2]	R	**DMAINT2**	DMA Channel2 interrupt status	0

Bit	R/W	Symbol	Description	Reset Value
[1]	R	**DMAINT1**	DMA Channel1 interrupt status	0
[0]	R	**DMAINT0**	DMA Channel0 interrupt status	0
DMA Channel Source I/O Request Map Register (DCH0SRM) ***Address : C000 0100h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH0SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH0SRM_NUM**	DMA Source I/O Peripheral Device Number, Total 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH1SRM) ***Address : C000 0104h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH1SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH1SRM_NUM**	DMA Source I/O Peripheral Device Number, A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH2SRM) ***Address : C000 0108h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH2SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH2SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH3SRM) ***Address : C000 010Ch***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH3SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH3SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH4SRM) ***Address : C000 0110h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH4SRM_VALID**	DMA Source I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH4SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH5SRM) ***Address : C000 0114h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH5SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH5SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH6SRM) ***Address : C000 0118h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH6SRM_VALID**	DMA Source I/O Map ValidBbit	0
[5:0]	R/W	**DCH6SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH7SRM) ***Address : C000 011Ch***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH7SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH7SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH8SRM) ***Address : C000 0120h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH8SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH8SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH9SRM) ***Address : C000 0124h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH9SRM_VALID**	DMA Source I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH9SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH10SRM) ***Address : C000 0128h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH10SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH10SRM_NUM**	DMA Source I/O Peripheral Device Numbe, A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH11SRM) ***Address : C000 012Ah***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH11SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH11SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH12SRM) ***Address : C000 0130h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH12SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH12SRM_NUM**	DMA Source I/O Peripheral Device Numbe, A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH13SRM) ***Address : C000 0134h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH13SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH13SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH14SRM) ***Address : C000 0138h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH14SRM_VALID**	DMA Source I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH14SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Source I/O Request Map Register (DCH15SRM) ***Address : C000 013Ch***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH15SRM_VALID**	DMA Source I/O Map Valid Bit	0
[5:0]	R/W	**DCH15SRM_NUM**	DMA Source I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH0TRM) ***Address : C000 0102h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH0TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH0TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH1TRM) ***Address : C000 0106h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH1TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH1TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH2TRM) ***Address : C000 010Ah***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH2TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH2TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH3TRM) ***Address : C000 010Eh***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH3TRM_VALID**	DMA Target I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH3TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH4TRM) ***Address : C000 0112h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH4TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH4TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH5TRM) ***Address : C000 0116h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH5TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH5TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH6TRM) ***Address : C000 011Ah***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH6TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH6TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH7TRM) ***Address : C000 011Eh***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH7TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH7TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH8TRM) ***Address : C000 0122h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH8TRM_VALID**	DMA Target I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH8TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH9TRM) ***Address : C000 0126h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH9TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH9TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH10TRM) ***Address : C000 012Ah***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH10TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH10TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH11TRM) ***Address : C000 012Eh***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH11TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH11TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH12TRM) ***Address : C000 0132h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH12TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH12TRM_NUM**	DMA Target I/O Peripheral Device Number, A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH13TRM) ***Address : C000 0136h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH13TRM_VALID**	DMA Target I/O Map Valid Bit	0

Bit	R/W	Symbol	Description	Reset Value
[5:0]	R/W	**DCH13TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH14TRM) ***Address : C000 013Ah***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH14TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH14TRM_NUM**	DMA Target I/O Peripheral Device Number, A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000
DMA Channel Target I/O Request Map Register (DCH15TRM) ***Address : C000 013Eh***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**DCH15TRM_VALID**	DMA Target I/O Map Valid Bit	0
[5:0]	R/W	**DCH15TRM_NUM**	DMA Target I/O Peripheral Device Number A total of 64 Peripheral Devices can access each DMA Channel. See Peripheral Index Table.	000000

TABLE 7-4. DMA CONTROLLER REGISTERS LIST

CHAPTER 8

INTERRUPT CONTROLLER

8. INTERRUPT CONTROLLER

8.1 OVERVIEW

ARM920T and ARM940T in 28 interrupt sources from internal peripherals, including the DMA controller, UART, I^2C and GPIO, etc. supply requests to an Interrupt Controller.

An FIQ or an IRQ (interrupt requests) are signaled by the Interrupt Controller to ARM920T or ARM940T. After arbitrating multiple requests from internal peripherals and GPIO, the Controller requests an interrupt.

The hardware arbitration logic decides the interrupt arbitration process, and the results are recorded in the interrupt pending registers.

BLOCK DIAGRAM

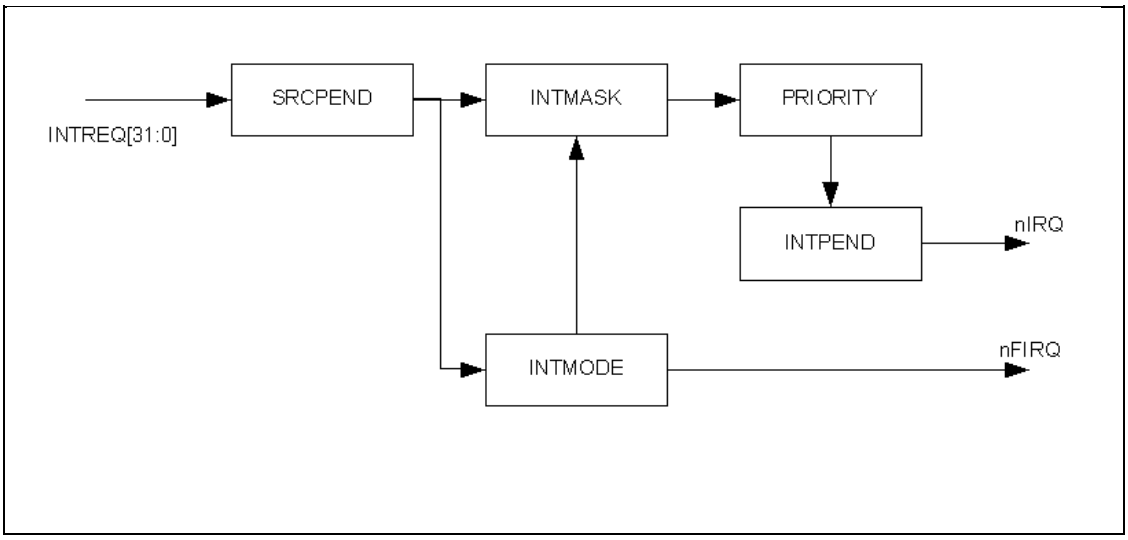


Figure 8-1. Interrupt Process Diagram

8.2 INTERRUPT CONTROLLER OPERATION

The interrupt controller consists of five control registers including the interrupt pending register, priority register, mask register, interrupt mode register and source pending register.

The first registration of all the interrupt requests from the interrupt source is done in the source pending register. Based on the interrupt mode register, interrupt requests are divided into two groups: FIQ requests and IRQ requests. Arbitration is performed for multiple IRQ requests according to the priority register.

F-bit and I-bit of PSR (program status register)

A FIQ (fast interrupt request) from the Interrupt Controller is not accepted by the CPU when the F-bit of PSR (program status register in ARM920T/ARM90T CPU) is set to 1. The IRQ (interrupt request) from the interrupt controller is not accepted by the CPU when the I-bit of PSR (program status register in ARM920T/ARM940T CPU) is set to 1. Therefore, the PSR F-bit or I-bit must be cleared to 0 and the corresponding bit of INTMSK must be set to 0 to enable the interrupt reception.

Interrupt Mode

ARM920T/ARM940T has 2 types of interrupt mode, FIQ or IRQ. All the interrupt sources determine the mode of interrupt to be used at interrupt request.

Interrupt Pending Register

There are two interrupt pending registers in MP2520F - the souce pending register (SRCPND) and the interrupt pending register (INTPND).The interrupt pending status is indicated by these pending registers. One bit of the INTPND register is set to 1 automatically after arbitration, and when the interrupt sources request interrupt service the corresponding bit of the SRCPND register is set to 1. The INTPND register bit is not changed when the corresponding bits of the SRCPND register are set to 1 and the interrupts are masked. The interrupt service routine starts whenever the I-flag or F-flag is set to 0 when a pending bit of the INTPND register is set. You can read and write to the SRCPND and the INTPND registers and the service routine has to clear the pending status by first writing a 1 to the corresponding bit in the SRCPND register and then clearing the pending status in the INTPND register the same way.

Interrupt Mask Register

Indicates that an interrupt has been disabled if the corresponding mask bit is 1. If an interrupt mask bit of INTMSK is 0, the interrupt will be serviced normally. If the corresponding mask bit is 1 and the interrupt is generated, the source pending bit will be set.

8.2.1 Interrupt Sources

32 interrupt sources are supported by interrupt controllers as shown in the following table.

Interrupt Num	Source	Description
0	DISPINT	Display Controller (display VSYNC rising/falling edge)
1	IMGHINT	Image Capture Controller (camera HSYNC)
2	IMGVINT	Image Capture Controller (camera VSYNC)
3	reserved	
4	reserved	
5	TIMERINT	Timer interrupt
6	MSTICKINT	Memory Stick
7	SSPINT	SSP
8	PPMINT	PPM
9	DMAINT	DMA
10	UARTINT	UART 0/1/2/3
11	GRP2DINT	2D Graphic Controller
12	SCALERINT	Image Scaler (VSYNC falling edge)
13	USBHINT	USB Host
14	SDINT	MMC/SD
15	USBDINT	USB Device
16	RTCINT	RTC (nBATTF, EXTIN0, EXTIN 1, Alarm, 1Hz)
17	ADCINT	ADC
18	I^2C INT	I^2C
19	AC97INT	AC97
20	reserved	
21	reserved	
22	reserved	
23	GPIOINT	GPIO
24	CDROMINT	CD-ROM Decoder
25	OWMINT	One Wire Master

Interrupt Num	Source	Description
26	DUALCPUINT	Dual CPU Controller
27	MCUCINT	Non DRAM Memory Controller
28	VLDINT	VLD
29	VIDEOINT	Video Processor
30	MPEGIFINT	MPEG Interface
31	I2SINT	I2S Controller

TABLE 8-1. INTERRUPT SOURCE TABLE

8.2.2 Interrupt Priority Generation Block

Six first-level arbiters and one second level arbiter make up the seven rotation based arbiters in the priority logic of 32 interrupt requests as shown in the following diagram.

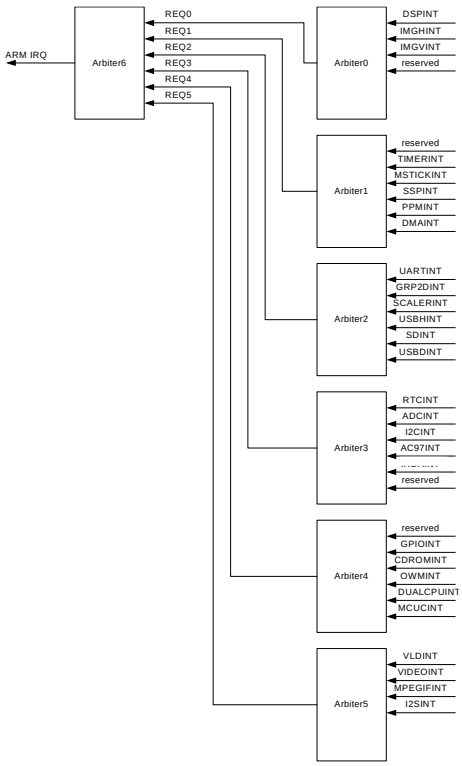


Figure 8-2. Priority Generating Block

8.2.3 Interrupt Priority

Six interrupt requests can be handled by each arbiter based on the one bit arbiter mode control (ARBMODE) and two bits of selection control signals (ARBSEL) as follows:

The order of priority is REQ0, REQ1, REQ2, REQ3, REQ4 and REQ5 when ARBSEL bits are 00b.
The order of priority is REQ0, REQ2, REQ3, REQ4, REQ1 and REQ5 when ARBSEL bits are 01b.
The order of priority is REQ0, REQ3, REQ4, REQ1, REQ2 and REQ5 when ARBSEL bits are 10b.
The order of priority is REQ0, REQ4, REQ1, REQ2, REQ3 and REQ5 when ARBSEL bits are 11b.

As noted the highest priority arbiter is always REQ0 and the lowest REQ5. The priorities of REQ1 to REQ4 can be rotated by changing the ARBSEL.

The arbiter operates in fixed priority mode as ARBSEL bits are not automatically changed even when the ARBMODE bit is set to 0. (However, manually changing the ARBSEL can change the priority.) ARBSEL bits are changed in rotation when ARBMODE bit is 1. For example, ARBSEL bits are changed to 01b automatically to make REQ1 the lowest priority when REQ1 is served. The following are the detailed rules for ARBSEL changes.

ARBSEL bits are not changed when REQ0 or REQ5 is served
ARBSEL bits are changed to 01b when REQ1 is served.
ARBSEL bits are changed to 10b when REQ2 is served.
ARBSEL bits are changed to 11b when REQ3 is served.
ARBSEL bits are changed to 00b when REQ4 is served.

8.2.4 SOURCE PENDING REGISTER (SRCPEND)

There are 24 bits, each related to an interrupt source, in the SRCPND register. When the interrupt request is generated and waiting for the interrupt to be served by the corresponding interrupt, each bit is set to 1. The interrupt sources waiting for their requests to be served can be seen by reading this register. The interrupt source automatically sets each SRCPND bit register regardless of the masking bit in the INTMSK register. The interrupt controller priority logic does not affect this.

The corresponding bit of SRCPND register must be cleared to get the request correctly from the same source in the interrupt service routine for a specific interrupt source. The interrupt controller is operated just like another interrupt request comes in from the same source at return from the ISR without clearing the bit.
A valid interrupt request waiting to be served is always considered when a specific SRCPND register bit is set to 1.

The user's requirement affects the specific time to clear the corresponding bit. The important thing is that you must clear the corresponding bit followed by enabling the interrupt when you want to receive another valid request from the same source.

Through writing a data to this register a specific bit of SRCPND register can be cleared. Only the SRCPND bit positions

corresponding to those set to one in the data are cleared. The corresponding bit positions to those with 0 set in the data remains as those without change.
The bit position which is set in the data by writing '1' can only be cleared. Without set in the write data the bit positions would not be changed.

NOTE : The specific SRCPND must be cleared before he corresponding bit of INTPND When a interrupt pending is cleared

Address : C000 0800h

Bit	R/W	Symbol	Description	Reset Value
[31]	R/C	**I2SINT**	0 = Not requested, 1 = Requested	0
[30]	R/C	**MPEGIFINT**	0 = Not requested, 1 = Requested	0
[29]	R/C	**VIDEOINT**	0 = Not requested, 1 = Requested	0
[28]	R/C	**VLDINT**	0 = Not requested, 1 = Requested	0
[27]	R/C	**MCUCINT**	0 = Not requested, 1 = Requested	0
[26]	R/C	**DUALCPUINT**	0 = Not requested, 1 = Requested	0
[25]	R/C	**OWMINT**	0 = Not requested, 1 = Requested	0
[24]	R/C	**CDROMINT**	0 = Not requested, 1 = Requested	0
[23]	R/C	**GPIOINT**	0 = Not requested, 1 = Requested	0
[22]		**Reserved**	-	-
[21]		**Reserved**	-	-
[20]		**Reserved**	-	-
[19]	R/C	AC97**INT**	0 = Not requested, 1 = Requested	0
[18]	R/C	I^2C **INT**	0 = Not requested, 1 = Requested	0
[17]	R/C	**ADCINT**	0 = Not requested, 1 = Requested	0
[16]	R/C	**RTCINT**	0 = Not requested, 1 = Requested	0
[15]	R/C	**USBDINT**	0 = Not requested, 1 = Requested	0
[14]	R/C	**SDINT**	0 = Not requested, 1 = Requested	0
[13]	R/C	**USBHINT**	0 = Not requested, 1 = Requested	0
[12]	R/C	**SCALERINT**	0 = Not requested, 1 = Requested	0
[11]	R/C	**GRP2DINT**	0 = Not requested, 1 = Requested	0
[10]	R/C	**UARTINT**	0 = Not requested, 1 = Requested	0
[9]	R/C	**DMAINT**	0 = Not requested, 1 = Requested	0

Bit	R/W	Symbol	Description	Reset Value
[8]	R/C	**PPMINT**	0 = Not requested, 1 = Requested	0
[7]	R/C	**SSPINT**	0 = Not requested, 1 = Requested	0
[6]	R/C	**MSTICKINT**	0 = Not requested, 1 = Requested	0
[5]	R/C	**TIMERINT**	0 = Not requested, 1 = Requested	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/C	**IMGVINT**	0 = Not requested, 1 = Requested	0
[1]	R/C	**IMGHINT**	0 = Not requested, 1 = Requested	0
[0]	R/C	**DISPINT**	0 = Not requested, 1 = Requested	0

TABLE 8-2. SOURCE PENDING REGISTER

8.2.5 INTERRUPT MODE REGISTER (INTMODE)

There are 24 interrupt source related bits in this register. The corresponding interrupt is processed in the FIQ (fast interrupt) mode when a specific is set to 1. If not, it is processed in the IRQ (normal interrupt) mode.

NOTE.

1) INTPND and INTOFFSET registers will not be affected by the FIQ interrupt when an interrupt mode is set to FIQ mode in INTMOD register. The INTPND and INTOFFSET registers are valid only for IRQ mode interrupt source.

2) In the interrupt controller only one interrupt source can be served in the FIQ mode. (For the urgent interrupt FIQ mode should only be used.) And only one INTMOD bit can be set to .

Address : C000 0804h

Bit	R/W	Symbol	Description	Reset Value
[31]	R/W	I2SINT	0 = IRQ mode, 1 = FIQ mode	0
[30]	R/W	**MPEGIFINT**	0 = IRQ mode, 1 = FIQ mode	0
[29]	R/W	**VIDEOINT**	0 = IRQ mode, 1 = FIQ mode	0
[28]	R/W	**VLDINT**	0 = IRQ mode, 1 = FIQ mode	0
[28]	R/W	**VLDINT**	0 = IRQ mode, 1 = FIQ mode	0
[27]	R/W	**MCUCINT**	0 = IRQ mode, 1 = FIQ mode	0
[26]	R/W	**DUALCPUINT**	0 = IRQ mode, 1 = FIQ mode	0
[25]	R/W	**OWMINT**	0 = IRQ mode, 1 = FIQ mode	0
[24]	R/W	**CDROMINT**	0 = IRQ mode, 1 = FIQ mode	0

Bit	R/W	Symbol	Description	Reset Value
[23]	R/W	**GPIOINT**	0 = IRQ mode, 1 = FIQ mode	0
[22]	R/W	**Reserved**	-	-
[21]	R/W	**Reserved**	-	-
[20]		**Reserved**	-	-
[19]	R/W	AC97**INT**	0 = IRQ mode, 1 = FIQ mode	0
[18]	R/W	I^2C **INT**	0 = IRQ mode, 1 = FIQ mode	0
[17]	R/W	**ADCINT**	0 = IRQ mode, 1 = FIQ mode	0
[16]	R/W	**RTCINT**	0 = IRQ mode, 1 = FIQ mode	0
[15]	R/W	**USBDINT**	0 = IRQ mode, 1 = FIQ mode	0
[14]	R/W	**SDINT**	0 = IRQ mode, 1 = FIQ mode	0
[13]	R/W	**USBHINT**	0 = IRQ mode, 1 = FIQ mode	0
[12]	R/W	**SCALERINT**	0 = IRQ mode, 1 = FIQ mode	0
[11]	R/W	**GRP2DINT**	0 = IRQ mode, 1 = FIQ mode	0
[10]	R/W	**UARTINT**	0 = IRQ mode, 1 = FIQ mode	0
[9]	R/W	**DMAINT**	0 = IRQ mode, 1 = FIQ mode	0
[8]	R/W	**PPMINT**	0 = IRQ mode, 1 = FIQ mode	0
[7]	R/W	**SSPINT**	0 = IRQ mode, 1 = FIQ mode	0
[6]	R/W	**MSTICKINT**	0 = IRQ mode, 1 = FIQ mode	0
[5]	R/W	**TIMERINT**	0 = IRQ mode, 1 = FIQ mode	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/W	**IMGVINT**	0 = IRQ mode, 1 = FIQ mode	0
[1]	R/W	**IMGHINT**	0 = IRQ mode, 1 = FIQ mode	0
[0]	R/W	**DISPINT**	0 = IRQ mode, 1 = FIQ mode	0

TABLE 8-3. INTERRUPT MODE REGISTER

8.2.6 INTERRUPT MASK REGISTER (INTMASK)

An interrupt source is related to each of the 24 bits in the mask register. CPU does not serve the interrupt request from the corresponding interrupt source when the specific bit is set to 1, even in the case of the corresponding SRCPND register bit is set to 1. The interrupt service is made when the mask bit is 0.

Address : C000 0808h

Bit	R/W	Symbol	Description	Reset Value
[31]	R/W	**I2SINT**	0 = Serviced, 1 = Masked	1
[30]	R/W	**MPEGIFINT**	0 = Serviced, 1 = Masked	1
[29]	R/W	**VIDEOINT**	0 = Serviced, 1 = Masked	1
[28]	R/W	**VLDINT**	0 = Serviced, 1 = Masked	1
[27]	R/W	**MCUCINT**	0 = Serviced, 1 = Masked	1
[26]	R/W	**DUALCPUINT**	0 = Serviced, 1 = Masked	1
[25]	R/W	**OWMINT**	0 = Serviced, 1 = Masked	1
[24]	R/W	**CDROMINT**	0 = Serviced, 1 = Masked	1
[23]	R/W	**GPIOINT**	0 = Serviced, 1 = Masked	1
[22]		**Reserved**	-	1
[21]		**Reserved**	-	1
[20]		**Reserved**	-	-
[19]	R/W	AC97**INT**	0 = Serviced, 1 = Masked	1
[18]	R/W	I^2C **INT**	0 = Serviced, 1 = Masked	1
[17]	R/W	**ADCINT**	0 = Serviced, 1 = Masked	1
[16]	R/W	**RTCINT**	0 = Serviced, 1 = Masked	1
[15]	R/W	**USBDINT**	0 = Serviced, 1 = Masked	1
[14]	R/W	**SDINT**	0 = Serviced, 1 = Masked	1
[13]	R/W	**USBHINT**	0 = Serviced, 1 = Masked	1
[12]	R/W	**SCALERINT**	0 = Serviced, 1 = Masked	1
[11]	R/W	**GRP2DINT**	0 = Serviced, 1 = Masked	1
[10]	R/W	**UARTINT**	0 = Serviced, 1 = Masked	1
[9]	R/W	**DMAINT**	0 = Serviced, 1 = Masked	1
[8]	R/W	**PPMINT**	0 = Serviced, 1 = Masked	1

Bit	R/W	Symbol	Description	Reset Value
[7]	R/W	**SSPINT**	0 = Serviced, 1 = Masked	1
[6]	R/W	**MSTICKINT**	0 = Serviced, 1 = Masked	1
[5]	R/W	**TIMERINT**	0 = Serviced, 1 = Masked	1
[4]		**Reserved**	-	1
[3]		**Reserved**	-	1
[2]	R/W	**IMGVINT**	0 = Serviced, 1 = Masked	1
[1]	R/W	**IMGHINT**	0 = Serviced, 1 = Masked	1
[0]	R/W	**DISPINT**	0 = Serviced, 1 = Masked	1

TABLE 8-4. INTERRUPT MASK REGISTER

8.2.7 INTERRUPT PRIORITY REGISTER(PRIORITY)

Address : C000 080Ch

Bit	R/W	Symbol	Description	Reset Value
[20:19]	R/W	**ARBSEL6**	Arbiter 6 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[18:17]	R/W	**ARBSEL5**	Arbiter 5 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
[16:15]	R/W	**ARBSEL4**	Arbiter 4 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[14:13]	R/W	**ARBSEL3**	Arbiter 3 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[12:11]	R/W	**ARBSEL2**	Arbiter 2 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[10:9]	R/W	**ARBSEL1**	Arbiter 1 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[8:7]	R/W	**ARBSEL0**	Arbiter 0 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
[6]	R/W	**ARBMODE6**	Arbiter 6 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1

Bit	R/W	Symbol	Description	Reset Value
[5]	R/W	**ARBMODE5**	Arbiter 5 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[4]	R/W	**ARBMODE4**	Arbiter 4 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[3]	R/W	**ARBMODE3**	Arbiter 3 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[2]	R/W	**ARBMODE2**	Arbiter 2 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[1]	R/W	**ARBMODE1**	Arbiter 1 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[0]	R/W	**ARBMODE0**	Arbiter 0 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1

TABLE 8-5. INTERRUPT PRIORITY REGISTER

8.2.8 INTERRUPT PENDING REGISTER (INTPEND)

In the interrupt pending register, each of the 24bits indicates if the corresponding interrupt request is the unmasked highest priority one and waits for the interrupt to be served. Only one bit can be set to 1 as INTPND is located after the priority logic, which is the interrupt request producing IRQ to CPU. This register can be read to determine the interrupt source to be served among 24 sources in interrupt service routine for IRQ.

Same as to the SRCPND, you must clear this register in the interrupt service routine after clearing SRCPND register. A specific INTPND register bit can be cleared by writing a data to this register. Only INTPND bit position corresponding to those set to '1' in the data can be cleared. The corresponding bit positions to those that are set to 0 in data remain unchanged.

NOTE : This register is only for the IRQ sources. This register does not show the FIQ request under being served.

Address : C000 0810

Bit	R/W	Symbol	Description	Reset Value
[31]	R/W	**I2SINT**	0 = Not requested, 1 = Requested	0
[30]	R/W	**MPEGIFINT**	0 = Not requested, 1 = Requested	0
[29]	R/W	**VIDEOINT**	0 = Not requested, 1 = Requested	0
[28]	R/W	**VLDINT**	0 = Not requested, 1 = Requested	0
[27]	R/W	**MCUCINT**	0 = Not requested, 1 = Requested	0
[26]	R/W	**DUALCPUINT**	0 = Not requested, 1 = Requested	0

Bit	R/W	Symbol	Description	Reset Value
[25]	R/W	**OWMINT**	0 = Not requested, 1 = Requested	0
[24]	R/W	**CDROMINT**	0 = Not requested, 1 = Requested	0
[23]	R/W	**GPIOINT**	0 = Not requested, 1 = Requested	0
[22]		**Reserved**	-	-
[21]		**Reserved**	-	-
[20]		**Reserved**	-	-
[19]	R/W	**AC97INT**	0 = Not requested, 1 = Requested	0
[18]	R/W	**I^2C INT**	0 = Not requested, 1 = Requested	0
[17]	R/W	**ADCINT**	0 = Not requested, 1 = Requested	0
[16]	R/W	**RTCINT**	0 = Not requested, 1 = Requested	0
[15]	R/W	**USBDINT**	0 = Not requested, 1 = Requested	0
[14]	R/W	**SDINT**	0 = Not requested, 1 = Requested	0
[13]	R/W	**USBHINT**	0 = Not requested, 1 = Requested	0
[12]	R/W	**SCALERINT**	0 = Not requested, 1 = Requested	0
[11]	R/W	**GRP2DINT**	0 = Not requested, 1 = Requested	0
[10]	R/W	**UARTINT**	0 = Not requested, 1 = Requested	0
[9]	R/W	**DMAINT**	0 = Not requested, 1 = Requested	0
[8]	R/W	**PPMINT**	0 = Not requested, 1 = Requested	0
[7]	R/W	**SSPINT**	0 = Not requested, 1 = Requested	0
[6]	R/W	**MSTICKINT**	0 = Not requested, 1 = Requested	0
[5]	R/W	**TIMERINT**	0 = Not requested, 1 = Requested	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/W	**IMGVINT**	0 = Not requested, 1 = Requested	0
[1]	R/W	**IMGHINT**	0 = Not requested, 1 = Requested	0
[0]	R/W	**DISPINT**	0 = Not requested, 1 = Requested	0

TABLE 8-6. INTERRUPT PENDING REGISTER

8.2.9 Interrupt Offset Register (INTOFFSET)

Interrupt request of IRQ mode in the INTPND register is shown by the number in the interrupt offset register. Clearing SRCPND and INTPND automatically clears this bit.

NOTE : The occurrence of the FIG mode will not affect INTOFFSET because the INTOFFSET register is available only for IRQ mode interrupt.

Address : C000 0814h

Bit	R/W	Symbol	Description	Reset Value
[4:0]	R	**OFFSET**	If INTPND[n] is set to 1 (due to interrupt requests from sources), number "n" is shown in INTOFFSET register. This is for the ease of interrupt target computation. Note that this value is valid if and only if a bit of INTPND is not 0.	0x00

TABLE 8-7. INTERRUPT OFFSET REGISTER

8.3 INTERRUPT CONTROLLER REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
SOURCE PENDING REGISTER (SRCPEND) ***Address : C000 0800h***				
[31]	R/C	**I2SINT**	0 = Not requested, 1 = Requested	0
[30]	R/C	**MPEGIFINT**	0 = Not requested, 1 = Requested	0
[29]	R/C	**VIDEOINT**	0 = Not requested, 1 = Requested	0
[28]	R/C	**VLDINT**	0 = Not requested, 1 = Requested	0
[27]	R/C	**MCUCINT**	0 = Not requested, 1 = Requested	0
[26]	R/C	**DUALCPUINT**	0 = Not requested, 1 = Requested	0
[25]	R/C	**OWMINT**	0 = Not requested, 1 = Requested	0
[24]	R/C	**CDROMINT**	0 = Not requested, 1 = Requested	0
[23]	R/C	**GPIOINT**	0 = Not requested, 1 = Requested	0
[22]		**Reserved**	-	-
[21]		**Reserved**	-	-
[20]		**Reserved**	-	-
[19]	R/C	**AC97INT**	0 = Not requested, 1 = Requested	0
[18]	R/C	I^2C **INT**	0 = Not requested, 1 = Requested	0
[17]	R/C	**ADCINT**	0 = Not requested, 1 = Requested	0
[16]	R/C	**RTCINT**	0 = Not requested, 1 = Requested	0

Bit	R/W	Symbol	Description	Reset Value
[15]	R/C	**USBDINT**	0 = Not requested, 1 = Requested	0
[14]	R/C	**SDINT**	0 = Not requested, 1 = Requested	0
[13]	R/C	**USBHINT**	0 = Not requested, 1 = Requested	0
[12]	R/C	**SCALERINT**	0 = Not requested, 1 = Requested	0
[11]	R/C	**GRP2DINT**	0 = Not requested, 1 = Requested	0
[10]	R/C	**UARTINT**	0 = Not requested, 1 = Requested	0
[9]	R/C	**DMAINT**	0 = Not requested, 1 = Requested	0
[8]	R/C	**PPMINT**	0 = Not requested, 1 = Requested	0
[7]	R/C	**SSPINT**	0 = Not requested, 1 = Requested	0
[6]	R/C	**MSTICKINT**	0 = Not requested, 1 = Requested	0
[5]	R/C	**TIMERINT**	0 = Not requested, 1 = Requested	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/C	**IMGVINT**	0 = Not requested, 1 = Requested	0
[1]	R/C	**IMGHINT**	0 = Not requested, 1 = Requested	0
[0]	R/C	**DISPINT**	0 = Not requested, 1 = Requested	0
INTERRUPT MODE REGISTER (INTMODE) ***Address : C000 0804h***				
[31]	R/W	**I2SINT**	0 = IRQ mode, 1 = FIQ mode	0
[30]	R/W	**MPEGIFINT**	0 = IRQ mode, 1 = FIQ mode	0
[29]	R/W	**VIDEOINT**	0 = IRQ mode, 1 = FIQ mode	0
[28]	R/W	**VLDINT**	0 = IRQ mode, 1 = FIQ mode	0
[27]	R/W	**MCUCINT**	0 = IRQ mode, 1 = FIQ mode	0
[26]	R/W	**DUALCPUINT**	0 = IRQ mode, 1 = FIQ mode	0
[25]	R/W	**OWMINT**	0 = IRQ mode, 1 = FIQ mode	0
[24]	R/W	**CDROMINT**	0 = IRQ mode, 1 = FIQ mode	0
[23]	R/W	**GPIOINT**	0 = IRQ mode, 1 = FIQ mode	0
[22]		**Reserved**	-	-
[21]		**Reserved**	-	-
[20]		**Reserved**	-	-
[19]	R/W	**AC97INT**	0 = IRQ mode, 1 = FIQ mode	0

Bit	R/W	Symbol	Description	Reset Value
[18]	R/W	**I²C INT**	0 = IRQ mode, 1 = FIQ mode	0
[17]	R/W	**ADCINT**	0 = IRQ mode, 1 = FIQ mode	0
[16]	R/W	**RTCINT**	0 = IRQ mode, 1 = FIQ mode	0
[15]	R/W	**USBDINT**	0 = IRQ mode, 1 = FIQ mode	0
[14]	R/W	**SDINT**	0 = IRQ mode, 1 = FIQ mode	0
[13]	R/W	**USBHINT**	0 = IRQ mode, 1 = FIQ mode	0
[12]	R/W	**SCALERINT**	0 = IRQ mode, 1 = FIQ mode	0
[11]	R/W	**GRP2DINT**	0 = IRQ mode, 1 = FIQ mode	0
[10]	R/W	**UARTINT**	0 = IRQ mode, 1 = FIQ mode	0
[9]	R/W	**DMAINT**	0 = IRQ mode, 1 = FIQ mode	0
[8]	R/W	**PPMINT**	0 = IRQ mode, 1 = FIQ mode	0
[7]	R/W	**SSPINT**	0 = IRQ mode, 1 = FIQ mode	0
[6]	R/W	**MSTICKINT**	0 = IRQ mode, 1 = FIQ mode	0
[5]	R/W	**TIMERINT**	0 = IRQ mode, 1 = FIQ mode	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/W	**IMGVINT**	0 = IRQ mode, 1 = FIQ mode	0
[1]	R/W	**IMGHINT**	0 = IRQ mode, 1 = FIQ mode	0
[0]	R/W	**DISPINT**	0 = IRQ mode, 1 = FIQ mode	0
INTERRUPT MASK REGISTER (INTMASK) ***Address : C000 0808h***				
[31]	R/W	**I2SINT**	0 = Serviced, 1 = Masked	1
[30]	R/W	**MPEGIFINT**	0 = Serviced, 1 = Masked	1
[29]	R/W	**VIDEOINT**	0 = Serviced, 1 = Masked	1
[28]	R/W	**VLDINT**	0 = Serviced, 1 = Masked	1
[27]	R/W	**MCUCINT**	0 = Serviced, 1 = Masked	1
[26]	R/W	**DUALCPUINT**	0 = Serviced, 1 = Masked	1
[25]	R/W	**OWMINT**	0 = Serviced, 1 = Masked	1
[24]	R/W	**CDROMINT**	0 = Serviced, 1 = Masked	1
[23]	R/W	**GPIOINT**	0 = Serviced, 1 = Masked	1

Bit	R/W	Symbol	Description	Reset Value
[22]		**Reserved**	-	1
[21]		**Reserved**	-	1
[20]	-	**Reserved**	-	-
[19]	R/W	**AC97INT**	0 = Serviced, 1 = Masked	1
[18]	R/W	**I^2C INT**	0 = Serviced, 1 = Masked	1
[17]	R/W	**ADCINT**	0 = Serviced, 1 = Masked	1
[16]	R/W	**RTCINT**	0 = Serviced, 1 = Masked	1
[15]	R/W	**USBDINT**	0 = Serviced, 1 = Masked	1
[14]	R/W	**SDINT**	0 = Serviced, 1 = Masked	1
[13]	R/W	**USBHINT**	0 = Serviced, 1 = Masked	1
[12]	R/W	**SCALERINT**	0 = Serviced, 1 = Masked	1
[11]	R/W	**GRP2DINT**	0 = Serviced, 1 = Masked	1
[10]	R/W	**UARTINT**	0 = Serviced, 1 = Masked	1
[9]	R/W	**DMAINT**	0 = Serviced, 1 = Masked	1
[8]	R/W	**PPMINT**	0 = Serviced, 1 = Masked	1
[7]	R/W	**SSPINT**	0 = Serviced, 1 = Masked	1
[6]	R/W	**MSTICKINT**	0 = Serviced, 1 = Masked	1
[5]	R/W	**TIMERINT**	0 = Serviced, 1 = Masked	1
[4]		**Reserved**	-	1
[3]		**Reserved**	-	1
[2]	R/W	**IMGVINT**	0 = Serviced, 1 = Masked	1
[1]	R/W	**IMGHINT**	0 = Serviced, 1 = Masked	1
[0]	R/W	**DISPINT**	0 = Serviced, 1 = Masked	1
INTERRUPT PRIORITY REGISTER(PRIORITY) ***Address : C000 080Ch***				
[20:19]	R/W	**ARBSEL6**	Arbiter 6 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[18:17]	R/W	**ARBSEL5**	Arbiter 5 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0

Bit	R/W	Symbol	Description	Reset Value
[16:15]	R/W	**ARBSEL4**	Arbiter 4 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[14:13]	R/W	**ARBSEL3**	Arbiter 3 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[12:11]	R/W	**ARBSEL2**	Arbiter 2 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[10:9]	R/W	**ARBSEL1**	Arbiter 1 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
[8:7]	R/W	**ARBSEL0**	Arbiter 0 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
[6]	R/W	**ARBMODE6**	Arbiter 6 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[5]	R/W	**ARBMODE5**	Arbiter 5 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[4]	R/W	**ARBMODE4**	Arbiter 4 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[3]	R/W	**ARBMODE3**	Arbiter 3 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[2]	R/W	**ARBMODE2**	Arbiter 2 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[1]	R/W	**ARBMODE1**	Arbiter 1 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
[0]	R/W	**ARBMODE0**	Arbiter 0 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
INTERRUPT PENDING REGISTER (INTPEND) **ADDRESS : C000 0810**				
[31]	R/W	**I2SINT**	0 = Not requested, 1 = Requested	0
[30]	R/W	**MPEGIFINT**	0 = Not requested, 1 = Requested	0
[29]	R/W	**VIDEOINT**	0 = Not requested, 1 = Requested	0
[28]	R/W	**VLDINT**	0 = Not requested, 1 = Requested	0
[27]	R/W	**MCUCINT**	0 = Not requested, 1 = Requested	0
[26]	R/W	**DUALCPUINT**	0 = Not requested, 1 = Requested	0

Bit	R/W	Symbol	Description	Reset Value
[25]	R/W	**OWMINT**	0 = Not requested, 1 = Requested	0
[24]	R/W	**CDROMINT**	0 = Not requested, 1 = Requested	0
[23]	R/W	**GPIOINT**	0 = Not requested, 1 = Requested	0
[22]		**Reserved**	-	-
[21]		**Reserved**	-	-
[20]	-	**Reserved**	-	-
[19]	R/W	**AC97INT**	0 = Not requested, 1 = Requested	0
[18]	R/W	**I^2C INT**	0 = Not requested, 1 = Requested	0
[17]	R/W	**ADCINT**	0 = Not requested, 1 = Requested	0
[16]	R/W	**RTCINT**	0 = Not requested, 1 = Requested	0
[15]	R/W	**USBDINT**	0 = Not requested, 1 = Requested	0
[14]	R/W	**SDINT**	0 = Not requested, 1 = Requested	0
[13]	R/W	**USBHINT**	0 = Not requested, 1 = Requested	0
[12]	R/W	**SCALERINT**	0 = Not requested, 1 = Requested	0
[11]	R/W	**GRP2DINT**	0 = Not requested, 1 = Requested	0
[10]	R/W	**UARTINT**	0 = Not requested, 1 = Requested	0
[9]	R/W	**DMAINT**	0 = Not requested, 1 = Requested	0
[8]	R/W	**PPMINT**	0 = Not requested, 1 = Requested	0
[7]	R/W	**SSPINT**	0 = Not requested, 1 = Requested	0
[6]	R/W	**MSTICKINT**	0 = Not requested, 1 = Requested	0
[5]	R/W	**TIMERINT**	0 = Not requested, 1 = Requested	0
[4]		**Reserved**	-	-
[3]		**Reserved**	-	-
[2]	R/W	**IMGVINT**	0 = Not requested, 1 = Requested	0
[1]	R/W	**IMGHINT**	0 = Not requested, 1 = Requested	0
[0]	R/W	**DISPINT**	0 = Not requested, 1 = Requested	0
Interrupt Offset Register (INTOFFSET) ***Address : C000 0814h***				
[4:0]	R	**OFFSET**	If INTPND[n] is set to 1 (due to interrupt requests from sources), number "n" is shown in INTOFFSET register. This is for the ease of interrupt target computation. Note that this value is valid if and only if a bit of INTPND is not 0.	0x00

TABLE 8-8. INTERRUPT CONTROLLER REGISTERS LIST

CHAPTER 9

TIMER/WATCH DOG TIMER

9. TIMER/WATCH DOG TIMER

9.1 OVERVIEW

The MP2520F has a 32-bit Timer that receives input from a 7.3728MHz clock. The TCOUNT register is a free-running up-counter. The Timer contains four 32-bit match registers - TMATCH0, TMATCH1, TMATCH2 and TMATCH3. All of these registers are read and write. If a value in the TCOUNT equals to the value in each match register (MA) and then relevant interrupt enable bit is set, the relevant bit of TSTATUS will also be set. These bits are coupled into an interrupt signal and attached to the interrupt controller.

TMATCH3 also operates as a watchdog timer register.

When watch dog timer enable bit (WDT_EN) in the TCONTROL register is set, watch dog function is enabled output of TMTCH3 will reset MP2520F when TMATCH3 bit is set. Before the CPU enables the FIQ and the IRQ, the TCOUNT register should be initialized and the TSTATUS should be cleared.

FEATURES

- 4-ch 32-bit Timers with 4 match registers
- Watch-dog Timer with reset function using TMATCH3 register

BLOCK DIAGRAM

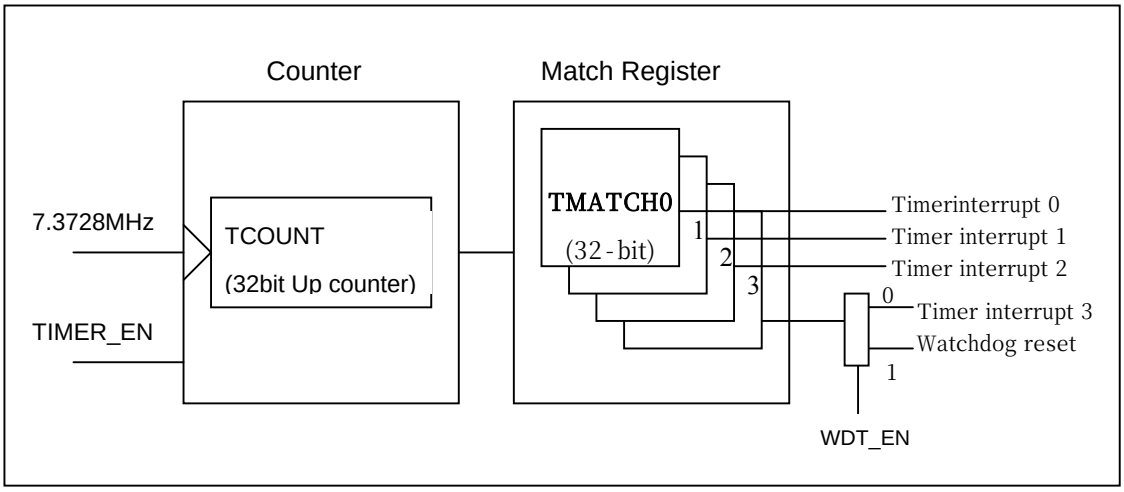


Figure 9-1. Timer Block Diagram

9.2 OPERATION

The Timer has one 32-bit free-running counter. The source clock is 7.3728 MHz OSC. If the CPU writes a TCOUNT register content, the count value increases by one every clock period. If the count value reaches ffff ffff, the next clock restarts from 0.

TIMER Counter REGISTER (TCOUNT)

Address : C000 0A00h

Bit	R/W	TCOUNT	Description	Reset Value
[31:0]	R/W	**TCOUNT**	Timer Counter Register This register will not be reloaded automatically, so the count will be restarted at 0 after a full count. One clock takes about 0.135uSec(1/7.3728MHz). In case of change TCOUNT Value, Follow next step 1. Reset TCOUNT Register by "0" 2. Input value what you want, after one clock Cf) If you want "0". First. In case of "0" input cummy value first and then input "0" after one Clock.	0

TABLE 9-1. TIMER COUNTER REGISTER

The Timer has 4 Match registers. When a Match register content coincides with the counter content, the relevant interrupt occurs. At this time, the relevant interrupt enable bit has to have been set already.

TIMER match 0 REGISTER (TMATCH0)

Address : C000 0A04h

Bit	R/W	TMATCH0	Description	Reset Value
[31:0]	R/W	**TMATCH0**	TIMER match 0 register	0

TABLE 9-2. TIMER MATCH 0 REGISTER

TIMER match 1 REGISTER (TMATCH1)

Address : C000 0A08h

Bit	R/W	TMATCH1	Description	Reset Value
[31:0]	R/W	**TMATCH1**	TIMER match 1 register	0

TABLE 9-3. TIMER MATCH 1 REGISTER

TIMER mach 2 REGISTER (TMATCH2)

Address : C000 0A0Ch

Bit	R/W	TMATCH2	Description	Reset Value
[31:0]	R/W	**TMATCH2**	TIMER match 2 register	0

TABLE 9-4. TIMER MATCH 2 REGISTER

TIMER match 3/Watch dog Timer REGISTER (TMATCH3)

Address : C000 0A10h

Bit	R/W	TMATCH3	Description	Reset Value
[31:0]	R/W	**TMATCH3**	TIMER match 3 register	0

TABLE 9-5. TIMER MATCH 3 / WATCH DOG TIMER REGISTER

Watchdog Timer Enable Register (TCONTROL)

In order to enable the Timer, the bit[0] of the TCONTROL must be set. If the TCONTROL[1] bit si set, the TMATCH3 register is available as a watchdog timer.

Address : C000 0A14h

Bit	R/W	TCONTROL	Description	Reset Value
[1]	R/W	**WDT_ EN**	Select timer 3 interrupt watchdog timer operation Timer 3 interrupt operates 0: Timer 3 interrupt 1: Watchdog reset	0
[0]	R/W	**TIMER_EN**	Timer block operation enable register 0: Timer counter disable, All timers[?] will stop. 1: Timer up-count enable	0

TABLE 9-6. WATCHDOG TIMER ENABLE REGISTER

Timer Status Register (TSTATUS)

The Timer interrupt status can be discovered by reading the TSTATUS register. The 0 to 3 bits of the register indicate that interrupts are initiated by the relevant match registers. Each interrupt is initiated by setting the relevant bit. If the relevant bit is set to 1, the interrupt status bit is cleared.

Address : C000 0A16h

Bit	R/W	TSTATUS	Description	Reset Value
[3]	R/W	**TSTATUS3**	Timer match 3 interrupt	0
[2]	R/W	**TSTATUS2**	Timer match 2 interrupt	0
[1]	R/W	**TSTATUS1**	Timer match 1 interrupt	0
[0]	R/W	**TSTATUS0**	Timer match 0 interrupt	0

TABLE 9-7. TIMER STATUS REGISTER

Timer Interrupt Enable Register (TINTEN)

To enable a timer interrupt, corresponding timer interrupt enable bit is set to 1

Address : C000 0A18h

Bit	R/W	TINTEN	Description	Reset Value
[3]	R/W	**TINTEN3**	Timer match 3 interrupt enable	0
[2]	R/W	**TINTEN2**	Timer match 2 interrupt enable	0
[1]	R/W	**TINTEN1**	Timer match 1 interrupt enable	0
[0]	R/W	**TINTEN0**	Timer match 0 interrupt enable	0

TABLE 9-8. TIMER INTERRUPT ENABLE REGISTER

9.3 TIMER / WATCH DOG TIMER REGISTER LIST

Bit	R/W	TCOUNT	Description	Reset Value
TIMER Counter REGISTER (TCOUNT) ***Address : C000 0A00h***				
[31:0]	RW	**TCOUNT**	Timer Counter Register This register will not be reloaded automatically, so the count will be restarted at 0 after a full count. One clock takes about 0.27uSec(1/7.3728MHz).	0
TIMER match 0 REGISTER (tmatch0) ***Address : C000 0A04h***				
[31:0]	RW	**TMATCH0**	TIMER match 0 register	0
TIMER match 1 REGISTER (tmatch1) ***Address : C000 0A08h***				
[31:0]	RW	**TMATCH1**	TIMER match 1 register	0
TIMER mach 2 REGISTER (tmatch2) ***Address : C000 0A0Ch***				
[31:0]	RW	**TMATCH2**	TIMER match 2 register	0
TIMER match 3/Watch dog Timer REGISTER (tmatch3) ***Address : C000 0A10h***				
[31:0]	RW	**TMATCH3**	TIMER match 3 register	0
Watchdog Timer Enable Register (tcontrol) ***Address : C000 0A14h***				
[1]	R/W	**WDT_ EN**	Select timer 3 interrupt watchdog timer operation Timer 3 interrupt operates 0: Timer 3 interrupt 1: Watchdog reset	0
[0]	R/W	**TIMER_EN**	Timer block operation enable register 0: Timer counter disable, All timers will stop. 1: Timer up-count enable	0
Timer Status Register (tstatus) ***Address : C000 0A16h***				
[3]	RW	**TSTATUS3**	Timer match 3 interrupt	0
[2]	RW	**TSTATUS2**	Timer match 2 interrupt	0
[1]	RW	**TSTATUS1**	Timer match 1 interrupt	0
[0]	RW	**TSTATUS0**	Timer match 0 interrupt	0

Bit	R/W	TCOUNT	Description	Reset Value
Timer Interrupt Enable Register (tinten) ***Address : C000 0A18h***				
[3]	RW	**TINTEN3**	Timer match 3 interrupt enable	0
[2]	RW	**TINTEN2**	Timer match 2 interrupt enable	0
[1]	RW	**TINTEN1**	Timer match 1 interrupt enable	0
[0]	RW	**TINTEN0**	Timer match 0 interrupt enable	0

TABLE 9-9. TIMER / WATCH DOG TIMER REGISTERS LIST

CHAPTER 10

UART

10. UART

10.1 OVERVIEW

Four independent asynchronous serial I/O (SIO) ports, each of which can operate in interrupt-based or DMA-based mode, are provided by the MP2520F UART (Universal Asynchronous Receiver and Transmitter) unit. That is, an interrupt or DMA request to transfer data between the CPU and UART can be generated by the UART. Bit rates of up to 3.1 Mbps can be supported by UART. Two 16-byte FIFOs are contained in each UART channel for receive and transmit.

Programmable baud-rates, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking are included in the MP2520F UART.

Fig 10-1 shows that baud-rate generator, transmitter, receiver and control unit are contained in each UART. PCLK can clock the baud-rate generator. The transmitter and the receiver contain 6-byte FIFOs and data shifters. Transmission data is written to FIFO and then copied to the transmit shifter. The transmit data pin (TXDn) then shifts out the data. The received data is shifted from the receive data pin (RXDn), and then copied to FIFO from the shifter.

FEATURES

- RXD0, TXD0, RXD1, TXD1, RXD2, TXD2, RXD3, TXD3 with DMA-based or interrupt-based operation
- UART Ch 1 or Ch2 with full modem function
- Supports handshake transmit / receive (UART Ch1 or Ch2)
- Ability to add or delete standard asynchronous communications bits (start, stop, and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate
- Modem control pins that allow flow control through software.
- Fully programmable serial-interface:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, and no parity detection
  - 1, or 2 stop bit generation
  - Baud rate generation up to around 3.1Mbps
- 16-byte transmit FIFO
- 16-byte receive FIFO
- Complete status reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include:
  - Loopback controls for communications link fault isolation
- Separate DMA requests for transmit and receive data services

BLOCK DIAGRAM

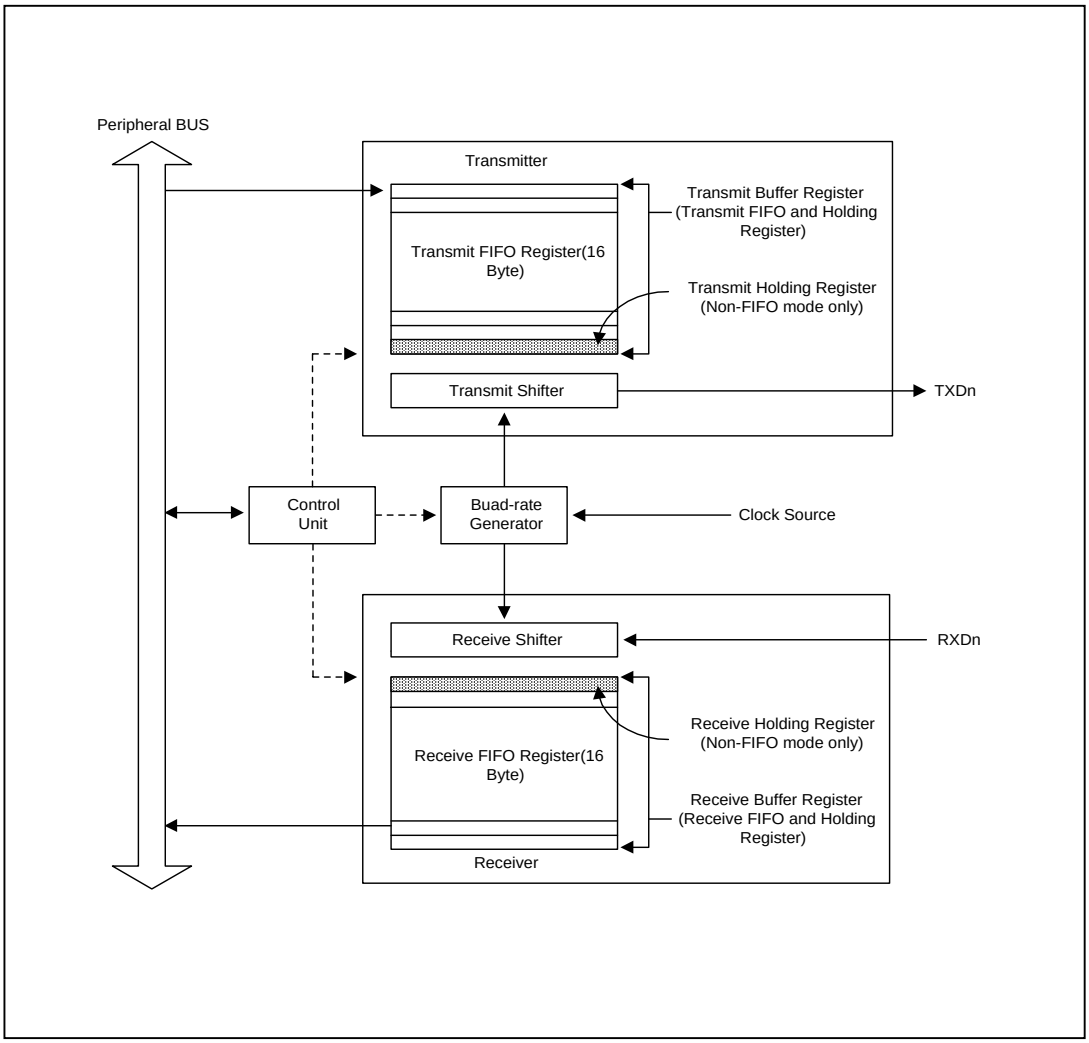


Figure 10-1. UART Block Diagram (with FIFO)

10.2 PIN DESCRIPTION

UART Pins		
TX0	O	UART0 Transmit Pin
RX0	I	UART0 Receive Pin
nRIO	I	UART1, UART2 Ring Indicator Pin
nDCD	I	UART1, UART2 Data-Carrier-Detect Pin
nDSR	I	UART1, UART2 Data-Set-Ready Pin
nDTR	O	UART1, UART2 Data-Terminal-Ready Pin
nCTS	I	UART1, UART2 Clear-To-Send Pin
nRTS	O	UART1, UART2 Ready-To-Send Pin
TX1	O	UART1 Transmit Pin
RX1	I	UART1 Receive Pin
RX2	I	UART2 Receive Pin
TX2	O	UART2 Transmit Pin
RX3	I	UART3 Receive Pin
TX3	O	UART3 Transmit Pin

TABLE 10-1. PIN DESCRIPTION TABLE

10.3 UART OPERATION

The UART operations that include Auto Flow Control, infra-red mode, loopback mode, baud-rate generation, interrupt generation, data reception, and data transmission are described in the following sections.

10.3.1 Data Transmission

For transmission the data frame is programmable. A start bit, 5 to 8 data bits, an optional parity bit, and 1 to 2 stop bits are included in the data frame, which can be specified by the Line Control Register (LCONn). The break conditions can also be produced by the transmitter. The serial out put is forced by the break condition to a logic 0 state for one frame transmission time. The break signal is transmitted by this block after the present transmission word transmits perfectly. Data are continuously transmitted into the TX FIFO (TX holding register in this case of non-FIFO mode) after the break signal transmission.

Break Condition

The break is defined as a continuous low level signal for one frame transmission time on the transmit data output.

10.3.2 Data Reception

Similar to the transmission, the data frame for reception is also programmable. The data frame for reception consists of a start bit, 5 to 8 data bits, an optional parity bit, and 1 to 2 stop bits in the Line Control Register LCONn). Overrun error, parity error, frame error and break condition, each of which can set an error flag, can be detected by the receiver.

- The fact that new data has overwritten the old data before the old has been read is indicated by the overrun error.
- The fact that the receiver has detected an unexpected parity condition is indicated by the parity error.
- The fact that the received data does not have a valid stop bit is indicated by the frame error.
- The fact that the RXDn input is held in the logic 0 state for a duration longer than one frame transmission time is indicated by the break condition.

Receive timeout condition occurs when the LCONn does not receive data during the value of timeout register word time (The setting of the Word Length bit is followed by this interval) and the RX FIFO is not empty in the FIFO mode.

10.3.3 Auto Flow Control(AFC)

In case MP2520F's UART would have to connect UART to UART, it supports Auto Flow Control with nRTS and nCTS signals. The AFC bit in the MCONn register is set to zero and control the signal of nRTS by software when users connect the UART to a modem.

In AFC, the condition of the receiver controls nRTS, and nCTS signal controls the operation of the transmitter.. In FIFO, the data is transferred by the UART's transmitter only when the nCTS signal is active (In AFC, nCTS means that the other UART's FIFO is ready to receive data.). nRTS must be activated when its receive FIFO has a spare more than 2-byte before the UART receives data and must be inactivated when its receive FIFO has a spare under 1-byte before the UART receives data (In AFC, nRTS means that its ownreceive FIFO is ready to receive data)

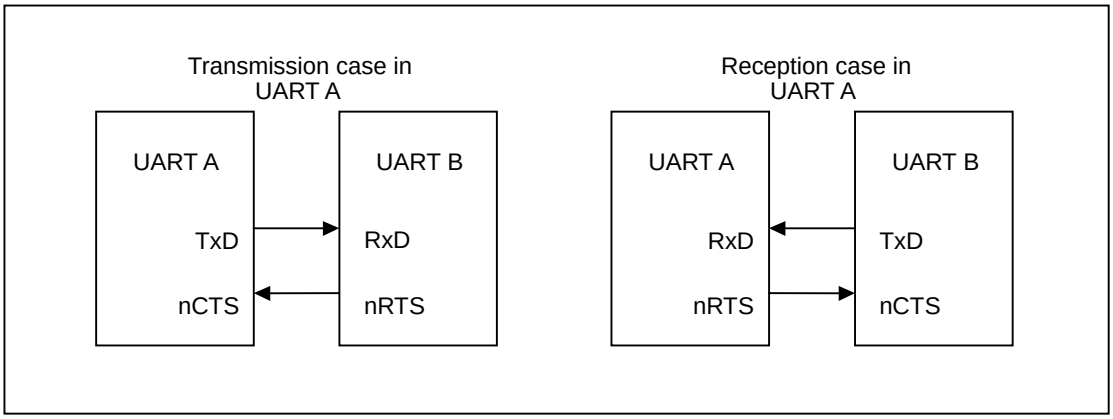


Figure 10-2. UART AFC interface

10.3.4 Non Auto-Flow control (Controlling nRTS and nCTS by S/W) Example

10.3.4.1 RX operation with FIFO

1. Select receive mode (Interrupt or DMA mode).
2. The value of RX FIFO count in FSTATUSn register is checked, and the user must set the value of RTS_ACTIVE (MCONn [0]) to '1' (active nRTS) when the value is less than 15, and the user must set the value to '0' (inactive nRTS) when the value is equal to or bigger than 15.
3. Repeat item 2.

10.3.4.2 TX operation with FIFO

1. Select transmit mode (Interrupt or DMA mode).
2. The value of CTS (MSTATUSn [0]) is checked. The user writes the data to the TX FIFO register when the value is '1' (nCTS is activated).

10.3.5 SIR (Serial Infra-Red) Mode

SIR (Serial Infra-red) transmission and reception are supported by the MP2520F UART, and can be selected by setting the SIR (Serial Infra-red mode bit) in UART Line Control Register (LCON1 or LCON2) and SIR signal control mode in the Serial Infra-red mode set register (UCONn) depending upon the IrDA transceiver type.

Then the UART block operates in the normal TX/RX mode. Figure 10-3 shows the implementation of the Sir mode.

The transmit period is pulsed at the normal serial transmit rate(when the transmit data bit is zero) of 3/16, in IR transmit mode.. The receive must detect the 3/6 pulsed period to recognize a zero value, in the IR receive mode (refer to the frame timing diagrams shown in Figures 10-5 and 10-6).

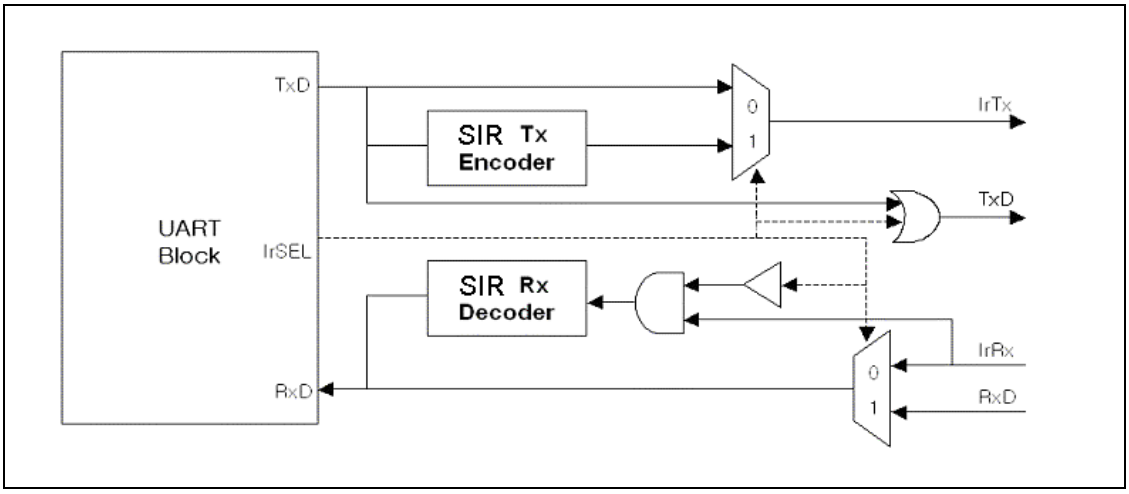


Figure 10-3. SIR Function Block Diagram

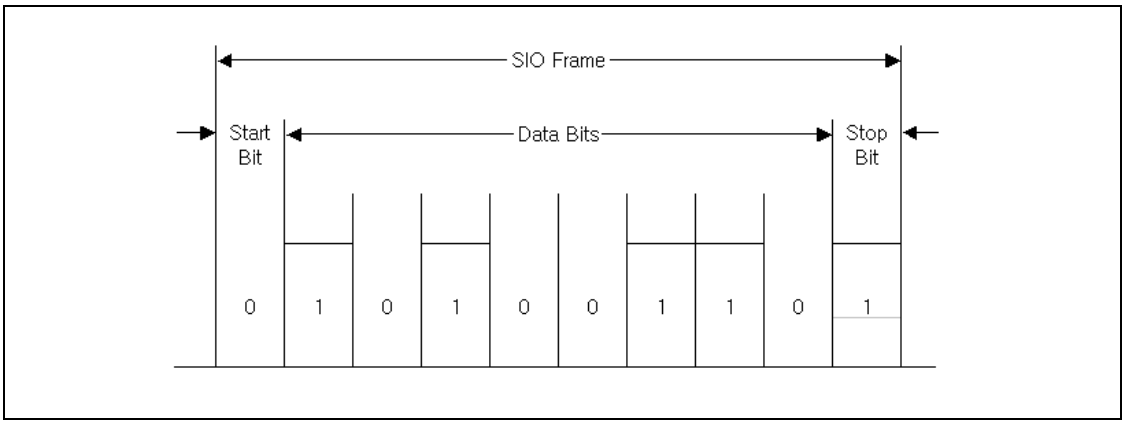


Figure 10-4. Serial I/O Frame Timing Diagram (Normal UART)

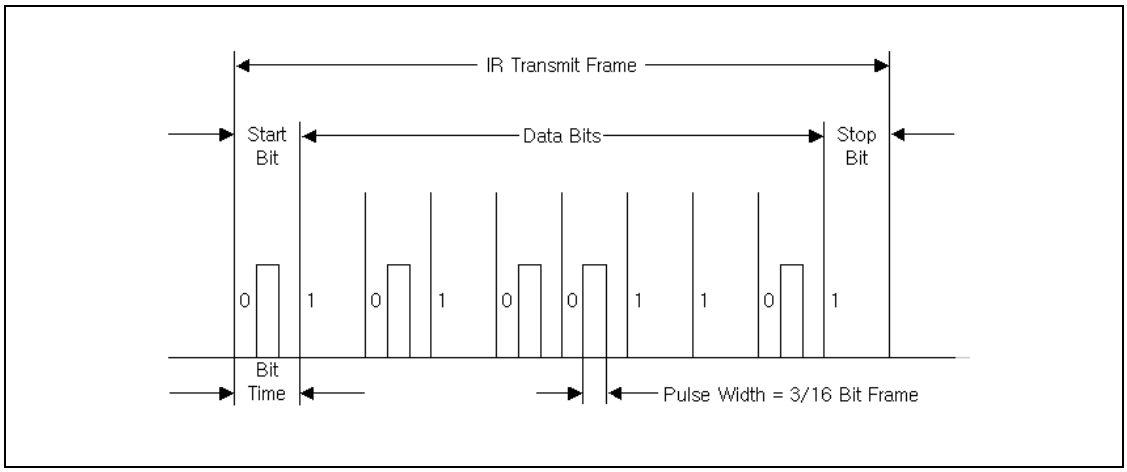


Figure 10-5. Infra-Red Transmit Mode Frame Timing Diagram

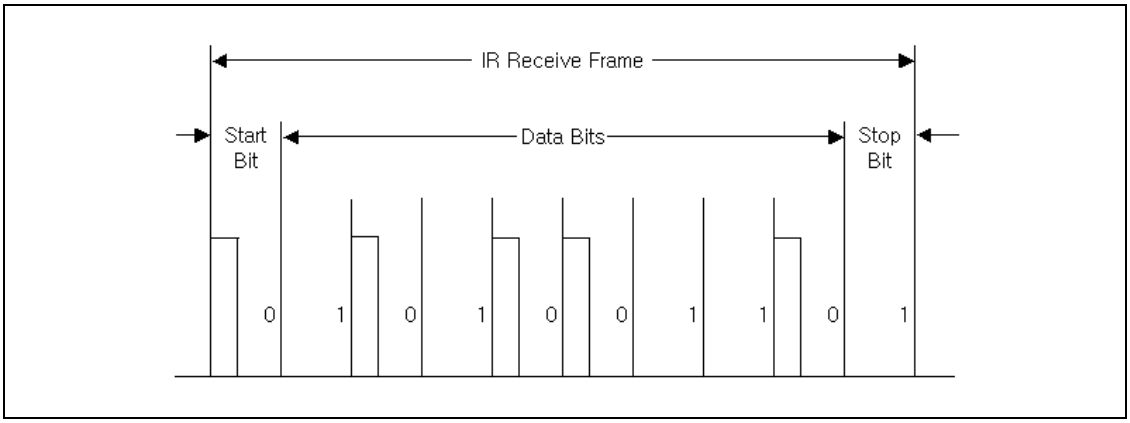


Figure 10-6. Infra-Red Receive Mode Frame Timing Diagram

10.3.6 Loop-back Mode

To aid in isolating faults in the communication link, the MP2520F UART provides a test mode referred to as the loopback mode. The transmitted data is immediately received in this mode. The processor is able to verify the internal transmit and receives the data path of each SIO channel due to this feature. Setting the loopback-bit in the UART control register (UCONn) will select this mode.

10.3.7 Modem Status Register Read

When the CTS is Active and the Delta CTS is High, the Modem Status Register becomes readable.

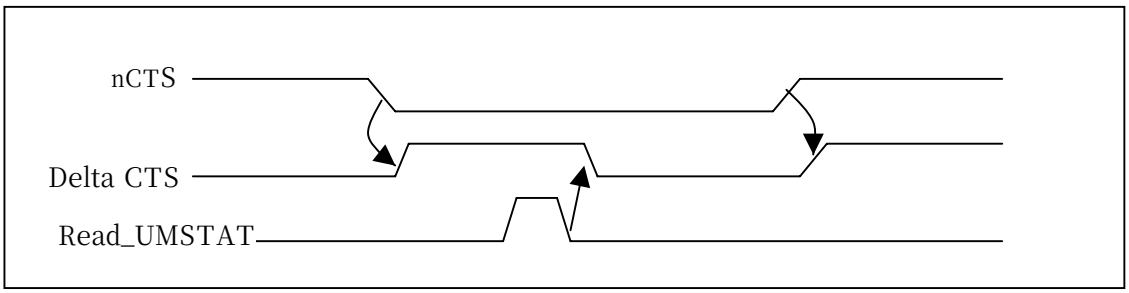


Figure 10-7. nCTS and Delta CTS Timing Diagram

10.3.8 RS-232C interface

The user needs nRTS, nCTS, nDSR, nDTR, DCD and nRI signals to connect to modem interface (not equal null modem).

10.3.9 Interrupt/DMA Request Generation

Each MP2520F UART consists of seven status (TX/RX/Error) signals, including Overrun error, Parity error, Frame error, Break, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (TRSSTATUSn/ESTATUSn).

The break condition, frame error, parity error, and overrun error are referred to as the receive error status, each of which can cause the receive error status interrupt request, if the RX ERRSTATUS (receive-error-status-interrupt-enable bit) is set to one in the control register UCONn. Reading ESTATUSn can identify the signal causing the request when a receive-error-status –interrupt-request is detected

When the data of the receiver shifter is transferred by the receiver to the receive FIFO and RX FIFO Trigger Level is reached by the number of received data, RX interrupt is generated if Receive mode in control register is selected as interrupt request or polling mode.

RX interrupt will be caused by transferring the data of the receive shifter to the receive FIFO under the Interrupt request and polling mode in the Non-FIFO mode.

When the data is transferred by the transmitter from its transmit FIFO to its transmit shifter and RX FIFO Trigger Level is reached by the number of data left in transmit FIFO, RX interrupt is generated if Transmit mode in UCONn (UART control register) is selected as Interrupt request or polling mode.

TX interrupt will be caused by transferring data from the transmit FIFO to the transmit shifter under the interrupt request and polling mode.

When the Receive and Transmit modes in UCONn (UART control register) are selected as the DMAn request mode, then instead of RX or TX interrupt in the situation mentioned above, DMAn request is
occured.

Type	FIFO Mode	Non-FIFO Mode
RX interrupt	Each time receive data reaches the trigger level of receive FIFO, the RX interrupt will be generated. When the number of data in FIFO does not reaches RX FIFO trigger Level and does not receive data during 3 word time(This interval follows the setting of Word Length bit), the RX interrupt will be generated(receive time out).	Each time receive data becomes full, the receive holding register generates an interrupt.
TX interrupt	Each time the transmit data reaches the trigger level of transmit FIFO(TX FIFO trigger Level), the TX interrupt will be generated.	Each time the transmit data becomes empty, the transmit holding register generates an interrupt.
Error interrupt	Frame error, parity error, and break signal are detected, and will generate an error interrupt. When it gets to the top of the receive FIFO without reading out data in it, the error interrupt will be generated(overrun error).	All errors generate an error interrupt immediately. However if another error occurs at the same time, only one interrupt is generated.

TABLE 10-2. INTERRUPTS IN CONNECTION WITH FIFO

10.3.10 UART ERROR STATUS FIFO

UART has the status FIFO in addition to the RX FIFO register. The status FIFO indicates which data, among FIFO registers, is received with an error. Only when the error having data is ready to read out, the error interrupt will be issued. The RHBn (Buffer or Received data) with an error and ESTATUSn must be read out to clear the status FIFO. Even if the RHBn is read out instead of the ESTATUSn, the Error Status IO is cleared.

For example,

The fact that the UART FIFO receives A, B, C, D, E characters sequentially and the frame error occurs while receiving 'B', and the parity error occurs while receiving 'D' is assumed.

The error interrupt will not be generated even though the actual UART error occurred because the character, which was received with an error, has not been read yet. The error interrupt will be occurred when the character is read out.

The address of the Error Status FIFO has been synchronized with the address of the Rx-FIFO.

Time	Sequence flow	Error interrupt	Note
#0	When no character is read out	–	
#1	After A is read out	The frame error(in B) interrupt occurs	The 'B' has to be read out
#2	After B is read out	–	
#3	After C is read out	The parity error(in D) interrupt occurs	The 'D' has to be read out
#4	After D is read out	–	
#5	After E is read out	–	

TABLE 10-3. ERROR INTERRUPTS TABLE

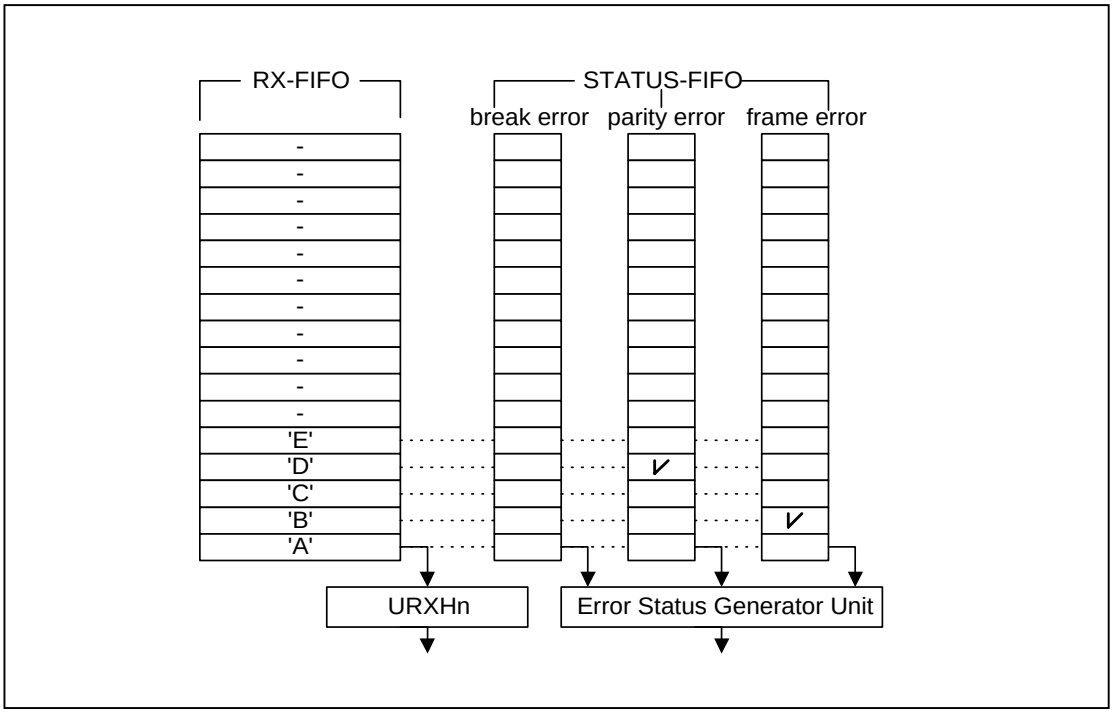


Figure 10-8. A Case showing UART Receiving 5 Characters with 2 Errors

10.3.11 BAUD-RATE GENERATION

The serial clock for transmitter and receiver are provided by each UART's baud-rate generator. The baud-rate generating source clock can be selected with the MP250F's internal system clock.. Dividing the source clock by 16 and a 16-bit divisor specified in the UART baud-rate divisor register (BRDn) generate the baud-rate clock. The following formula can determine the BRDn:

BRDn = (int) (PCLK/(bps x 16))

where the divisor is from 1 to (216-1). For example, when the baud-rate is 115,200 bps and PCLK is 40 MHz, BRDn is as follows:

BRDn = (int)(40,000,000/(115,200 x 16)) -1
= (int)(21.7) -1
= 21 – 1 = 20

10.4 UART REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
LINE CONTROL REGISTER (LCON0, LCON1, LCON2, LCON3) ***Address : C000 1200h / C000 1220h / C000 1240h / C000 1260h***				
[15:7]	-	**Reserved**	-	-
[6]	R/W	**SIR_MODE**	The Serial Infra-Red mode determines whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red SIR TX/RX mode	0
[5:3]	R/W	**PARITY_MODE**	The parity mode specifies how parity generation and checking are to be performed during the UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	0
[2]	R/W	**STOPBIT**	The number of stop bits - specifies how many stop bits are to be used to signal end-of-frame. 0 = One stop bit per frame 1 = Two stop bit per frame	0
[1:0]	R/W	**WORD_LEN**	The word length indicates the number of data bits to be transmitted or received per frame. 00 = 5-bits 01 = 6-bits 10 = 7-bits 11 = 8-bits	0
CONTROL REGISTER (UCON0, UCON1, UCON2, UCON3) ***Address : C000 1202h / C000 1222h / C000 1242h / C000 1262h***				
[9]	R/W	**TX_INT**	Interrupt request type 0 = Pulse (Interrupt is requested as soon as TX buffer becomes empty in Non-FIFO mode or TX FIFO reaches Trigger Level in FIFO mode) 1 = Level (Interrupt is requested while TX buffer is empty in Non-FIFO mode or TX FIFO reached in Trigger Level in FIFO mode)	0
[8]	R/W	**RX_INT**	Interrupt request type 0 = Pulse (Interrupt is requested the instant RX buffer receives the data in Non-FIFO mode or reaches RX FIFO Trigger Level in FIFO mode) 1 = Level (Interrupt is requested while RX buffer is receiving data in Non-FIFO mode or reaches RX FIFO Trigger Level in FIFO mode)	0
[7]	R/W	**RX_TIMEOUT**	Enable/Disable RX time out interrupt when UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disable 1 = Enable	0
[6]	R/W	**RX_ERRSTATUS**	This bit enables the UART to generate an interrupt if an exception, such as a	0

Bit	R/W	Symbol	Description	Reset Value
			break, frame error, parity error, or overrun error occurs during a receive operation. 0 = Do not generate 1 = Generate	
[5]	R/W	**LOOPBACK_MODE**	Setting loop-back bit to 1 cause the UART to enter the loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode	0
[4]	R/W	**SEND_BREAK**	Setting this bit causes the UART to send a break during 1 frame time (auto-cleared after sending the break signal). 0 = Normal transmit 1 = Send break signal	0
[3:2]	R/W	**TRANS_MODE**	These two bits determine which function is currently able to write TX data to the UART transmit buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request 11 = RESERVED	0
[1:0]	R/W	**RECEIVE_MODE**	These two bits determine which function is currently able to read data from UART receive buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request 11= RESERVED	0
FIFO CONTROL REGISTER (FCON0, FCON1, FCON2, FCON3) ***Address : C000 1204h / C000 1224h / C000 1244h / C000 1264h***				
[15:8]	-	**Reserved**	-	-
[7:6]	R/W	**TX_FIFO_TRIGGER**	These two bits determine the trigger level of transmit FIFO. 00 = Empty 01 = 4-byte 10 = 8-byte 11 = 12-byte	0
[5:4]	R/W	**RX_FIFO_TRIGGER**	These two bits determine the trigger level of receive FIFO. 00 = 4byte 01 = 8byte 10 = 12byte 11 = 15byte ex)If the register value of RX_FIFO_TRIGGER is set to "00" and FIFO is set upto 4byte, an interrupt will be taken place	0
[3]	-	**Reserved**		0
[2]	R/W	**TX_FIFO_RESET**	This bit is auto-cleared after resetting FIFO. 0 = Normal 1= TX FIFO reset	0
[1]	R/W	**RX_FIFO_RESET**	This bit is auto-cleared after resetting FIFO. 0 = Normal 1= RX FIFO reset	0
[0]	R/W	**FIFO_EN**	0 = FIFO disable 1 = FIFO mode	0
NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the RX interrupt will be generated (receive timeout), and the users should check the FIFO status and read out the rest.				
MODEM CONTROL REGISTER (MCON0, MCON1, MCON2, MCON3) ***Address : C000 1206h / C000 1226h / C000 1246h / C000 1266h***				
[15:5]	-	**Reserved**	-	-

Bit	R/W	Symbol	Description	Reset Value
[4]	R/W	**AFC**	0 = Disable 1 = Enable	0
[3]	R/W	**MODEM_INT**	0 = Disable 1 = Enable	0
[2]	-	**Reserved**	These bits must be 0's	-
[1]	R/W	**DTR_ACTIVE**	0 = Inactive 1 = Active	0
[0]	R/W	**RTS_ACTIVE**	If the AFC bit is enabled, this value will be ignored. In this case the MP2520F will control nRTS automatically. If the AFC bit is disabled, nRTS must be controlled by S/W. 0 = 'H' level(Inactivate nRTS) 1 = 'L' level(Activate nRTS)	0
TX/RX STATUS REGISTER (TRSTATUS0, TRSTATUS1, TRSTATUS2, FTSTATUS3) ***Address : C000 1208h / C000 1228h / C000 1248h / C000 1268h***				
[15:3]	-	**Reserved**	-	-
[2]	R	**TRANSMITTER_EMPTY**	This bit is automatically set to 1 when the transmit buffer register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmit buffer & shifter register empty	1
[1]	R	**TRANSMIT_BUFFER_EMPTY**	This bit is automatically set to 1 when the transmit buffer register is empty. 0 =The buffer register is not empty 1 = Empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested when TX FIFO Trigger Level is set to 00 (Empty)) If the UART uses the FIFO, users should check TX FIFO Count bits and TX FIFO Full bit in the UFSTAT register instead of this bit.	1
[0]	R	**RECEIVE_BUFFER_DATA_READY**	This bit is automatically set to 1 whenever the receive buffer register contains valid data received over the RXDn port. 0 = Empty 1 = The buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If the UART uses the FIFO, users should check RX FIFO Count bits and RX FIFO Full bit in the UFSTAT register instead of this bit.	0
ERROR STATUS REGISTER (ESTATUS0, ESTATUS1, ESTATUS2, ESTATUS3) ***Address : C000 120Ah / C000 122Ah / C000 124Ah / C000 126Ah***				
[15:4]	-	**Reserved**	-	-

Bit	R/W	Symbol	Description	Reset Value
[3]	R	**BREAK_DETECT**	This bit is automatically set to 1 to indicate that a break signal has been received. 0 = No break receive 1 = Break receive(Interrupt is requested)	0
[2]	R	**FRAME_ERROR**	This bit is automatically set to 1 whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error(Interrupt is requested)	0
[1]	R	**PARITY_ERROR**	This bit is automatically set to 1 whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error(Interrupt is requested)	0
[0]	R	**OVERRUN_ERROR**	This bit is automatically set to 1 whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error(Interrupt is requested)	0
NOTE: These bits (ESTATUSn[3:0]) are automatically cleared to 0 when the UART error status register is read.				
FIFO STATUS REGISTER (FSTATUS0, FSTATUS1, FSTATUS2, FSTATUS3) ***Address : 7000 120Ch / 7000 122Ch / 7000 124Ch / 7000 126Ch***				
[15:11]	-	**Reserved**	-	-
[10]	R	**RX_FIFO_ERROR**	Error in RX FIFO detect 0 = No error receive 1 = Error receive	0
[9]	R	**TX_FIFO_FULL**	This bit is automatically set to 1 whenever Transmit FIFO is full during transmit operation 0 = 0-byte ≤ TX FIFO data ≤ 15-byte 1 = Full	0
[8]	R	**RX_FIFO_FULL**	This bit is automatically set to 1 whenever Receive FIFO is full during receive operation 0 = 0-byte ≤ RX FIFO data ≤ 15-byte 1 = Full	0
[7:4]	R	**TX_FIFO_COUNT**	Number of data in TX FIFO	0
[3:0]	R	**RX_FIFO_COUNT**	Number of data in RX FIFO	0
MODEM STATUS REGISTER (MSTATUS0, MSTATUS1, MSTATUS2, MSTATUS3) ***Address : C000 120Eh / C000 122Eh / C000 124Eh / C000 126Eh***				
[15:8]	-	**Reserved**	-	-
[7]	R	**DELTA_DCD**	Delta DCD input 0 = Has not changed	0

Bit	R/W	Symbol	Description	Reset Value
			1 = Has changed	
[6]	R	**DELTA_RI**	Delta RI input 0 = Has not changed 1 = Has changed	0
[5]	R	**DELTA_DSR**	Delta DSR(Data Set Ready) input 0 = Has not changed 1 = Has changed	0
[4]	R	**DELTA_CTS**	Delta CTS input This bit indicates that the nCTS input to MP2520F has changed state since the last time it was read by the CPU. (Refer to Figure 10-8) 0 = Has not changed 1 = Has changed	0
[3]	R	**DCD**	DCD(Data Carrier Detect) input	0
[2]	R	**RI**	RI(Ring Indicator) input	0
[1]	R	**DSR**	DSR(Data Set Ready) input	0
[0]	R	**CTS**	CTS(Clear to Send) input 0 = CTS signal is not activated(nCTS pin is high) 1 = CTS signal is activated(nCTS pin is low)	0
TRANSMIT BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER) **THBn has an 8-bit data for transmission data (THB0, THB1, THB2, THB3)** ***Address : C000 1210h / C000 1230h / C000 1250h / C000 1270h***				
[7:0]	w	**THBn**	Transmit data for UARTn	0
RECEIVE BUFFER EGISTER (HOLDING REGISTER & FIFO REGISTER) **RHBn has an 8-bit data for received data (RHB0)** ***Address : C000 1212h***				
[7:0]	R	**RHB0**	Receive data for UART0	0
RHBn has an 8-bit data for received data (RHB1) ***Address : C000 1232h***				
[7:0]	R	**RHB1**	Receive data for UART1	0
RHBn has an 8-bit data for received data (RHB2) ***Address : C000 1252h***				
[7:0]	R	**RHB2**	Receive data for UART2	0
RHBn has an 8-bit data for received data (RHB3) ***Address : C000 1272h***				
[7:0]	R	**RHB3**	Receive data for UART3	0
NOTE: When an overrun error occurs, the RHBn must be read. If not, the next received data will also make an overrun error, even though the overrun bit of ESTATUSn had been cleared.				

Bit	R/W	Symbol	Description	Reset Value
The value stored in the baud rate divisor register (BRD0) ***Address : C000 1214h***				
[15:0]	R	**BRD0**	Baud rate division value BRD0>0	-
The value stored in the baud rate divisor register (BRD1) ***Address : C000 1234h***				
[15:0]	R	**BRD1**	Baud rate division value BRD1>0	-
The value stored in the baud rate divisor register (BRD2) ***Address : C000 1254h***				
[15:0]	R	**BRD2**	Baud rate division value BRD2>0	-
The value stored in the baud rate divisor register (BRD3) ***Address : C000 1274h***				
[15:0]	R	**BRD3**	Baud rate division value BRD3>0	-
RECEIVE TIMEOUT REGISTER **There are four UART receive timeout registers (TIMEOUTREG0)** ***Address : C000 1216h***				
[15:0]	R/W	**TIMEOUTREG 0**	Receive time out period value	0x001f
There are four UART receive time out registers (TIMEOUTREG1) *Address : C000 1236h*				
[15:0]	R/W	**TIMEOUTREG 1**	Receive timeout period value	0x001f
There are four UART receive time out registers (TIMEOUTREG2) ***Address : C000 1256h***				
[15:0]	R/W	**TIMEOUTREG 2**	Receive timeout period value	0x001f
There are four UART receive time out registers (TIMEOUTREG3) ***Address : C000 1276h***				
[15:0]	R/W	**TIMEOUTREG3**	Receive timeout period value	0x001f
INTERRUPT STATUS REGISTER **There are one UART interrupt status registers (INTSTATREG).** ***Address : C000 1280h***				
[15]	R/W	**MODEM 3**	UART channel 3 Modem interrupt	0x00
[14]	R/W	**ERROR3**	UART channel 3 Error interrupt	0x00
[13]	R/W	**RXD3**	UART channel 3 Receive interrupt	0x00

Bit	R/W	Symbol	Description	Reset Value
[12]	R/W	**TXD3**	UART channel 3 Transmit interrupt	0x00
[11]	R/W	**MODEM2**	UART channel 2 Modem interrupt	0x00
[10]	R/W	**ERROR2**	UART channel 2 Error interrupt	0x00
[9]	R/W	**RXD2**	UART channel 2 Receive interrupt	0x00
[8]	R/W	**TXD2**	UART channel 2 Transmit interrupt	0x00
[7]	R/W	**MODEM1**	UART channel 1 Modem interrupt	0x00
[6]	R/W	**ERROR1**	UART channel 1 Error interrupt	0x00
[5]	R/W	**RXD1**	UART channel 1 Receive interrupt	0x00
[4]	R/W	**TXD1**	UART channel 1 Transmit interrupt	0x00
[3]	R/W	**MODEM0**	UART channel 0 Modem interrupt	0x00
[2]	R/W	**ERROR0**	UART channel 0 Error interrupt	0x00
[1]	R/W	**RXD0**	UART channel 0 Receive interrupt	0x00
[0]	R/W	**TXD0**	UART channel 0 Transmit interrupt	0x00
PORT CONTROL REGISTER **There are one UART port control registers (PORTCON)** ***Address : C000 1282h***				
[1]	R/W	**RTS**	'0' : UART1 use RTS '1' : UART2 use RTS	0x00
[0]	R/W	**DTS**	'0' : UART1 use DTS '1' : UART2 use DTS	0x00

TABLE 10-4. UART INTERRUPT REGISTERS LIST

CHAPTER 11

GENERAL PURPOSE I/0 (GPIO)

11. GENERAL PURPOSE I/O (GPIO)

11.1 OVERVIEW

The MP2520F has 189 pins of general-purpose I/O (GPIO). All GPIO pins can be set as an input or an output. If a pin is set as an input, it can be used as an input source. GPIO consists of 15 groups, and the numbers of pins by group are shown below.

GPIO Group	Pins	GPIO Group	Pins
GPIOA	16	GPIOI	16
GPIOB	16	GPIOJ	16
GPIOC	16	GPIOK	8
GPIOD	14	GPIOL	15
GPIOE	16	GPIOM	9
GPIOF	10	GPION	8
GPIOG	16	GPIOO	6
GPIOH	7		

TABLE 11-1. GPIO PIN GROUP

After reset, all GPIO pins, excluding GPIOD[1:0], GPIOE[15:8], GPIOF[9:0], GPIOG[15:0], GPIOH[0], GPIOI[15:0], GPIOJ[15:0] and GPIOL[10], are set as GPIO inputs. The initial values of the excluded pins are as follows:

GPIOD[1:0] : Alt Function 1

GPIOE[15:8] : Alt Function 1 for SRAM Boot and 16-bit SRAM Bus Width. GPIO Input elsewhere.

GPIOF[9:0] : Alt Function 1 for SRAM Boot. GPIO input elsewhere.

GPIOG[15:0] : Alt Function 1 for SRAM Boot. GPIO input elsewhere.

If the GPIO Alt Function Register is set, the GPIO pins are used for the alternative function. In the Stop mode, the states of all pins, except for the GPIOE, the GPIOF, the GPIOG, the GPIOI, and the GPIOJ pins, are determined by the values of GPIO Alt Function Registers and GPIO Output Registers. The states of the
GPIOE, the GPIOF, the GPIOG, the GPIOI, and the GPIOJ pins are subject to the value of the GPIO Alive Register.

BLOCK DIAGRAM

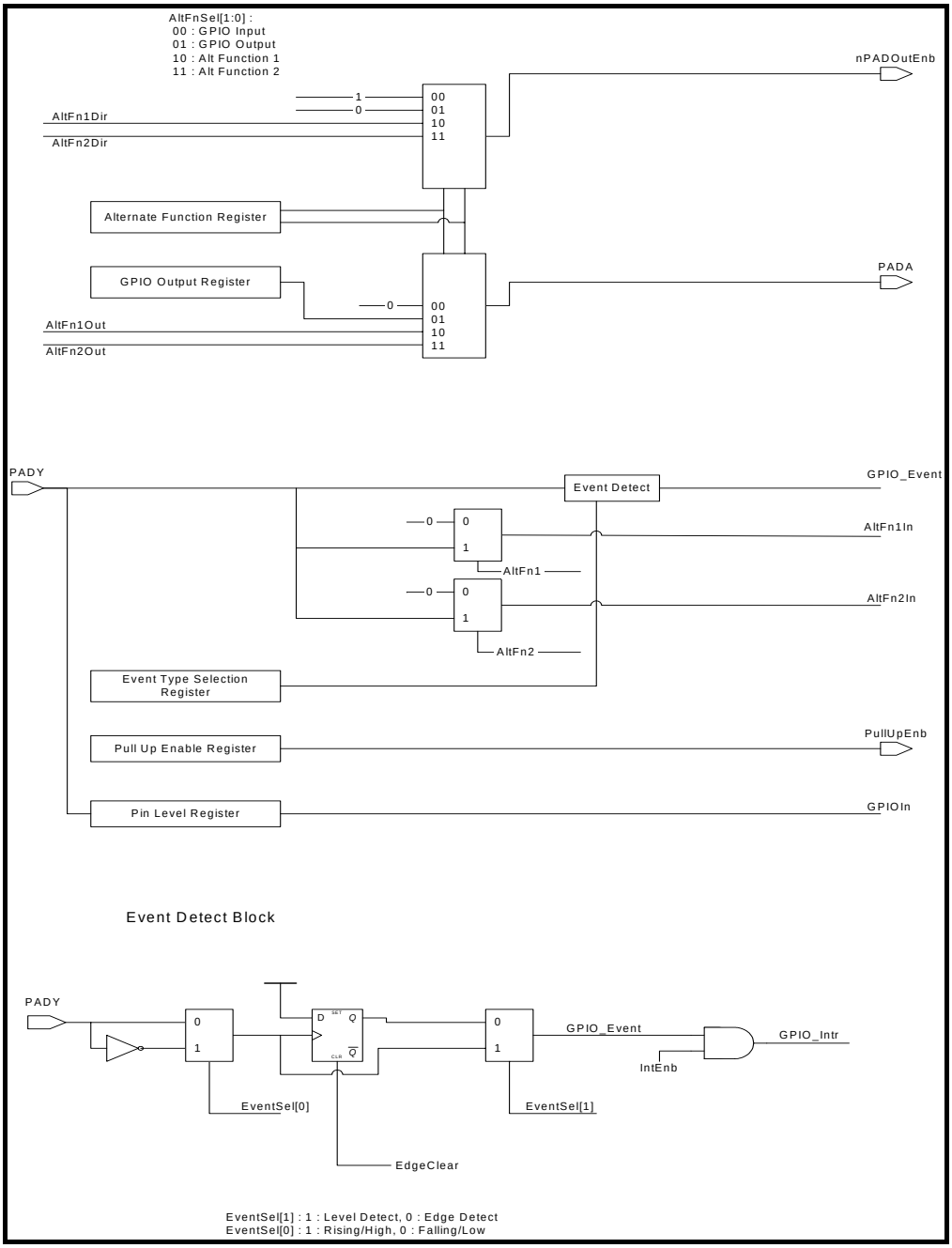


Figure 11-1. GPIO Block Diagram

11.2 GPIO OPERATION

GPIOA Alternate Function High Register (GPIOAALTFNHI)

This Register selects the function of the GPIOA MSB 16-bit. Two register bits are allocated to GPIOA pin.

Address : 0xC0001040h *GPIOAALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOA15_ALTFN**	**GPIOA[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOA14_ALTFN**	**GPIOA[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOA13_ALTFN**	**GPIOA[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOA12_ALTFN**	**GPIOA[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOA11_ALTFN**	**GPIOA[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOA10_ALTFN**	**GPIOA[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOA9_ALTFN**	**GPIOA[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOA8_ALTFN**	**GPIOA[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-2. GPIOA ALTERNATE FUNCTION HIGH REGISTER

GPIOA Alternate Function Low Register (GPIOAALTFNLOW)

This Register selects the function of the GPIOA LSB 16-bit. Two register bits are allocated to GPIOA pin.

Address : 0xC0001020h *GPIOAALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOA7_ALTFN**	**GPIOA[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOA6_ALTFN**	**GPIOA[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOA5_ALTFN**	**GPIOA[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOA4_ALTFN**	**GPIOA[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOA3_ALTFN**	**GPIOA[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOA2_ALTFN**	**GPIOA[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOA1_ALTFN**	**GPIOA[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOA0_ALTFN**	**GPIOA[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-3. GPIOA ALTERNATE FUNCTION LOW REGISTER

GPIOB Alternate Function High Register (GPIOBALTFNHI)

This Register selects the function of the GPIOB MSB 16-bit. Two register bits are allocated to GPIOB pin.

Address : 0xC0001042h *GPIOBALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOB15_ALTFN**	**GPIOB[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOB14_ALTFN**	**GPIOB[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOB13_ALTFN**	**GPIOB[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOB12_ALTFN**	**GPIOB[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOB11_ALTFN**	**GPIOB[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOB10_ALTFN**	**GPIOB[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOB9_ALTFN**	**GPIOB[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOB8_ALTFN**	**GPIOB[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-4. GPIOB ALTERNATE FUNCTION HIGH REGISTER

GPIOB Alternate Function Low Register (GPIOBALTFNLOW)

This Register selects the function of the GPIOB LSB 16-bit. Two register bits are allocated to GPIOB pin.

Address : 0xC0001022h *GPIOBALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOB7_ALTFN**	**GPIOB[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOB6_ALTFN**	**GPIOB[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOB5_ALTFN**	**GPIOB[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOB4_ALTFN**	**GPIOB[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOB3_ALTFN**	**GPIOB[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOB2_ALTFN**	**GPIOB[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOB1_ALTFN**	**GPIOB[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOB0_ALTFN**	**GPIOB[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-5. GPIOB ALTERNATE FUNCTION LOW REGISTER

GPIOC Alternate Function High Register (GPIOCALTFNHI)

This Register selects the function of the GPIOC MSB 16-bit. Two register bits are allocated to GPIOC pin.

Address : 0xC0001044h *GPIOCALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOC15_ALTFN**	**GPIOC[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOC14_ALTFN**	**GPIOC[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOC13_ALTFN**	**GPIOC[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOC12_ALTFN**	**GPIOC[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOC11_ALTFN**	**GPIOC[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOC10_ALTFN**	**GPIOC[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOC9_ALTFN**	**GPIOC[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOC8_ALTFN**	**GPIOC[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-6. GPIOC ALTERNATE FUNCTION HIGH REGISTER

GPIOC Alternate Function Low Register (GPIOCALTFNLOW)

This Register selects the function of the GPIOC LSB 16-bit. Two register bits are allocated to GPIOC pin.

Address : 0xC0001024h *GPIOCALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOC7_ALTFN**	**GPIOC[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOC6_ALTFN**	**GPIOC[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOC5_ALTFN**	**GPIOC[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOC4_ALTFN**	**GPIOC[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOC3_ALTFN**	**GPIOC[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOC2_ALTFN**	**GPIOC[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOC1_ALTFN**	**GPIOC[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOC0_ALTFN**	**GPIOC[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-7. GPIOC ALTERNATE FUNCTION LOW REGISTER

GPIOD Alternate Function High Register (GPIODALTFNHI)

***** Register (GPIODALTFNHI, GPIODALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOD MSB 16-bit. Two register bits are allocated to GPIOD pin.

Address : 0xC0001046h *GPIODALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	Reserved	-	-
[13:12]	-	Reserved	-	-
[11:10]	W	GPIOD13_ALTFN	GPIOD[13] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	GPIOD12_ALTFN	GPIOD[12] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	GPIOD11_ALTFN	GPIOD[11] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	GPIOD10_ALTFN	GPIOD[10] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	GPIOD9_ALTFN	GPIOD[9] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	GPIOD8_ALTFN	GPIOD[8] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-8. GPIOD ALTERNATE FUNCTION HIGH REGISTER

GPIOD Alternate Function Low Register (GPIODALTFNLOW)

This Register selects the function of the GPIOD LSB 16-bit. Two register bits are allocated to GPIOD pin.

Address : 0xC0001026h *GPIODALTFNLO Default Value : 16'h000a*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	GPIOD7_ALTFN	GPIOD[7] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	GPIOD6_ALTFN	GPIOD[6] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	GPIOD5_ALTFN	GPIOD[5] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	GPIOD4_ALTFN	GPIOD[4] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	GPIOD3_ALTFN	GPIOD[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	GPIOD2_ALTFN	GPIOD[2] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	GPIOD1_ALTFN	GPIOD[1] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	W	GPIOD0_ALTFN	GPIOD[0] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-9. GPIOD ALTERNATE FUNCTION LOW REGISTER

GPIOD Alternate Function High Register (GPIODALTFNHI)

***** Register (GPIODALTFNHI, GPIODALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOD MSB 16-bit. Two register bits are allocated to GPIOD pin.

Address : 0xC0001046h *GPIODALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	Reserved	-	-
[13:12]	R	GPIOD13_ALTFN	GPIOD[13] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	GPIOD12_ALTFN	GPIOD[12] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R	GPIOD11_ALTFN	GPIOD[11] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	GPIOD10_ALTFN	GPIOD[10] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	GPIOD9_ALTFN	GPIOD[9] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	GPIOD8_ALTFN	GPIOD[8] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	GPIOD7_ALTFN	GPIOD[7] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-10. GPIOD ALTERNATE FUNCTION HIGH REGISTER

GPIOD Alternate Function Low Register (GPIODALTFNLOW)

This Register selects the function of the GPIOD LSB 16-bit. Two register bits are allocated to GPIOD pin.

Address : 0xC0001026h *GPIODALTFNLO Default Value : 16'h000a*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	Reserved	-	-
[13:12]	R	GPIOD6_ALTFN	GPIOD[6] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	GPIOD5_ALTFN	GPIOD[5] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R	GPIOD4_ALTFN	GPIOD[4] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	GPIOD3_ALTFN	GPIOD[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	GPIOD2_ALTFN	GPIOD[2] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	GPIOD1_ALTFN	GPIOD[1] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R	GPIOD0_ALTFN	GPIOD[0] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-11. GPIOD ALTERNATE FUNCTION LOW REGISTER

GPIOE Alternate Function High Register (GPIOEALTFNHI)

This Register selects the function of the GPIOE MSB 16-bit. Two register bits are allocated to GPIOE pin.

Address : 0xC0001048h *GPIOEALTFNHI Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOE15_ALTFN**	**GPIOE[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[13:12]	R/W	**GPIOE14_ALTFN**	**GPIOE[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[11:10]	R/W	**GPIOE13_ALTFN**	**GPIOE[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[9:8]	R/W	**GPIOE12_ALTFN**	**GPIOE[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[7:6]	R/W	**GPIOE11_ALTFN**	**GPIOE[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[5:4]	R/W	**GPIOE10_ALTFN**	**GPIOE[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[3:2]	R/W	**GPIOE9_ALTFN**	**GPIOE[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R/W	**GPIOE8_ALTFN**	**GPIOE[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-12. GPIOE ALTERNATE FUNCTION HIGH REGISTER

GPIOE Alternate Function Low Register (GPIOEALTFNLOW)

This Register selects the function of the GPIOE LSB 16-bit. Two register bits are allocated to GPIOE pin.

Address : 0xC0001028h *GPIOEALTFNLO Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOE7_ALTFN**	**GPIOE[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[13:12]	R/W	**GPIOE6_ALTFN**	**GPIOE[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[11:10]	R/W	**GPIOE5_ALTFN**	**GPIOE[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[9:8]	R/W	**GPIOE4_ALTFN**	**GPIOE[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[7:6]	R/W	**GPIOE3_ALTFN**	**GPIOE[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[5:4]	R/W	**GPIOE2_ALTFN**	**GPIOE[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[3:2]	R/W	**GPIOE1_ALTFN**	**GPIOE[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R/W	**GPIOE0_ALTFN**	**GPIOE[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-13. GPIOE ALTERNATE FUNCTION LOW REGISTER

GPIOF Alternate Function High Register (GPIOFALTFNHI)

***** Register (GPIOFALTFNHI, GPIOFALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOF MSB 16-bit. Two register bits are allocated to GPIOF pin.

Address : 0xC000104Ah *if SRAM Boot 4'ha else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	W	**GPIOF9_ALTFN**	**GPIOF[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOF8_ALTFN**	**GPIOF[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-14. GPIOF ALTERNATE FUNCTION HIGH REGISTER

GPIOF Alternate Function Low Register (GPIOFALTFNLOW)

This Register selects the function of the GPIOF LSB 16-bit. Two register bits are allocated to GPIOF pin.

Address : 0xC000102Ah *if SRAM Boot 16'haaaa else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOF7_ALTFN**	**GPIOF[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOF6_ALTFN**	**GPIOF[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOF5_ALTFN**	**GPIOF[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOF4_ALTFN**	**GPIOF[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOF3_ALTFN**	**GPIOF[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOF2_ALTFN**	**GPIOF[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOF1_ALTFN**	**GPIOF[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOF0_ALTFN**	**GPIOF[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-15. GPIOF ALTERNATE FUNCTION LOW REGISTER

GPIOF Alternate Function High Register (GPIOFALTFNHI)

***** Register (GPIOFALTFNHI, GPIOFALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOF MSB 16-bit. Two register bits are allocated to GPIOF pin.

Address : 0xC000104Ah *if SRAM Boot 4'ha else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOF9_ALTFN**	**GPIOF[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOF8_ALTFN**	**GPIOF[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOF7_ALTFN**	**GPIOF[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOF6_ALTFN**	**GPIOF[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOF5_ALTFN**	**GPIOF[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-16. GPIOF ALTERNATE FUNCTION HIGH REGISTER

GPIOF Alternate Function Low Register (GPIOFALTFNLOW)

This Register selects the function of the GPIOF LSB 16-bit. Two register bits are allocated to GPIOF pin.

Address : 0xC000102Ah *if SRAM Boot 16'haaaa else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOF4_ALTFN**	**GPIOF[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOF3_ALTFN**	**GPIOF[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOF2_ALTFN**	**GPIOF[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOF1_ALTFN**	**GPIOF[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOF0_ALTFN**	**GPIOF[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-17. GPIOF ALTERNATE FUNCTION LOW REGISTER

GPIOG Alternate Function High Register (GPIOGALTFNHI)

This Register selects the function of the GPIOG MSB 16-bit. Two register bits are allocated to GPIOG pin.

Address : 0xC000104Ch *if SRAM Boot 16'haaaa else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOG15_ALTFN**	**GPIOG[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOG14_ALTFN**	**GPIOG[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOG13_ALTFN**	**GPIOG[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOG12_ALTFN**	**GPIOG[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOG11_ALTFN**	**GPIOG[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOG10_ALTFN**	**GPIOG[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOG9_ALTFN**	**GPIOG[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOG8_ALTFN**	**GPIOG[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-18. GPIOG ALTERNATE FUNCTION HIGH REGISTER

GPIOG Alternate Function Low Register (GPIOGALTFNLOW)

This Register selects the function of the GPIOG LSB 16-bit. Two register bits are allocated to GPIOG pin.

Address : 0xC000102Ch *if SRAM Boot 16'haaaa else 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOG7_ALTFN**	**GPIOG[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOG6_ALTFN**	**GPIOG[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOG5_ALTFN**	**GPIOG[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOG4_ALTFN**	**GPIOG[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOG3_ALTFN**	**GPIOG[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOG2_ALTFN**	**GPIOG[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOG1_ALTFN**	**GPIOG[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOG0_ALTFN**	**GPIOG[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-19. GPIOG ALTERNATE FUNCTION LOW REGISTER

GPIOH Alternate Function High Register (GPIOHALTFNHI)

***** Register (GPIOHALTFNHI, GPIOHALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOH MSB 16-bit. Two register bits are allocated to GPIOH pin.

Address : 0xC000104Eh *GPIOHALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-20. GPIOH ALTERNATE FUNCTION HIGH REGISTER

GPIOH Alternate Function Low Register (GPIOHALTFNLOW)

This Register selects the function of the GPIOH LSB 16-bit. Two register bits are allocated to GPIOH pin.

Address : 0xC000102Eh *GPIOHALTFNLO Default Value : 14'h0002*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	W	GPIOH6_ALTFN	GPIOH[6] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	GPIOH5_ALTFN	GPIOH[5] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	GPIOH4_ALTFN	GPIOH[4] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	GPIOH3_ALTFN	GPIOH[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	GPIOH2_ALTFN	GPIOH[2] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	GPIOH1_ALTFN	GPIOH[1] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	GPIOH0_ALTFN	GPIOH[0] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-21. GPIOH ALTERNATE FUNCTION LOW REGISTER

GPIOH Alternate Function High Register (GPIOHALTFNHI)

***** Register (GPIOHALTFNHI, GPIOHALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOH MSB 16-bit. Two register bits are allocated to GPIOH pin.

Address : 0xC000104Eh *GPIOHALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[19:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6:5]	R	GPIOH6_ALTFN	GPIOH[6] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	GPIOH5_ALTFN	GPIOH[5] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	GPIOH4_ALTFN	GPIOH[4] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	GPIOH3_ALTFN	GPIOH[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0

TABLE 11-22. GPIOH ALTERNATE FUNCTION HIGH REGISTER

GPIOH Alternate Function Low Register (GPIOHALTFNLOW)

This Register selects the function of the GPIOH LSB 16-bit. Two register bits are allocated to GPIOH pin.

Address : 0xC000102Eh *GPIOHALTFNLO Default Value : 14'h0002*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6]	R	GPIOH3_ALTFN	GPIOH[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[5:4]	R	GPIOH2_ALTFN	GPIOH[2] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	GPIOH1_ALTFN	GPIOH[1] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	GPIOH0_ALTFN	GPIOH[0] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

TABLE 11-23. GPIOH ALTERNATE FUNCTION LOW REGISTER

GPIOI Alternate Function High Register (GPIOIALTFNHI)

This Register selects the function of the GPIOI MSB 16-bit. Two register bits are allocated to GPIOI pin.

Address : 0xC0001050h *GPIOIALTFNHI Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOI15_ALTFN**	**GPIOI[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOI14_ALTFN**	**GPIOI[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOI13_ALTFN**	**GPIOI[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOI12_ALTFN**	**GPIOI[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOI11_ALTFN**	**GPIOI[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOI10_ALTFN**	**GPIOI[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOI9_ALTFN**	**GPIOI[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOI8_ALTFN**	**GPIOI[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-24. GPIOI ALTERNATE FUNCTION HIGH REGISTER

GPIOI Alternate Function Low Register (GPIOIALTFNLOW)

This Register selects the function of the GPIOI LSB 16-bit. Two register bits are allocated to GPIOI pin.

Address : 0xC0001030h *GPIOIALTFNLO Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOI7_ALTFN**	**GPIOI[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOI6_ALTFN**	**GPIOI[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOI5_ALTFN**	**GPIOI[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOI4_ALTFN**	**GPIOI[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOI3_ALTFN**	**GPIOI[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOI2_ALTFN**	**GPIOI[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOI1_ALTFN**	**GPIOI[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOI0_ALTFN**	**GPIOI[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-25. GPIOI ALTERNATE FUNCTION LOW REGISTER

GPIOJ Alternate Function High Register (GPIOJALTFNHI)

This Register selects the function of the GPIOJ MSB 16-bit. Two register bits are allocated to GPIOJ pin.

Address : 0xC0001052h *GPIOJALTFNHI Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOJ15_ALTFN**	**GPIOJ[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOJ14_ALTFN**	**GPIOJ[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOJ13_ALTFN**	**GPIOJ[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOJ12_ALTFN**	**GPIOJ[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOJ11_ALTFN**	**GPIOJ[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOJ10_ALTFN**	**GPIOJ[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOJ9_ALTFN**	**GPIOJ[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOJ8_ALTFN**	**GPIOJ[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-26. GPIOJ ALTERNATE FUNCTION HIGH REGISTER

GPIOJ Alternate Function Low Register (GPIOJALTFNLOW)

This Register selects the function of the GPIOJ LSB 16-bit. Two register bits are allocated to GPIOJ pin.

Address : 0xC0001032h *GPIOJALTFNLO Default Value : 16'haaaa*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOJ7_ALTFN**	**GPIOJ[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOJ6_ALTFN**	**GPIOJ[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOJ5_ALTFN**	**GPIOJ[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOJ4_ALTFN**	**GPIOJ[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOJ3_ALTFN**	**GPIOJ[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOJ2_ALTFN**	**GPIOJ[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOJ1_ALTFN**	**GPIOJ[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOJ0_ALTFN**	**GPIOJ[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-27. GPIOJ ALTERNATE FUNCTION LOW REGISTER

GPIOK Alternate Function High Register (GPIOKALTFNHI)

***** Register (GPIOKALTFNHI, GPIOKALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOK MSB 16-bit. Two register bits are allocated to GPIOK pin.

Address : 0xC0001054h *GPIOKALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-28. GPIOK ALTERNATE FUNCTION HIGH REGISTER

GPIOK Alternate Function Low Register (GPIOKALTFNLOW)

This Register selects the function of the GPIOK LSB 16-bit. Two register bits are allocated to GPIOK pin.

Address : 0xC0001034h *GPIOKALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOK7_ALTFN**	**GPIOK[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOK6_ALTFN**	**GPIOK[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOK5_ALTFN**	**GPIOK[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOK4_ALTFN**	**GPIOK[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOK3_ALTFN**	**GPIOK[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOK2_ALTFN**	**GPIOK[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOK1_ALTFN**	**GPIOK[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOK0_ALTFN**	**GPIOK[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-29. GPIOK ALTERNATE FUNCTION LOW REGISTER

GPIOK Alternate Function High Register (GPIOKALTFNHI)

***** Register (GPIOHALTFNHI, GPIOHALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOK MSB 16-bit. Two register bits are allocated to GPIOK pin.

Address : 0xC0001054h *GPIOKALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOK7_ALTFN**	**GPIOK[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOK6_ALTFN**	**GPIOK[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOK5_ALTFN**	**GPIOK[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOK4_ALTFN**	**GPIOK[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-30. GPIOK ALTERNATE FUNCTION HIGH REGISTER

GPIOK Alternate Function Low Register (GPIOKALTFNLOW)

This Register selects the function of the GPIOK LSB 16-bit. Two register bits are allocated to GPIOK pin.

Address : 0xC0001034h *GPIOKALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOK3_ALTFN**	**GPIOK[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOK2_ALTFN**	**GPIOK[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOK1_ALTFN**	**GPIOK[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOK0_ALTFN**	**GPIOK[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-31. GPIOK ALTERNATE FUNCTION LOW REGISTER

GPIOL Alternate Function High Register (GPIOLALTFNHI)

***** Register (GPIOLALTFNHI, GPIOLALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOL MSB 16-bit. Two register bits are allocated to GPIOL pin.

Address : 0xC0001056h *GPIOLALTFNHI Default Value : 14'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOL14_ALTFN**	**GPIOL[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOL13_ALTFN**	**GPIOL[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOL12_ALTFN**	**GPIOL[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOL11_ALTFN**	**GPIOL[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOL10_ALTFN**	**GPIOL[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOL9_ALTFN**	**GPIOL[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOL8_ALTFN**	**GPIOL[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-32. GPIOL ALTERNATE FUNCTION HIGH REGISTER

GPIOL Alternate Function Low Register (GPIOLALTFNLOW)

This Register selects the function of the GPIOL LSB 16-bit. Two register bits are allocated to GPIOL pin.

Address : 0xC0001036h *GPIOLALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOL7_ALTFN**	**GPIOL[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOL6_ALTFN**	**GPIOL[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOL5_ALTFN**	**GPIOL[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOL4_ALTFN**	**GPIOL[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOL3_ALTFN**	**GPIOL[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOL2_ALTFN**	**GPIOL[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOL1_ALTFN**	**GPIOL[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOL0_ALTFN**	**GPIOL[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-33. GPIOL ALTERNATE FUNCTION LOW REGISTER

GPIOL Alternate Function High Register (GPIOLALTFNHI)

***** Register (GPIOLALTFNHI, GPIOLALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOL MSB 16-bit. Two register bits are allocated to GPIOL pin.

Address : 0xC0001056h *GPIOLALTFNHI Default Value : 14'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15]	-	-	Reserved	-
[14:13]	R	GPIOL14_ALTFN	GPIOL[14] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[12:11]	R	GPIOL13_ALTFN	GPIOL[13] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[10:9]	R	GPIOL12_ALTFN	GPIOL[12] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[8:7]	R	GPIOL11_ALTFN	GPIOL[11] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[6:5]	R	GPIOL10_ALTFN	GPIOL[10] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	GPIOL9_ALTFN	GPIOL[9] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	GPIOL8_ALTFN	GPIOL[8] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	GPIOL7_ALTFN	GPIOL[7] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0

TABLE 11-34. GPIOL ALTERNATE FUNCTION HIGH REGISTER

GPIOL Alternate Function Low Register (GPIOLALTFNLOW)

This Register selects the function of the GPIOL LSB 16-bit. Two register bits are allocated to GPIOL pin.

Address : 0xC0001036h *GPIOLALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15]	-	-	Reserved	-
[14]	R	GPIOL7_ALTFN	GPIOL[7] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[13:12]	R	GPIOL6_ALTFN	GPIOL[6] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	GPIOL5_ALTFN	GPIOL[5] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R	GPIOL4_ALTFN	GPIOL[4] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	GPIOL3_ALTFN	GPIOL[3] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	GPIOL2_ALTFN	GPIOL[2] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	GPIOL1_ALTFN	GPIOL[1] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	GPIOL0_ALTFN	GPIOL[0] 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-35. GPIOL ALTERNATE FUNCTION LOW REGISTER

GPIOM Alternate Function High Register (GPIOMALTFNHI)

***** Register (GPIOMALTFNHI, GPIOMALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOM MSB 16-bit. Two register bits are allocated to GPIOM pin.

Address : 0xC0001058h *GPIOMALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	W	**GPIOM8_ALTFN**	**GPIOM[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-36. GPIOM ALTERNATE FUNCTION HIGH REGISTER

GPIOM Alternate Function Low Register (GPIOMALTFNLOW)

This Register selects the function of the GPIOM LSB 16-bit. Two register bits are allocated to GPIOM pin.

Address : 0xC0001038h *GPIOMALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOM7_ALTFN**	**GPIOM[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOM6_ALTFN**	**GPIOM[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOM5_ALTFN**	**GPIOM[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOM3_ALTFN**	**GPIOM[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOM2_ALTFN**	**GPIOM[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOM1_ALTFN**	**GPIOM[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOM0_ALTFN**	**GPIOM[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-37. GPIOM ALTERNATE FUNCTION LOW REGISTER

GPIOM Alternate Function High Register (GPIOMALTFNHI)

***** Register (GPIOMALTFNHI, GPIOMALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOM MSB 16-bit. Two register bits are allocated to GPIOM pin.

Address : 0xC0001058h *GPIOMALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	R	**GPIOM8_ALTFN**	**GPIOM[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[6:5]	R	**GPIOM7_ALTFN**	**GPIOM[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	**GPIOM6_ALTFN**	**GPIOM[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	**GPIOM5_ALTFN**	**GPIOM[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0

TABLE 11-38. GPIOM ALTERNATE FUNCTION HIGH REGISTER

GPIOM Alternate Function Low Register (GPIOMALTFNLOW)

This Register selects the function of the GPIOM LSB 16-bit. Two register bits are allocated to GPIOM pin.

Address : 0xC0001038h *GPIOMALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8]	R	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[7:6]	R	**GPIOM3_ALTFN**	**GPIOM[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOM2_ALTFN**	**GPIOM[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOM1_ALTFN**	**GPIOM[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOM0_ALTFN**	**GPIOM[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-39. GPIOM ALTERNATE FUNCTION LOW REGISTER

GPION Alternate Function High Register (GPIONALTFNHI)

***** Register (GPIONALTFNHI, GPIONALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPION MSB 16-bit. Two register bits are allocated to GPION pin.

Address : 0xC000105Ah *GPIONALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-40. GPION ALTERNATE FUNCTION HIGH REGISTER

GPION Alternate Function Low Register (GPIONALTFNLOW)

This Register selects the function of the GPION LSB 16-bit. Two register bits are allocated to GPION pin.

Address : 0xC000103Ah *GPIONALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPION7_ALTFN**	**GPION[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPION6_ALTFN**	**GPION[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPION5_ALTFN**	**GPION[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPION4_ALTFN**	**GPION[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPION3_ALTFN**	**GPION[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPION2_ALTFN**	**GPION[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPION1_ALTFN**	**GPION[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPION0_ALTFN**	**GPION[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-41. GPION ALTERNATE FUNCTION LOW REGISTER

GPION Alternate Function High Register (GPIONALTFNHI)

***** Register (GPIONALTFNHI, GPIONALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPION MSB 16-bit. Two register bits are allocated to GPION pin.

Address : 0xC000105Ah *GPIONALTFNHI Default Value : reserved*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPION7_ALTFN**	**GPION[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPION6_ALTFN**	**GPION[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPION5_ALTFN**	**GPION[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPION4_ALTFN**	**GPION[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-42. GPION ALTERNATE FUNCTION HIGH REGISTER

GPION Alternate Function Low Register (GPIONALTFNLOW)

This Register selects the function of the GPION LSB 16-bit. Two register bits are allocated to GPION pin.

Address : 0xC000103Ah *GPIONALTFNLO Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPION3_ALTFN**	**GPION[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPION2_ALTFN**	**GPION[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPION1_ALTFN**	**GPION[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPION0_ALTFN**	**GPION[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-43. GPION ALTERNATE FUNCTION LOW REGISTER

GPIOO Alternate Function High Register (GPIOOALTFNHI)

***** Register (GPIOOALTFNHI, GPIOOALTFNLOW) has a different value when Write. *****

This Register selects the function of the GPIOO MSB 16-bit. Two register bits are allocated to GPIOO pin.

Address : 0xC000105Ch *GPIOOALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-44. GPIOO ALTERNATE FUNCTION HIGH REGISTER

GPIOO Alternate Function Low Register (GPIOOALTFNLOW)

This Register selects the function of the GPIOO LSB 16-bit. Two register bits are allocated to GPIOO pin.

Address : 0xC000103Ch *GPIOOALTFNLO Default Value : 12'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIOO5_ALTFN**	**GPIOO[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOO4_ALTFN**	**GPIOO[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOO3_ALTFN**	**GPIOO[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOO2_ALTFN**	**GPIOO[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOO1_ALTFN**	**GPIOO[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOO0_ALTFN**	**GPIOO[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-45. GPIOO ALTERNATE FUNCTION LOW REGISTER

GPIOO Alternate Function High Register (GPIOOALTFNHI)

***** Register (GPIOOALTFNHI, GPIOOALTFNLOW) has a different value when Read. *****

This Register selects the function of the GPIOO MSB 16-bit. Two register bits are allocated to GPIOO pin.

Address : 0xC000105Ch *GPIOOALTFNHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOO5_ALTFN**	**GPIOO[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOO4_ALTFN**	**GPIOO[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOO3_ALTFN**	**GPIOO[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-46. GPIOO ALTERNATE FUNCTION HIGH REGISTER

GPIOO Alternate Function Low Register (GPIOOALTFNLOW)

This Register selects the function of the GPIOO LSB 16-bit. Two register bits are allocated to GPIOO pin.

Address : 0xC000103Ch *GPIOOALTFNLO Default Value : 12 'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOO2_ALTFN**	**GPIOO[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOO1_ALTFN**	**GPIOO[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOO0_ALTFN**	**GPIOO[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

TABLE 11-47. GPIOO ALTERNATE FUNCTION LOW REGISTER

GPIOx Output Level Register (GPIOxOUT)

This Register sets the output level when a GPIO Pin is set as a GPIO Output.

GPIO	Address	GPIO	Address	GPIO	Address
GPIOA	*0xC000 1060h*	GPIOF	*0xC000 106Ah*	GPIOK	*0xC000 1074h*
GPIOB	*0xC000 1062h*	GPIOG	*0xC000 106Ch*	GPIOL	*0xC000 1076h*
GPIOC	*0xC000 1064h*	GPIOH	*0xC000 106Eh*	GPIOM	*0xC000 1078h*
GPIOD	*0xC000 1066h*	GPIOI	*0xC000 1070h*	GPION	*0xC000 107Ah*
GPIOE	*0xC000 1068h*	GPIOJ	*0xC000 1072h*	GPIOO	*0xC000 107Ch*

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**GPIOxOUT15**	GPIO[15] Output Level	0
[14]	R/W	**GPIOxOUT14**	GPIO[14] Output Level	0
[13]	R/W	**GPIOxOUT13**	GPIO[13] Output Level	0
[12]	R/W	**GPIOxOUT12**	GPIO[12] Output Level	0
[11]	R/W	**GPIOxOUT11**	GPIO[11] Output Level	0
[10]	R/W	**GPIOxOUT10**	GPIO[10] Output Level	0
[9]	R/W	**GPIOxOUT9**	GPIO[9] Output Level	0
[8]	R/W	**GPIOxOUT8**	GPIO[8] Output Level	0
[7]	R/W	**GPIOxOUT7**	GPIO[7] Output Level	0
[6]	R/W	**GPIOxOUT6**	GPIO[6] Output Level	0
[5]	R/W	**GPIOxOUT5**	GPIO[5] Output Level	0
[4]	R/W	**GPIOxOUT4**	GPIO[4] Output Level	0
[3]	R/W	**GPIOxOUT3**	GPIO[3] Output Level	0
[2]	R/W	**GPIOxOUT2**	GPIO[2] Output Level	0
[1]	R/W	**GPIOxOUT1**	GPIO[1] Output Level	0
[0]	R/W	**GPIOxOUT0**	GPIO[0] Output Level	0

TABLE 11-48. GPIOX OUTPUT LEVEL REGISTER

GPIOA Event Type High Register (GPIOAEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A0h *GPIOAEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOAEVTTYP15**	**GPIOA[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOAEVTTYP14**	**GPIOA[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOAEVTTYP13**	**GPIOA[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOAEVTTYP12**	**GPIOA[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOAEVTTYP11**	**GPIOA[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOAEVTTYP10**	**GPIOA[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOAEVTTYP9**	**GPIOA[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOAEVTTYP8**	**GPIOA[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-49. GPIOA EVENT TYPE HIGH REGISTER

GPIOA Event Type Low Register (GPIOAEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001080h *GPIOAEVTTYP HI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOAEVTTYP7**	**GPIOA[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOAEVTTYP6**	**GPIOA[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOAEVTTYP5**	**GPIOA[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOAEVTTYP4**	**GPIOA[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOAEVTTYP3**	**GPIOA[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOAEVTTYP2**	**GPIOA[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOAEVTTYP1**	**GPIOA[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOAEVTTYP0**	**GPIOA[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-50. GPIOA EVENT TYPE LOW REGISTER

GPIOB Event Type High Register (GPIOBEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A2h *GPIOBEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOBEVTTYP15**	**GPIOB[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOBEVTTYP14**	**GPIOB[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOBEVTTYP13**	**GPIOB[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOBEVTTYP12**	**GPIOB[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOBEVTTYP11**	**GPIOB[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOBEVTTYP10**	**GPIOB[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOBEVTTYP9**	**GPIOB[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOBEVTTYP8**	**GPIOB[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-51. GPIOB EVENT TYPE HIGH REGISTER

GPIOB Event Type Low Register (GPIOBEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001082h *GPIOBEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOBEVTTYP7**	**GPIOB[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOBEVTTYP6**	**GPIOB[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOBEVTTYP5**	**GPIOB[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOBEVTTYP4**	**GPIOB[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOBEVTTYP3**	**GPIOB[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOBEVTTYP2**	**GPIOB[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOBEVTTYP1**	**GPIOB[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOBEVTTYP0**	**GPIOB[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-52. GPIOB EVENT TYPE LOW REGISTER

GPIOC Event Type High Register (GPIOCEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A4h *GPIOCEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOCEVTTYP15**	**GPIOC[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOCEVTTYP14**	**GPIOC[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOCEVTTYP13**	**GPIOC[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOCEVTTYP12**	**GPIOC[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOCEVTTYP11**	**GPIOC[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOCEVTTYP10**	**GPIOC[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOCEVTTYP9**	**GPIOC[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOCEVTTYP8**	**GPIOC[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-53. GPIOC EVENT TYPE HIGH REGISTER

GPIOC Event Type Low Register (GPIOCEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001084h *GPIOCEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOCEVTTYP7**	**GPIOC[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOCEVTTYP6**	**GPIOC[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOCEVTTYP5**	**GPIOC[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOCEVTTYP4**	**GPIOC[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOCEVTTYP3**	**GPIOC[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOCEVTTYP2**	**GPIOC[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOCEVTTYP1**	**GPIOC[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOCEVTTYP0**	**GPIOC[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-54. GPIOC EVENT TYPE LOW REGISTER

GPIOD Event Type High Register (GPIODEVTTYPHI)

***** Register (GPIODEVTTYPHI, GPIODEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A6h *GPIODEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIODEVTTYP13**	**GPIOD[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIODEVTTYP12**	**GPIOD[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIODEVTTYP11**	**GPIOD[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIODEVTTYP10**	**GPIOD[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIODEVTTYP9**	**GPIOD[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIODEVTTYP8**	**GPIOD[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-55. GPIOD EVENT TYPE HIGH REGISTER

GPIOD Event Type Low Register (GPIODEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001086h *GPIODEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIODEVTTYP7**	**GPIOD[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIODEVTTYP6**	**GPIOD[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIODEVTTYP5**	**GPIOD[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIODEVTTYP4**	**GPIOD[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIODEVTTYP3**	**GPIOD[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIODEVTTYP2**	**GPIOD[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIODEVTTYP1**	**GPIOD[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIODEVTTYP0**	**GPIOD[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-56. GPIOD EVENT TYPE LOW REGISTER

GPIOD Event Type High Register (GPIODEVTTYPHI)

***** Register (GPIODEVTTYPHI, GPIODEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A6h *GPIODEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	R	**GPIODEVTTYP13**	**GPIOD[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00-
[11:10]	R	**GPIODEVTTYP12**	**GPIOD[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIODEVTTYP11**	**GPIOD[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIODEVTTYP10**	**GPIOD[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIODEVTTYP9**	**GPIOD[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIODEVTTYP8**	**GPIOD[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIODEVTTYP7**	**GPIOD[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-57. GPIOD EVENT TYPE HIGH REGISTER

GPIOD Event Type Low Register (GPIODEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001086h *GPIODEVTTYP HI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	R	**GPIODEVTTYP6**	**GPIOD[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R	**GPIODEVTTYP5**	**GPIOD[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIODEVTTYP4**	**GPIOD[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIODEVTTYP3**	**GPIOD[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIODEVTTYP2**	**GPIOD[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIODEVTTYP1**	**GPIOD[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIODEVTTYP0**	**GPIOD[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-58. GPIOD EVENT TYPE LOW REGISTER

GPIOE Event Type High Register (GPIOEEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010A8h *GPIOEEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOEEVTTYP15**	**GPIOE[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOEEVTTYP14**	**GPIOE[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOEEVTTYP13**	**GPIOE[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOEEVTTYP12**	**GPIOE[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOEEVTTYP11**	**GPIOE[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOEEVTTYP10**	**GPIOE[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOEEVTTYP9**	**GPIOE[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOEEVTTYP8**	**GPIOE[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-59. GPIOE EVENT TYPE HIGH REGISTER

GPIOE Event Type Low Register (GPIOEEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001088h *GPIOEEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOEEVTTYP7**	**GPIOE[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOEEVTTYP6**	**GPIOE[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOEEVTTYP5**	**GPIOE[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOEEVTTYP4**	**GPIOE[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOEEVTTYP3**	**GPIOE[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOEEVTTYP2**	**GPIOE[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOEEVTTYP1**	**GPIOE[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOEEVTTYP0**	**GPIOE[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-60. GPIOE EVENT TYPE LOW REGISTER

GPIOF Event Type High Register (GPIOFEVTTYPHI)

***** Register (GPIOFEVTTYPHI, GPIOFEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010AAh *GPIOFEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	W	**GPIOFEVTTYP9**	**GPIOF[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOFEVTTYP8**	**GPIOF[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-61. GPIOF EVENT TYPE HIGH REGISTER

GPIOF Event Type Low Register (GPIOFEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000108Ah *GPIOFEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOFEVTTYP7**	**GPIOF[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOFEVTTYP6**	**GPIOF[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOFEVTTYP5**	**GPIOF[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOFEVTTYP4**	**GPIOF[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOFEVTTYP3**	**GPIOF[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOFEVTTYP2**	**GPIOF[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOFEVTTYP1**	**GPIOF[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOFEVTTYP0**	**GPIOF[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-62. GPIOF EVENT TYPE LOW REGISTER

GPIOF Event Type High Register (GPIOFEVTTYPHI)

***** Register (GPIOFEVTTYPHI, GPIOFEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010AAh *GPIOFEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOFEVTTYP9**	**GPIOF[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIOFEVTTYP8**	**GPIOF[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOFEVTTYP7**	**GPIOF[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOFEVTTYP6**	**GPIOF[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOFEVTTYP5**	**GPIOF[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-63. GPIOF EVENT TYPE HIGH REGISTER

GPIOF Event Type Low Register (GPIOFEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000108Ah *GPIOFEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOFEVTTYP4**	**GPIOF[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIOFEVTTYP3**	**GPIOF[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOFEVTTYP2**	**GPIOF[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOFEVTTYP1**	**GPIOF[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOFEVTTYP0**	**GPIOF[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-64. GPIOF EVENT TYPE LOW REGISTER

GPIOG Event Type High Register (GPIOGEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010ACh *GPIOGEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOGEVTTYP15**	**GPIOG[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOGEVTTYP14**	**GPIOG[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOGEVTTYP13**	**GPIOG[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOGEVTTYP12**	**GPIOG[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOGEVTTYP11**	**GPIOG[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOGEVTTYP10**	**GPIOG[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOGEVTTYP9**	**GPIOG[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOGEVTTYP8**	**GPIOG[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-65. GPIOG EVENT TYPE HIGH REGISTER

GPIOG Event Type Low Register (GPIOGEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000108Ch *GPIOGEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOGEVTTYP7**	**GPIOG[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOGEVTTYP6**	**GPIOG[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOGEVTTYP5**	**GPIOG[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOGEVTTYP4**	**GPIOG[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOGEVTTYP3**	**GPIOG[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOGEVTTYP2**	**GPIOG[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOGEVTTYP1**	**GPIOG[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOGEVTTYP0**	**GPIOG[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-66. GPIOG EVENT TYPE LOW REGISTER

GPIOH Event Type High Register (GPIOHEVTTYPHI)

***** Register (GPIOHEVTTYPHI, GPIOHEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010AEh *GPIOHEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-67. GPIOH EVENT TYPE HIGH REGISTER

GPIOH Event Type Low Register (GPIOHEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000108Eh *GPIOHEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOHEVTTYP6**	**GPIOH[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOHEVTTYP5**	**GPIOH[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOHEVTTYP4**	**GPIOH[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOHEVTTYP2**	**GPIOH[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOHEVTTYP1**	**GPIOH[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOHEVTTYP0**	**GPIOH[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-68. GPIOH EVENT TYPE LOW REGISTER

GPIOH Event Type High Register (GPIOHEVTTYPHI)

***** Register (GPIOHEVTTYPHI, GPIOHEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010AEh *GPIOHEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6:5]	R	**GPIOHEVTTYP6**	**GPIOH[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOHEVTTYP5**	**GPIOH[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOHEVTTYP4**	**GPIOH[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[0]	R	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0

TABLE 11-69. GPIOH EVENT TYPE HIGH REGISTER

GPIOH Event Type Low Register (GPIOHEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000108Eh *GPIOHEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6]	R	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[5:4]	R	**GPIOHEVTTYP2**	**GPIOH[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOHEVTTYP1**	**GPIOH[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOHEVTTYP0**	**GPIOH[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-70. GPIOH EVENT TYPE LOW REGISTER

GPIOI Event Type High Register (GPIOIEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B0h *GPIOIEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOIEVTTYP15**	**GPIOI[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOIEVTTYP14**	**GPIOI[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOIEVTTYP13**	**GPIOI[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOIEVTTYP12**	**GPIOI[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOIEVTTYP11**	**GPIOI[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOIEVTTYP10**	**GPIOI[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOIEVTTYP9**	**GPIOI[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOIEVTTYP8**	**GPIOI[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-71. GPIOI EVENT TYPE HIGH REGISTER

GPIOI Event Type Low Register (GPIOIEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001090h *GPIOIEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOIEVTTYP7**	**GPIOI[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOIEVTTYP6**	**GPIOI[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOIEVTTYP5**	**GPIOI[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOIEVTTYP4**	**GPIOI[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOIEVTTYP3**	**GPIOI[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOIEVTTYP2**	**GPIOI[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOIEVTTYP1**	**GPIOI[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOIEVTTYP0**	**GPIOI[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-72. GPIOI EVENT TYPE LOW REGISTER

GPIOJ Event Type High Register (GPIOJEVTTYPHI)

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B2h *GPIOJEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOJEVTTYP15**	**GPIOJ[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOJEVTTYP14**	**GPIOJ[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOJEVTTYP13**	**GPIOJ[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOJEVTTYP12**	**GPIOJ[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOJEVTTYP11**	**GPIOJ[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOJEVTTYP10**	**GPIOJ[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOJEVTTYP9**	**GPIOJ[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOJEVTTYP8**	**GPIOJ[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-73. GPIOJ EVENT TYPE HIGH REGISTER

GPIOJ Event Type Low Register (GPIOJEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001092h *GPIOJEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOJEVTTYP7**	**GPIOJ[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOJEVTTYP6**	**GPIOJ[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOJEVTTYP5**	**GPIOJ[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOJEVTTYP4**	**GPIOJ[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOJEVTTYP3**	**GPIOJ[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOJEVTTYP2**	**GPIOJ[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOJEVTTYP1**	**GPIOJ[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOJEVTTYP0**	**GPIOJ[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-74. GPIOJ EVENT TYPE LOW REGISTER

GPIOK Event Type High Register (GPIOKEVTTYPHI)

***** Register (GPIOKEVTTYPHI, GPIOKEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B4h *GPIOKEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-75. GPIOK EVENT TYPE HIGH REGISTER

GPIOK Event Type Low Register (GPIOKEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001094h *GPIOKEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOKEVTTYP7**	**GPIOK[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOKEVTTYP6**	**GPIOK[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOKEVTTYP5**	**GPIOK[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOKEVTTYP4**	**GPIOK[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOKEVTTYP3**	**GPIOK[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOKEVTTYP2**	**GPIOK[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOKEVTTYP1**	**GPIOK[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOKEVTTYP0**	**GPIOK[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-76. GPIOK EVENT TYPE LOW REGISTER

GPIOK Event Type High Register (GPIOKEVTTYPHI)

***** Register (GPIOKEVTTYPHI, GPIOKEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B4h *GPIOKEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOKEVTTYP7**	**GPIOK[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOKEVTTYP6**	**GPIOK[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOKEVTTYP5**	**GPIOK[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOKEVTTYP4**	**GPIOK[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-77. GPIOK EVENT TYPE HIGH REGISTER

GPIOK Event Type Low Register (GPIOKEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001094h *GPIOKEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOKEVTTYP3**	**GPIOK[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOKEVTTYP2**	**GPIOK[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOKEVTTYP1**	**GPIOK[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOKEVTTYP0**	**GPIOK[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-78. GPIOK EVENT TYPE LOW REGISTER

GPIOL Event Type High Register (GPIOLEVTTYPHI)

***** Register (GPIOLEVTTYPHI, GPIOLEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B6h *GPIOLEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOLEVTTYP14**	**GPIOL[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOLEVTTYP13**	**GPIOL[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOLEVTTYP12**	**GPIOL[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOLEVTTYP11**	**GPIOL[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOLEVTTYP10**	**GPIOL[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOLEVTTYP9**	**GPIOL[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOLEVTTYP8**	**GPIOL[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-79. GPIOL EVENT TYPE HIGH REGISTER

GPIOL Event Type Low Register (GPIOLEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001096h *GPIOLEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOLEVTTYP6**	**GPIOL[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOLEVTTYP5**	**GPIOL[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOLEVTTYP4**	**GPIOL[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOLEVTTYP3**	**GPIOL[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOLEVTTYP2**	**GPIOL[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOLEVTTYP1**	**GPIOL[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOLEVTTYP0**	**GPIOL[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-80. GPIOL EVENT TYPE LOW REGISTER

GPIOL Event Type High Register (GPIOLEVTTYPHI)

***** Register (GPIOLEVTTYPHI, GPIOLEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B6h *GPIOLEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15]	-	-	Reserved	-
[14:13]	R	**GPIOLEVTTYP14**	**GPIOL[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[12:11]	R	**GPIOLEVTTYP13**	**GPIOL[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[10:9]	R	**GPIOLEVTTYP12**	**GPIOL[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[8:7]	R	**GPIOLEVTTYP11**	**GPIOL[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[6:5]	R	**GPIOLEVTTYP10**	**GPIOL[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOLEVTTYP9**	**GPIOL[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOLEVTTYP8**	**GPIOL[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[0]	R	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0

TABLE 11-81. GPIOL EVENT TYPE HIGH REGISTER

GPIOL Event Type Low Register (GPIOLEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001096h *GPIOLEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15]	-	-	Reserved	-
[14]	R	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[13:12]	R	**GPIOLEVTTYP6**	**GPIOL[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R	**GPIOLEVTTYP5**	**GPIOL[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIOLEVTTYP4**	**GPIOL[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIOLEVTTYP3**	**GPIOL[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOLEVTTYP2**	**GPIOL[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOLEVTTYP1**	**GPIOL[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOLEVTTYP0**	**GPIOL[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-82. GPIOL EVENT TYPE LOW REGISTER

GPIOM Event Type High Register (GPIOMEVTTYPHI)

***** Register (GPIOMEVTTYPHI, GPIOMEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B8h *GPIOMEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	W	**GPIOMEVTTYP8**	**GPIOM[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-83. GPIOM EVENT TYPE HIGH REGISTER

GPIOM Event Type Low Register (GPIOMEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001098h *GPIOMEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOMEVTTYP7**	**GPIOM[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOMEVTTYP6**	**GPIOM[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOMEVTTYP5**	**GPIOM[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOMEVTTYP3**	**GPIOM[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOMEVTTYP2**	**GPIOM[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOMEVTTYP1**	**GPIOM[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOMEVTTYP0**	**GPIOM[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-84. GPIOM EVENT TYPE LOW REGISTER

GPIOM Event Type High Register (GPIOMEVTTYPHI)

***** Register (GPIOMEVTTYPHI, GPIOMEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010B8h *GPIOMEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	R	**GPIOMEVTTYP8**	**GPIOM[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[6:5]	R	**GPIOMEVTTYP7**	**GPIOM[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOMEVTTYP6**	**GPIOM[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOMEVTTYP5**	**GPIOM[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[0]	R	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0

TABLE 11-85. GPIOM EVENT TYPE HIGH REGISTER

GPIOM Event Type Low Register (GPIOMEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC0001098h *GPIOMEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8]	R	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[7:6]	R	**GPIOMEVTTYP3**	**GPIOM[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOMEVTTYP2**	**GPIOM[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOMEVTTYP1**	**GPIOM[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOMEVTTYP0**	**GPIOM[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-86. GPIOM EVENT TYPE LOW REGISTER

GPION Event Type High Register (GPIONEVTTYPHI)

***** Register (GPIONEVTTYPHI, GPIONEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010BAh *GPIONEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-87. GPION EVENT TYPE HIGH REGISTER

GPION Event Type Low Register (GPIONEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000109Ah *GPIONEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIONEVTTYP7**	**GPION[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIONEVTTYP6**	**GPION[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIONEVTTYP5**	**GPION[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIONEVTTYP4**	**GPION[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIONEVTTYP3**	**GPION[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIONEVTTYP2**	**GPION[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIONEVTTYP1**	**GPION[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIONEVTTYP0**	**GPION[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-88. GPION EVENT TYPE LOW REGISTER

GPION Event Type High Register (GPIONEVTTYPHI)

***** Register (GPIONEVTTYPHI, GPIONEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010BAh *GPIONEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIONEVTTYP7**	**GPION[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIONEVTTYP6**	**GPION[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIONEVTTYP5**	**GPION[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIONEVTTYP4**	**GPION[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-89. GPION EVENT TYPE HIGH REGISTER

GPION Event Type Low Register (GPIONEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000109Ah *GPIONEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIONEVTTYP3**	**GPION[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIONEVTTYP2**	**GPION[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIONEVTTYP1**	**GPION[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIONEVTTYP0**	**GPION[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-90. GPION EVENT TYPE LOW REGISTER

GPIOO Event Type High Register (GPIOOEVTTYPHI)

***** Register (GPIOOEVTTYPHI, GPIOOEVTTYPLOW) has a different value when Write. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010BCh *GPIOOEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-

TABLE 11-91. GPIOO EVENT TYPE HIGH REGISTER

GPIOO Event Type Low Register (GPIOOEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000109Ch *GPIOOEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIOOEVTTYP5**	**GPIOO[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOOEVTTYP4**	**GPIOO[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOOEVTTYP3**	**GPIOO[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOOEVTTYP2**	**GPIOO[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOOEVTTYP1**	**GPIOO[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOOEVTTYP0**	**GPIOO[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-92. GPIOO EVENT TYPE LOW REGISTER

GPIOO Event Type High Register (GPIOOEVTTYPHI)

***** Register (GPIOOEVTTYPHI, GPIOOEVTTYPLOW) has a different value when Read. *****

This Register indicates the event type of the GPIO MSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC00010BCh *GPIOOEVTTYPHI Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOOEVTTYP5**	**GPIOO[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOOEVTTYP4**	**GPIOO[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOOEVTTYP3**	**GPIOO[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-93. GPIOO EVENT TYPE HIGH REGISTER

GPIOO Event Type Low Register (GPIOOEVTTYPLOW)

This Register indicates the event type of the GPIO LSB 16-bit when a GPIO Pin is set as a GPIO input.

Address : 0xC000109Ch *GPIOOEVTTYPLOW Default Value : 16'h0000*

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOOEVTTYP2**	**GPIOO[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOOEVTTYP1**	**GPIOO[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOOEVTTYP0**	**GPIOO[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

TABLE 11-94. GPIOO EVENT TYPE LOW REGISTER

GPIOX PULL UP ENABLE REGISTER (GPIOXPUENB)

This Register enables GPIO pins to pull up. When the value of a bit of the register is 1, it enables the corresponding pin to pull up.

GPIO	Address	GPIO	Address	GPIO	Address
GPIOA	*0xC000 10C0h*	GPIOF	*0xC000 10Cah*	GPIOK	*0xC000 10D4h*
GPIOB	*0xC000 10C2h*	GPIOG	*0xC000 10CCh*	GPIOL	*0xC000 10D6h*
GPIOC	*0xC000 10C4h*	GPIOH	*0xC000 10Ceh*	GPIOM	*0xC000 10D8h*
GPIOD	*0xC000 10C6h*	GPIOI	*0xC000 10D0h*	GPION	*0xC000 10DAh*
GPIOE	*0xC000 10C8h*	GPIOJ	*0xC000 10D2h*	GPIOO	*0xC000 10DCh*

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**GPIOxPUENB15**	GPIO[15] pull up enable	3)
[14]	R/W	**GPIOxPUENB14**	GPIO[14] pull up enable	3)
[13]	R/W	**GPIOxPUENB13**	GPIO[13] pull up enable	3)
[12]	R/W	**GPIOxPUENB12**	GPIO[12] pull up enable	3)
[11]	R/W	**GPIOxPUENB11**	GPIO[11] pull up enable	3)
[10]	R/W	**GPIOxPUENB10**	GPIO[10] pull up enable	3)
[9]	R/W	**GPIOxPUENB9**	GPIO[9] pull up enable	3)
[8]	R/W	**GPIOxPUENB8**	GPIO[8] pull up enable	3)
[7]	R/W	**GPIOxPUENB7**	GPIO[7] pull up enable	3)
[6]	R/W	**GPIOxPUENB6**	GPIO[6] pull up enable	3)
[5]	R/W	**GPIOxPUENB5**	GPIO[5] pull up enable	3)
[4]	R/W	**GPIOxPUENB4**	GPIO[4] pull up enable	3)
[3]	R/W	**GPIOxPUENB3**	GPIO[3] pull up enable	3)
[2]	R/W	**GPIOxPUENB2**	GPIO[2] pull up enable	3)
[1]	R/W	**GPIOxPUENB1**	GPIO[1] pull up enable	3)
[0]	R/W	**GPIOxPUENB0**	GPIO[0] pull up enable	3)

TABLE 11-95. GPIOX PULL UP ENABLE REGISTER

3) GPIOPUENB reset value

GPIOA : 16'hffff
GPIOB : 16'hffff
GPIOC : 16'hffff
GPIOD : 14'h3ffc
GPIOE : 16'h0000
GPIOF : 4'h0
GPIOG : 16'h0000
GPIOH : 7'h7e
GPIOI : 16'h0000
GPIOJ : 16'h0000
GPIOK : 8'hff
GPIOL : 15'h7fff
GPIOM : 9'h1ff
GPION : 8'hff
GPIOO : 6'h2f

GPIOx Interrupt Enable Register (GPIOxINTENB)

When a GPIO pin is set as a GPIO Input, this Register enables the pin to be an Interrupt source.
When the value of a bit of the register is 1, the register enables the corresponding GPIO pin to interrupt.

GPIO	Address	GPIO	Address	GPIO	Address
GPIOA	*0xC000 10E0h*	GPIOF	*0xC000 10EAh*	GPIOK	*0xC000 10F4h*
GPIOB	*0xC000 10E2h*	GPIOG	*0xC000 10ECh*	GPIOL	*0xC000 10F6h*
GPIOC	*0xC000 10E4h*	GPIOH	*0xC000 10EEh*	GPIOM	*0xC000 10F8h*
GPIOD	*0xC000 10E6h*	GPIOI	*0xC000 10F0h*	GPION	*0xC000 10FAh*
GPIOE	*0xC000 10E8h*	GPIOJ	*0xC000 10F2h*	GPIOO	*0xC000 10FCh*

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**GPIOxINTENB15**	GPIO[15] interrupt enable	1
[14]	R/W	**GPIOxINTENB14**	GPIO[14] interrupt enable	1
[13]	R/W	**GPIOxINTENB13**	GPIO[13] interrupt enable	1
[12]	R/W	**GPIOxINTENB12**	GPIO[12] interrupt enable	1
[11]	R/W	**GPIOxINTENB11**	GPIO[11] interrupt enable	1
[10]	R/W	**GPIOxINTENB10**	GPIO[10] interrupt enable	1

Bit	R/W	Symbol	Description	Reset Value
[9]	R/W	**GPIOxINTENB9**	GPIO[9] interrupt enable	1
[8]	R/W	**GPIOxINTENB8**	GPIO[8] interrupt enable	1
[7]	R/W	**GPIOxINTENB7**	GPIO[7] interrupt enable	1
[6]	R/W	**GPIOxINTENB6**	GPIO[6] interrupt enable	1
[5]	R/W	**GPIOxINTENB5**	GPIO[5] interrupt enable	1
[4]	R/W	**GPIOxINTENB4**	GPIO[4] interrupt enable	1
[3]	R/W	**GPIOxINTENB3**	GPIO[3] interrupt enable	1
[2]	R/W	**GPIOxINTENB2**	GPIO[2] interrupt enable	1
[1]	R/W	**GPIOxINTENB1**	GPIO[1] interrupt enable	1
[0]	R/W	**GPIOxINTENB0**	GPIO[0] interrupt enable	1

TABLE 11-96. GPIOX INTERRUPT ENABLE REGISTER

GPIOx Event Register (GPIOxEVT)

GPIO	Address	GPIO	Address	GPIO	Address
GPIOA	***0xC000 1100h***	**GPIOF**	***0xC000 110Ah***	**GPIOK**	***0xC000 1114h***
GPIOB	***0xC000 1102h***	**GPIOG**	***0xC000 110Ch***	**GPIOL**	***0xC000 1116h***
GPIOC	***0xC000 1104h***	**GPIOH**	***0xC000 110Eh***	**GPIOM**	***0xC000 1118h***
GPIOD	***0xC000 1106h***	**GPIOI**	***0xC000 1110h***	**GPION**	***0xC000 111Ah***
GPIOE	***0xC000 1108h***	**GPIOJ**	***0xC000 1112h***	**GPIOO**	***0xC000 111Ch***

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**GPIOxEVT15**	R : GPIO[15] event status, 0 : event not detected, 1 : event detected W : GPIO[15] event clear, 0 : don't care, 1 : event status register clear	0
[14]	R/W	**GPIOxEVT14**	R : GPIO[14] event status, 0 : event not detected, 1 : event detected W : GPIO[14] event clear, 0 : don't care, 1 : event status register clear	0
[13]	R/W	**GPIOxEVT13**	R : GPIO[13] event status, 0 : event not detected, 1 : event detected W : GPIO[13] event clear, 0 : don't care, 1 : event status register clear	0
[12]	R/W	**GPIOxEVT12**	R : GPIO[12] event status, 0 : event not detected, 1 : event detected W : GPIO[12] event clear, 0 : don't care, 1 : event status register clear	0
[11]	R/W	**GPIOxEVT11**	R : GPIO[11] event status, 0 : event not detected, 1 : event detected W : GPIO[11] event clear, 0 : don't care, 1 : event status register clear	0

Bit	R/W	Symbol	Description	Reset Value
[10]	R/W	**GPIOxEVT10**	R : GPIO[10] event status, 0 : event not detected, 1 : event detected W : GPIO[10] event clear, 0 : don't care, 1 : event status register clear	0
[9]	R/W	**GPIOxEVT9**	R : GPIO[9] event status, 0 : event not detected, 1 : event detected W : GPIO[9] event clear, 0 : don't care, 1 : event status register clear	0
[8]	R/W	**GPIOxEVT8**	R : GPIO[8] event status, 0 : event not detected, 1 : event detected W : GPIO[8] event clear, 0 : don't care, 1 : event status register clear	0
[7]	R/W	**GPIOxEVT7**	R : GPIO[7] event status, 0 : event not detected, 1 : event detected W : GPIO[7] event clear, 0 : don't care, 1 : event status register clear	0
[6]	R/W	**GPIOxEVT6**	R : GPIO[6] event status, 0 : event not detected, 1 : event detected W : GPIO[6] event clear, 0 : don't care, 1 : event status register clear	0
[5]	R/W	**GPIOxEVT5**	R : GPIO[5] event status, 0 : event not detected, 1 : event detected W : GPIO[5] event clear, 0 : don't care, 1 : event status register clear	0
[4]	R/W	**GPIOxEVT4**	R : GPIO[4] event status, 0 : event not detected, 1 : event detected W : GPIO[4] event clear, 0 : don't care, 1 : event status register clear	0
[3]	R/W	**GPIOxEVT3**	R : GPIO[3] event status, 0 : event not detected, 1 : event detected W : GPIO[3] event clear, 0 : don't care, 1 : event status register clear	0
[2]	R/W	**GPIOxEVT2**	R : GPIO[2] event status, 0 : event not detected, 1 : event detected W : GPIO[2] event clear, 0 : don't care, 1 : event status register clear	0
[1]	R/W	**GPIOxEVT1**	R : GPIO[1] event status, 0 : event not detected, 1 : event detected W : GPIO[1] event clear, 0 : don't care, 1 : event status register clear	0
[0]	R/W	**GPIOxEVT0**	R : GPIO[0] event status, 0 : event not detected, 1 : event detected W : GPIO[0] event clear, 0 : don't care, 1 : event status register clear	0

TABLE 11-97. GPIOX EVENT REGISTER

GPIO PAD Selection Register (GPIOPADSEL)

This Register multiplexes and controls the MPEG I/F, CD-ROM Decoder, and USB signals out of GPIO pins.

Address : 0xC000 1120

Bit	R/W	Description	Reset Value
[4]	R/W	0 : UART2 1 : IrDA	0

Bit	R/W	Description	Reset Value
[3]	R/W	MPEG Interface PAD Selection 0 : GPIOM[8:4] GPIOM[8] : TSISYNC GPIOM[7] : TSIDP GPIOM[6] : TSIERR GPIOM[5] : TSIDI0 GPIOM[4] : TSICLK 1 : GPION[7:3] GPION[7] : TSISYNC GPION[6] : TSIDP GPION[5] : TSIERR GPION[4] : TSIDI0 GPION[3] : TSICLK	0
[2]	R/W	CDROM Interface PAD Selection 0 : GPIOM[8:6] GPIOM[8] : LRCK GPIOM[7] : BCK GPIOM[6] : SDAT 1 : GPION[5:3] GPION[5] : LRCK GPION[4] : BCK GPION[3] : SDAT	0
[1]	R/W	USB PAD 3 Type 0 : USB Host 1 : USB Device	0
[0]	R/W	USB PAD 1 Type 0 : USB Host 1 : USB Device	0

TABLE 11-98. GPIO PAD SELECTION REGISTER

GPIO Group Event Register (GPIOGREVTSTAT)

This Register shows if events by GPIO group were detected or not. Each bit indicates one GPIO group. If its value is 1, then an event was detected.

Address : 0xC000 1140

Bit	R/W	Symbol	Description	Reset Value
[14]	R	**GPIOOEVTST**	GPIOO event status, 0 : event not detected, 1 : event detected	0
[13]	R	**GPIONEVTST**	GPION event status, 0 : event not detected, 1 : event detected	0

Bit	R/W	Symbol	Description	Reset Value
[12]	R	**GPIOMEVTST**	GPIOM event status, 0 : event not detected, 1 : event detected	0
[11]	R	**GPIOLEVTST**	GPIOL event status, 0 : event not detected, 1 : event detected	0
[10]	R	**GPIOKEVTST**	GPIOK event status, 0 : event not detected, 1 : event detected	0
[9]	R	**GPIOJEVTST**	GPIOJ event status, 0 : event not detected, 1 : event detected	0
[8]	R	**GPIOIEVTST**	GPIOI event status, 0 : event not detected, 1 : event detected	0
[7]	R	**GPIOHEVTST**	GPIOH event status, 0 : event not detected, 1 : event detected	0
[6]	R	**GPIOGEVTST**	GPIOG event status, 0 : event not detected, 1 : event detected	0
[5]	R	**GPIOFEVTST**	GPIOF event status, 0 : event not detected, 1 : event detected	0
[4]	R	**GPIOEEVTST**	GPIOE event status, 0 : event not detected, 1 : event detected	0
[3]	R	**GPIODEVTST**	GPIOD event status, 0 : event not detected, 1 : event detected	0
[2]	R	**GPIOCEVTST**	GPIOC event status, 0 : event not detected, 1 : event detected	0
[1]	R	**GPIOBEVTST**	GPIOB event status, 0 : event not detected, 1 : event detected	0
[0]	R	**GPIOAEVTST**	GPIOA event status, 0 : event not detected, 1 : event detected	0

TABLE 11-99. GPIO GROUP EVENT REGISTER

GPIOx Pin Level Register (GPIOxPINLVL)

This Register can read the input signal level when GPIO pins are set to input mode.

GPIO	Address	GPIO	Address	GPIO	Address
GPIOA	***0xC000 1180h***	**GPIOF**	***0xC000 118Ah***	**GPIOK**	***0xC000 1194h***
GPIOB	***0xC000 1182h***	**GPIOG**	***0xC000 118Ch***	**GPIOL**	***0xC000 1196h***
GPIOC	***0xC000 1184h***	**GPIOH**	***0xC000 118Eh***	**GPIOM**	***0xC000 1198h***
GPIOD	***0xC000 1186h***	**GPIOI**	***0xC000 1190h***	**GPION**	***0xC000 119Ah***
GPIOE	***0xC000 1188h***	**GPIOJ**	***0xC000 1192h***	**GPIOO**	***0xC000 119Ch***

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W		GPIO[15] input level	0
[14]	R/W		GPIO[14] input level	0
[13]	R/W		GPIO[13] input level	0
[12]	R/W		GPIO[12] input level	0
[11]	R/W		GPIO[11] input level	0

Bit	R/W	Symbol	Description	Reset Value
[10]	R/W		GPIO[10] input level	0
[9]	R/W		GPIO[9] input level	0
[8]	R/W		GPIO[8] input level	0
[7]	R/W		GPIO[7] input level	0
[6]	R/W		GPIO[6] input level	0
[5]	R/W		GPIO[5] input level	0
[4]	R/W		GPIO[4] input level	0
[3]	R/W		GPIO[3] input level	0
[2]	R/W		GPIO[2] input level	0
[1]	R/W		GPIO[1] input level	0
[0]	R/W		GPIO[0] input level	0

TABLE 11-100. GPIOX PIN LEVEL REGISTER

GPIOE Output Alive Register (GPIOEOUT_ALIVE)

This Register sets up the output level of the GPIOE[15:0] pin when MP2520F executes the STOP Mode.

Address : 0xC000 11A0

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOE[15:0][?? – thru this section] alive output level	0

TABLE 11-101. GPIOE OUTPUT ALIVE REGISTER (GPIOEOUT_ALIVE)

GPIOE Output Enable Alive Register (GPIOEOUTENB_ALIVE)

This Register enables the GPIOE[15:0] pin to output when MP2520F executes the STOP Mode.

Address : 0xC000 11A2

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOE[15:0] alive output enable, 0 : output, 1 : input	0

TABLE 11-102. GPIOE OUTPUT ENABLE ALIVE REGISTER (GPIOEOUTENB_ALIVE)

GPIOE Pull Up Enable Alive Register (GPIOEPUENB_ALIVE)

This Register enables the GPIOE[15:0] pin to pull up when MP2520F executes the STOP Mode.

Address : 0xC000 11A4

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOE[15:0] alive pull up enable, 0 : pull up disable, 1 : pull up enable	0

TABLE 11-103. GPIOE PULL UP ENABLE ALIVE REGISTER (GPIOEPUENB_ALIVE)

GPIOF Output Alive Register (GPIOFOUT_ALIVE)

This Register sets up the output level of the GPIOF[9:0] pin when MP2520F executes the STOP Mode.

Address : 0xC000 11A6

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W		GPIOF[9:0] alive output level	0

TABLE 11-104. GPIOF OUTPUT ALIVE REGISTER (GPIOFOUT_ALIVE)

GPIOF Output Enable Alive Register (GPIOFOUTENB_ALIVE)

This Register enables the GPIOF[9:0] pin to output when MP2520F executes the STOP Mode.

Address : 0xC000 11A8

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W		GPIOF[9:0] alive output enable, 0 : output, 1 : input	0

TABLE 11-105. GPIOF OUTPUT ENABLE ALIVE REGISTER (GPIOFOUTENB_ALIVE)

GPIOF Pull Up Enable Alive Register (GPIOFPUENB_ALIVE)

This Register enables the GPIOF[9:0] pin to pull up when MP2520F executes the STOP Mode.

Address : 0xC000 11AA

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W		GPIOF[9:0] alive pull up enable, 0 : disable, 1 : enable	0

TABLE 11-106. GPIOF PULL UP ENABLE ALIVE REGISTER (GPIOFPUENB_ALIVE)

GPIOG Output Alive Register (GPIOGOUT_ALIVE)

This Register sets up the output level of the GPIOG[15:0] pin when MP2520F executes the STOP Mode.

Address : 0xC000 11AC

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOG[15:0] alive output level	0

TABLE 11-107. GPIOG OUTPUT ALIVE REGISTER (GPIOGOUT_ALIVE)

GPIOG Output Enable Alive Register (GPIOGOUTENB_ALIVE)

This Register enables the GPIOG[15:0] pin to output when MP2520F executes the STOP Mode.

Address : 0xC000 11AE

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOG[15:0] alive output enable, 0 : output, 1 : input	0

TABLE 11-108. GPIOG OUTPUT ENABLE ALIVE REGISTER (GPIOGOUTENB_ALIVE)

GPIOG Pull Up Enable Register (GPIOGPUENB_ALIVE)

This Register enables the GPIOG[15:0] pin to pull up when MP2520F executes the STOP Mode.

Address : 0xC000 11B0

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOG[15:0] alive pull up enable, 0 : disable, 1 : enable	0

TABLE 11-109. GPIOG PULL UP ENABLE REGISTER (GPIOGPUENB_ALIVE)

GPIOI Output Alive Register (GPIOIOUT_ALIVE)

This Register sets up the output level of the GPIOI[15:0] pin when MP2520F executes the STOP Mode.

Address : 0xC000 11B2

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOI[15:0] alive output level	0

TABLE 11-110. GPIOI OUTPUT ALIVE REGISTER (GPIOIOUT_ALIVE)

GPIOI Output Enable Alive Register (GPIOIOUTENB_ALIVE)

This Register enables the GPIOI[15:0] pin to output when MP2520F executes the STOP Mode.

Address : 0xC000 11B4

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOI[15:0] alive output enable, 0 : output, 1 : input	0

TABLE 11-111. GPIOI OUTPUT ENABLE ALIVE REGISTER (GPIOIOUTENB_ALIVE)

GPIOI Pull Up Enable Alive Register (GPIOIPUENB_ALIVE)

This Register enables the GPIOI[15:0] pin to pull up when MP2520F executes the STOP Mode.

Address : 0xC000 11B6

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOI[15:0] alive pull up enable, 0 : disable, 1 : enable	0

TABLE 11-112. GPIOI PULL UP ENABLE ALIVE REGISTER (GPIOIPUENB_ALIVE)

GPIOJ Output Alive Register (GPIOJOUT_ALIVE)

This Register sets up the output level of the GPIOJ[15:0] pin when MP2520F executes the STOP Mode.

Address : 0xC000 11B8

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOJ[15:0] alive output level	0

TABLE 11-113. GPIOJ OUTPUT ALIVE REGISTER (GPIOJOUT_ALIVE)

GPIOJ Output Enable Alive Register (GPIOJOUTENB_ALIVE)

This Register enables the GPIOJ[15:0] pin to output when MP2520F executes the STOP Mode.

Address : 0xC000 11BA

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOJ[15:0] alive output enable, 0 : output, 1 : input	0

TABLE 11-114. GPIOJ OUTPUT ENABLE ALIVE REGISTER (GPIOJOUTENB_ALIVE)

GPIOJ Pull Up Enable Alive Register (GPIOJPUENB_ALIVE)

This Register enables the GPIOJ[15:0] pin to pull up when MP2520F executes the STOP Mode.

Address : 0xC000 11BC

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W		GPIOJ[15:0] alive pull up enable, 0 : disable, 1 : enable	0

TABLE 11-115. GPIOJ PULL UP ENABLE ALIVE REGISTER (GPIOJPUENB_ALIVE)

11.3 GPIO REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
GPIOA Alternate Function High Register (GPIOAALTFNHI) *Address : 0xC0001040h* *GPIOAALTFNHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOA15_ALTFN**	**GPIOA[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOA14_ALTFN**	**GPIOA[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOA13_ALTFN**	**GPIOA[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOA12_ALTFN**	**GPIOA[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOA11_ALTFN**	**GPIOA[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOA10_ALTFN**	**GPIOA[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOA9_ALTFN**	**GPIOA[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOA8_ALTFN**	**GPIOA[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOA Alternate Function Low Register (GPIOAALTFNLOW) *Address : 0xC0001020h* *GPIOAALTFNLO Default Value : 16'h0000*				
[15:14]	R/W	**GPIOA7_ALTFN**	**GPIOA[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOA6_ALTFN**	**GPIOA[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOA5_ALTFN**	**GPIOA[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOA4_ALTFN**	**GPIOA[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOA3_ALTFN**	**GPIOA[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOA2_ALTFN**	**GPIOA[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOA1_ALTFN**	**GPIOA[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOA0_ALTFN**	**GPIOA[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOB Alternate Function High Register (GPIOBALTFNHI) *Address : 0xC0001042h* *GPIOBALTFNHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOB15_ALTFN**	**GPIOB[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOB14_ALTFN**	**GPIOB[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOB13_ALTFN**	**GPIOB[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOB12_ALTFN**	**GPIOB[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOB11_ALTFN**	**GPIOB[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[5:4]	R/W	**GPIOB10_ALTFN**	**GPIOB[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOB9_ALTFN**	**GPIOB[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOB8_ALTFN**	**GPIOB[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOB Alternate Function Low Register (GPIOBALTFNLOW) *Address : 0xC0001022h*			*GPIOBALTFNLO Default Value : 16'h0000*	
[15:14]	R/W	**GPIOB7_ALTFN**	**GPIOB[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOB6_ALTFN**	**GPIOB[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOB5_ALTFN**	**GPIOB[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOB4_ALTFN**	**GPIOB[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOB3_ALTFN**	**GPIOB[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOB2_ALTFN**	**GPIOB[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOB1_ALTFN**	**GPIOB[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOB0_ALTFN**	**GPIOB[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOC Alternate Function High Register (GPIOCALTFNHI) *Address : 0xC0001044h*			*GPIOCALTFNHI Default Value : 16'h0000*	
[15:14]	R/W	**GPIOC15_ALTFN**	**GPIOC[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOC14_ALTFN**	**GPIOC[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOC13_ALTFN**	**GPIOC[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOC12_ALTFN**	**GPIOC[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOC11_ALTFN**	**GPIOC[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOC10_ALTFN**	**GPIOC[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOC9_ALTFN**	**GPIOC[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOC8_ALTFN**	**GPIOC[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOC Alternate Function Low Register (GPIOCALTFNLOW) *Address : 0xC0001024h*			*GPIOCALTFNLO Default Value : 16'h0000*	
[15:14]	R/W	**GPIOC7_ALTFN**	**GPIOC[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOC6_ALTFN**	**GPIOC[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOC5_ALTFN**	**GPIOC[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOC4_ALTFN**	**GPIOC[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[7:6]	R/W	**GPIOC3_ALTFN**	**GPIOC[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOC2_ALTFN**	**GPIOC[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOC1_ALTFN**	**GPIOC[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOC0_ALTFN**	**GPIOC[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOD Alternate Function High Register (GPIODALTFNHI) *Address : 0xC0001046h*			*GPIODALTFNHI Default Value : 16'h0000*	
[15:14]	-	**Reserved**	-	-
[13:12]	-	**Reserved**	-	-
[11:10]	W	**GPIOD13_ALTFN**	**GPIOD[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOD12_ALTFN**	**GPIOD[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOD11_ALTFN**	**GPIOD[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOD10_ALTFN**	**GPIOD[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOD9_ALTFN**	**GPIOD[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOD8_ALTFN**	**GPIOD[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOD Alternate Function Low Register (GPIODALTFNLOW) *Address : 0xC0001026h*			*GPIODALTFNLO Default Value : 16'h000a*	
[15:14]	W	**GPIOD7_ALTFN**	**GPIOD[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOD6_ALTFN**	**GPIOD[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOD5_ALTFN**	**GPIOD[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOD4_ALTFN**	**GPIOD[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOD3_ALTFN**	**GPIOD[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOD2_ALTFN**	**GPIOD[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOD1_ALTFN**	**GPIOD[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	W	**GPIOD0_ALTFN**	**GPIOD[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOD Alternate Function High Register (GPIODALTFNHI) *Address : 0xC0001046h*			*GPIODALTFNHI Default Value : 16'h0000*	
[15:14]	-	**Reserved**	-	-
[13:12]	R	**GPIOD13_ALTFN**	**GPIOD[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	**GPIOD12_ALTFN**	**GPIOD[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[9:8]	R	**GPIOD11_ALTFN**	**GPIOD[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOD10_ALTFN**	**GPIOD[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOD9_ALTFN**	**GPIOD[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOD8_ALTFN**	**GPIOD[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOD7_ALTFN**	**GPIOD[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOD Alternate Function Low Register (GPIODALTFNLOW) *Address : 0xC0001026h*			*GPIODALTFNLO Default Value : 16'h000a*	
[15:14]	-	**Reserved**	-	-
[13:12]	R	**GPIOD6_ALTFN**	**GPIOD[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	**GPIOD5_ALTFN**	**GPIOD[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R	**GPIOD4_ALTFN**	**GPIOD[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOD3_ALTFN**	**GPIOD[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOD2_ALTFN**	**GPIOD[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOD1_ALTFN**	**GPIOD[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R	**GPIOD0_ALTFN**	**GPIOD[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOE Alternate Function High Register (GPIOEALTFNHI) *Address : 0xC0001048h*			*GPIOEALTFNHI Default Value : 16'haaaa*	
[15:14]	R/W	**GPIOE15_ALTFN**	**GPIOE[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[13:12]	R/W	**GPIOE14_ALTFN**	**GPIOE[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[11:10]	R/W	**GPIOE13_ALTFN**	**GPIOE[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[9:8]	R/W	**GPIOE12_ALTFN**	**GPIOE[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[7:6]	R/W	**GPIOE11_ALTFN**	**GPIOE[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[5:4]	R/W	**GPIOE10_ALTFN**	**GPIOE[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[3:2]	R/W	**GPIOE9_ALTFN**	**GPIOE[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R/W	**GPIOE8_ALTFN**	**GPIOE[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOE Alternate Function Low Register (GPIOEALTFNLOW) *Address : 0xC0001028h*			*GPIOEALTFNLO Default Value : 16'haaaa*	
[15:14]	R/W	**GPIOE7_ALTFN**	**GPIOE[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[13:12]	R/W	**GPIOE6_ALTFN**	**GPIOE[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10

Bit	R/W	Symbol	Description	Reset Value
[11:10]	R/W	**GPIOE5_ALTFN**	**GPIOE[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[9:8]	R/W	**GPIOE4_ALTFN**	**GPIOE[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[7:6]	R/W	**GPIOE3_ALTFN**	**GPIOE[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[5:4]	R/W	**GPIOE2_ALTFN**	**GPIOE[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[3:2]	R/W	**GPIOE1_ALTFN**	**GPIOE[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
[1:0]	R/W	**GPIOE0_ALTFN**	**GPIOE[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOF Alternate Function High Register (GPIOFALTFNHI) *Address : 0xC000104Ah*			*if SRAM Boot 4'ha else 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	W	**GPIOF9_ALTFN**	**GPIOF[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOF8_ALTFN**	**GPIOF[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOF Alternate Function Low Register (GPIOFALTFNLOW) *Address : 0xC000102Ah*			*if SRAM Boot 16'haaaa else 16'h0000*	
[15:14]	W	**GPIOF7_ALTFN**	**GPIOF[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOF6_ALTFN**	**GPIOF[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOF5_ALTFN**	**GPIOF[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOF4_ALTFN**	**GPIOF[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOF3_ALTFN**	**GPIOF[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOF2_ALTFN**	**GPIOF[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOF1_ALTFN**	**GPIOF[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOF0_ALTFN**	**GPIOF[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOF Alternate Function High Register (GPIOFALTFNHI) *Address : 0xC000104Ah*			*if SRAM Boot 4'ha else 16'h0000*	
[15:14]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOF9_ALTFN**	**GPIOF[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOF8_ALTFN**	**GPIOF[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOF7_ALTFN**	**GPIOF[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOF6_ALTFN**	**GPIOF[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOF5_ALTFN**	**GPIOF[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOF Alternate Function Low Register (GPIOFALTFNLOW) *Address : 0xC000102Ah*			*if SRAM Boot 16'haaaa else 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOF4_ALTFN**	**GPIOF[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOF3_ALTFN**	**GPIOF[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOF2_ALTFN**	**GPIOF[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOF1_ALTFN**	**GPIOF[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOF0_ALTFN**	**GPIOF[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOG Alternate Function High Register (GPIOGALTFNHI) *Address : 0xC000104Ch*			*if SRAM Boot 16'haaaa else 16'h0000*	
[15:14]	R/W	**GPIOG15_ALTFN**	**GPIOG[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOG14_ALTFN**	**GPIOG[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOG13_ALTFN**	**GPIOG[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOG12_ALTFN**	**GPIOG[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOG11_ALTFN**	**GPIOG[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOG10_ALTFN**	**GPIOG[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOG9_ALTFN**	**GPIOG[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOG8_ALTFN**	**GPIOG[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOG Alternate Function Low Register (GPIOGALTFNLOW) *Address : 0xC000102Ch*			*if SRAM Boot 16'haaaa else 16'h0000*	

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**GPIOG7_ALTFN**	**GPIOG[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOG6_ALTFN**	**GPIOG[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOG5_ALTFN**	**GPIOG[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOG4_ALTFN**	**GPIOG[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOG3_ALTFN**	**GPIOG[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOG2_ALTFN**	**GPIOG[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOG1_ALTFN**	**GPIOG[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOG0_ALTFN**	**GPIOG[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOH Alternate Function High Register (GPIOHALTFNHI) *Address : 0xC000104Eh* *GPIOHALTFNHI Default Value : reserved*				
[15:14]	-	-	**Reserved**	-
[13:12]	-	-	**Reserved**	-
[11:10]	-	-	**Reserved**	-
[9:8]	-	-	**Reserved**	-
[7:6]	-	-	**Reserved**	-
[5:4]	-	-	**Reserved**	-
[3:2]	-	-	**Reserved**	-
[1:0]	-	-	**Reserved**	-
GPIOH Alternate Function Low Register (GPIOHALTFNLOW) *Address : 0xC000102Eh* *GPIOHALTFNLO Default Value : 14'h0002*				
[15:14]	-	-	**Reserved**	-
[13:12]	W	**GPIOH6_ALTFN**	**GPIOH[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOH5_ALTFN**	**GPIOH[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOH4_ALTFN**	**GPIOH[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOH3_ALTFN**	**GPIOH[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOH2_ALTFN**	**GPIOH[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOH1_ALTFN**	**GPIOH[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOH0_ALTFN**	**GPIOH[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOH Alternate Function High Register (GPIOHALTFNHI)				

Bit	R/W	Symbol	Description	Reset Value
Address : 0xC000104Eh			*GPIOHALTFNHI Default Value : reserved*	
[15:13]	-	-	**Reserved**	-
[12:11]	-	-	**Reserved**	-
[19:9]	-	-	**Reserved**	-
[8:7]	-	-	**Reserved**	-
[6:5]	R	**GPIOH6_ALTFN**	**GPIOH[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	**GPIOH5_ALTFN**	**GPIOH[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	**GPIOH4_ALTFN**	**GPIOH[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	**GPIOH3_ALTFN**	**GPIOH[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
GPIOH Alternate Function Low Register (GPIOHALTFNLOW)				
Address : 0xC000102Eh			*GPIOHALTFNLO Default Value : 14'h0002*	
[15:13]	-	-	**Reserved**	-
[12:11]	-	-	**Reserved**	-
[10:9]	-	-	**Reserved**	-
[8:7]	-	-	**Reserved**	-
[6]	R	**GPIOH3_ALTFN**	**GPIOH[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[5:4]	R	**GPIOH2_ALTFN**	**GPIOH[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOH1_ALTFN**	**GPIOH[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOH0_ALTFN**	**GPIOH[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	10
GPIOI Alternate Function High Register (GPIOIALTFNHI)				
Address : 0xC0001050h			*GPIOIALTFNHI Default Value : 16'haaaa*	
[15:14]	R/W	**GPIOI15_ALTFN**	**GPIOI[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOI14_ALTFN**	**GPIOI[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOI13_ALTFN**	**GPIOI[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOI12_ALTFN**	**GPIOI[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOI11_ALTFN**	**GPIOI[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOI10_ALTFN**	**GPIOI[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOI9_ALTFN**	**GPIOI[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOI8_ALTFN**	**GPIOI[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
GPIOI Alternate Function Low Register (GPIOIALTFNLOW) *Address : 0xC0001030h* *GPIOIALTFNLO Default Value : 16'haaaa*				
[15:14]	R/W	**GPIOI7_ALTFN**	**GPIOI[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOI6_ALTFN**	**GPIOI[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOI5_ALTFN**	**GPIOI[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOI4_ALTFN**	**GPIOI[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOI3_ALTFN**	**GPIOI[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOI2_ALTFN**	**GPIOI[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOI1_ALTFN**	**GPIOI[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOI0_ALTFN**	**GPIOI[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOJ Alternate Function High Register (GPIOJALTFNHI) *Address : 0xC0001052h* *GPIOJALTFNHI Default Value : 16'haaaa*				
[15:14]	R/W	**GPIOJ15_ALTFN**	**GPIOJ[15]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOJ14_ALTFN**	**GPIOJ[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOJ13_ALTFN**	**GPIOJ[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOJ12_ALTFN**	**GPIOJ[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOJ11_ALTFN**	**GPIOJ[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOJ10_ALTFN**	**GPIOJ[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOJ9_ALTFN**	**GPIOJ[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R/W	**GPIOJ8_ALTFN**	**GPIOJ[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOJ Alternate Function Low Register (GPIOJALTFNLOW) *Address : 0xC0001032h* *GPIOJALTFNLO Default Value : 16'haaaa*				
[15:14]	R/W	**GPIOJ7_ALTFN**	**GPIOJ[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	R/W	**GPIOJ6_ALTFN**	**GPIOJ[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R/W	**GPIOJ5_ALTFN**	**GPIOJ[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R/W	**GPIOJ4_ALTFN**	**GPIOJ[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R/W	**GPIOJ3_ALTFN**	**GPIOJ[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R/W	**GPIOJ2_ALTFN**	**GPIOJ[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R/W	**GPIOJ1_ALTFN**	**GPIOJ[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[1:0]	R/W	**GPIOJ0_ALTFN**	**GPIOJ[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOK Alternate Function High Register (GPIOKALTFNHI) *Address : 0xC0001054h*			*GPIOKALTFNHI Default Value : reserved*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPIOK Alternate Function Low Register (GPIOKALTFNLOW) *Address : 0xC0001034h*			*GPIOKALTFNLO Default Value : 16'h0000*	
[15:14]	W	**GPIOK7_ALTFN**	**GPIOK[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOK6_ALTFN**	**GPIOK[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOK5_ALTFN**	**GPIOK[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOK4_ALTFN**	**GPIOK[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOK3_ALTFN**	**GPIOK[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOK2_ALTFN**	**GPIOK[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOK1_ALTFN**	**GPIOK[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOK0_ALTFN**	**GPIOK[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOK Alternate Function High Register (GPIOKALTFNHI) *Address : 0xC0001054h*			*GPIOKALTFNHI Default Value : reserved*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOK7_ALTFN**	**GPIOK[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOK6_ALTFN**	**GPIOK[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[3:2]	R	**GPIOK5_ALTFN**	**GPIOK[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOK4_ALTFN**	**GPIOK[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOK Alternate Function Low Register (GPIOKALTFNLOW) *Address : 0xC0001034h*			*GPIOKALTFNLO Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOK3_ALTFN**	**GPIOK[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOK2_ALTFN**	**GPIOK[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOK1_ALTFN**	**GPIOK[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOK0_ALTFN**	**GPIOK[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOL Alternate Function High Register (GPIOLALTFNHI) *Address : 0xC0001056h*			*GPIOLALTFNHI Default Value : 14'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOL14_ALTFN**	**GPIOL[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOL13_ALTFN**	**GPIOL[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOL12_ALTFN**	**GPIOL[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOL11_ALTFN**	**GPIOL[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOL10_ALTFN**	**GPIOL[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOL9_ALTFN**	**GPIOL[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOL8_ALTFN**	**GPIOL[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOL Alternate Function Low Register (GPIOLALTFNLOW) *Address : 0xC0001036h*			*GPIOLALTFNLO Default Value : 16'h0000*	
[15:14]	W	**GPIOL7_ALTFN**	**GPIOL[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOL6_ALTFN**	**GPIOL[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOL5_ALTFN**	**GPIOL[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOL4_ALTFN**	**GPIOL[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOL3_ALTFN**	**GPIOL[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
[5:4]	W	**GPIOL2_ALTFN**	**GPIOL[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOL1_ALTFN**	**GPIOL[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOL0_ALTFN**	**GPIOL[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOL Alternate Function High Register (GPIOLALTFNHI) *Address : 0xC0001056h*			*GPIOLALTFNHI Default Value : 14'h0000*	
[15]	-	-	Reserved	-
[14:13]	R	**GPIOL14_ALTFN**	**GPIOL[14]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[12:11]	R	**GPIOL13_ALTFN**	**GPIOL[13]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[10:9]	R	**GPIOL12_ALTFN**	**GPIOL[12]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[8:7]	R	**GPIOL11_ALTFN**	**GPIOL[11]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[6:5]	R	**GPIOL10_ALTFN**	**GPIOL[10]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	**GPIOL9_ALTFN**	**GPIOL[9]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	**GPIOL8_ALTFN**	**GPIOL[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	**GPIOL7_ALTFN**	**GPIOL[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
GPIOL Alternate Function Low Register (GPIOLALTFNLOW) *Address : 0xC0001036h*			*GPIOLALTFNLO Default Value : 16'h0000*	
[15]	-	-	Reserved	-
[14]	R	**GPIOL7_ALTFN**	**GPIOL[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[13:12]	R	**GPIOL6_ALTFN**	**GPIOL[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	R	**GPIOL5_ALTFN**	**GPIOL[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	R	**GPIOL4_ALTFN**	**GPIOL[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	R	**GPIOL3_ALTFN**	**GPIOL[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOL2_ALTFN**	**GPIOL[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOL1_ALTFN**	**GPIOL[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOL0_ALTFN**	**GPIOL[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOM Alternate Function High Register (GPIOMALTFNHI) *Address : 0xC0001058h*			*GPIOMALTFNHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	W	**GPIOM8_ALTFN**	**GPIOM[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOM Alternate Function Low Register (GPIOMALTFNLOW) *Address : 0xC0001038h* *GPIOMALTFNLO Default Value : 16'h0000*				
[15:14]	W	**GPIOM7_ALTFN**	**GPIOM[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPIOM6_ALTFN**	**GPIOM[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPIOM5_ALTFN**	**GPIOM[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOM3_ALTFN**	**GPIOM[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOM2_ALTFN**	**GPIOM[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOM1_ALTFN**	**GPIOM[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOM0_ALTFN**	**GPIOM[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOM Alternate Function High Register (GPIOMALTFNHI) *Address : 0xC0001058h* *GPIOMALTFNHI Default Value : 16'h0000*				
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	R	**GPIOM8_ALTFN**	**GPIOM[8]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[6:5]	R	**GPIOM7_ALTFN**	**GPIOM[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[4:3]	R	**GPIOM6_ALTFN**	**GPIOM[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[2:1]	R	**GPIOM5_ALTFN**	**GPIOM[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[0]	R	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
GPIOM Alternate Function Low Register (GPIOMALTFNLOW) *Address : 0xC0001038h* *GPIOMALTFNLO Default Value : 16'h0000*				
[15:13]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8]	R	**GPIOM4_ALTFN**	**GPIOM[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	0
[7:6]	R	**GPIOM3_ALTFN**	**GPIOM[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPIOM2_ALTFN**	**GPIOM[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOM1_ALTFN**	**GPIOM[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOM0_ALTFN**	**GPIOM[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPION Alternate Function High Register (GPIONALTFNHI) *Address : 0xC000105Ah*			*GPIONALTFNHI Default Value : reserved*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPION Alternate Function Low Register (GPIONALTFNLOW) *Address : 0xC000103Ah*			*GPIONALTFNLO Default Value : 16'h0000*	
[15:14]	W	**GPION7_ALTFN**	**GPION[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[13:12]	W	**GPION6_ALTFN**	**GPION[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[11:10]	W	**GPION5_ALTFN**	**GPION[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPION4_ALTFN**	**GPION[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPION3_ALTFN**	**GPION[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPION2_ALTFN**	**GPION[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPION1_ALTFN**	**GPION[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPION0_ALTFN**	**GPION[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPION Alternate Function High Register (GPIONALTFNHI) *Address : 0xC000105Ah*			*GPIONALTFNHI Default Value : reserved*	

Bit	R/W	Symbol	Description	Reset Value
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPION7_ALTFN**	**GPION[7]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPION6_ALTFN**	**GPION[6]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPION5_ALTFN**	**GPION[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPION4_ALTFN**	**GPION[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPION Alternate Function Low Register (GPIONALTFNLOW) *Address : 0xC000103Ah* *GPIONALTFNLO Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPION3_ALTFN**	**GPION[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	R	**GPION2_ALTFN**	**GPION[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPION1_ALTFN**	**GPION[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPION0_ALTFN**	**GPION[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOO Alternate Function High Register (GPIOOALTFNHI) *Address : 0xC000105Ch* *GPIOOALTFNHI Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPIOO Alternate Function Low Register (GPIOOALTFNLOW)				

Bit	R/W	Symbol	Description	Reset Value
Address : 0xC000103Ch			*GPIOOALTFNLO Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIOO5_ALTFN**	**GPIOO[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[9:8]	W	**GPIOO4_ALTFN**	**GPIOO[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[7:6]	W	**GPIOO3_ALTFN**	**GPIOO[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[5:4]	W	**GPIOO2_ALTFN**	**GPIOO[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	W	**GPIOO1_ALTFN**	**GPIOO[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	W	**GPIOO0_ALTFN**	**GPIOO[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOO Alternate Function High Register (GPIOOALTFNHI)				
Address : 0xC000105Ch			*GPIOOALTFNHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOO5_ALTFN**	**GPIOO[5]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOO4_ALTFN**	**GPIOO[4]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOO3_ALTFN**	**GPIOO[3]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
GPIOO Alternate Function Low Register (GPIOOALTFNLOW)				
Address : 0xC000103Ch			*GPIOOALTFNLO Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOO2_ALTFN**	**GPIOO[2]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[3:2]	R	**GPIOO1_ALTFN**	**GPIOO[1]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00
[1:0]	R	**GPIOO0_ALTFN**	**GPIOO[0]** 00 : Input, 01 : Output, 10 : ALT Function 1, 11 : ALT Function 2	00

Bit	R/W	Symbol	Description	Reset Value
GPIOx Output Level Register (GPIOxOUT) ***Address : C000 1060h ~ C000 107Ch***				
[15]	R/W	**GPIOxOUT15**	GPIO[15] Output Level	0
[14]	R/W	**GPIOxOUT14**	GPIO[14] Output Level	0
[13]	R/W	**GPIOxOUT13**	GPIO[13] Output Level	0
[12]	R/W	**GPIOxOUT12**	GPIO[12] Output Level	0
[11]	R/W	**GPIOxOUT11**	GPIO[11] Output Level	0
[10]	R/W	**GPIOxOUT10**	GPIO[10] Output Level	0
[9]	R/W	**GPIOxOUT9**	GPIO[9] Output Level	0
[8]	R/W	**GPIOxOUT8**	GPIO[8] Output Level	0
[7]	R/W	**GPIOxOUT7**	GPIO[7] Output Level	0
[6]	R/W	**GPIOxOUT6**	GPIO[6] Output Level	0
[5]	R/W	**GPIOxOUT5**	GPIO[5] Output Level	0
[4]	R/W	**GPIOxOUT4**	GPIO[4] Output Level	0
[3]	R/W	**GPIOxOUT3**	GPIO[3] Output Level	0
[2]	R/W	**GPIOxOUT2**	GPIO[2] Output Level	0
[1]	R/W	**GPIOxOUT1**	GPIO[1] Output Level	0
[0]	R/W	**GPIOxOUT0**	GPIO[0] Output Level	0
GPIOA Event Type High Register (GPIOAEVTTYPHI) *Address : 0xC00010A0h* *GPIOAEVTTYPHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOAEVTTYP15**	**GPIOA[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOAEVTTYP14**	**GPIOA[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOAEVTTYP13**	**GPIOA[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOAEVTTYP12**	**GPIOA[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOAEVTTYP11**	**GPIOA[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOAEVTTYP10**	**GPIOA[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOAEVTTYP9**	**GPIOA[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOAEVTTYP8**	**GPIOA[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOA Event Type Low Register (GPIOAEVTTYPLOW)				

Bit	R/W	Symbol	Description	Reset Value
Address : 0xC0001080h			*GPIOAEVTTYP HI Default Value : 16'h0000*	
[15:14]	R/W	**GPIOAEVTTYP7**	**GPIOA[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOAEVTTYP6**	**GPIOA[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOAEVTTYP5**	**GPIOA[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOAEVTTYP4**	**GPIOA[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOAEVTTYP3**	**GPIOA[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOAEVTTYP2**	**GPIOA[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOAEVTTYP1**	**GPIOA[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOAEVTTYP0**	**GPIOA[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOB Event Type High Register (GPIOBEVTTYPHI)				
Address : 0xC00010A2h			*GPIOBEVTTYPHI Default Value : 16'h0000*	
[15:14]	R/W	**GPIOBEVTTYP15**	**GPIOB[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOBEVTTYP14**	**GPIOB[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOBEVTTYP13**	**GPIOB[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOBEVTTYP12**	**GPIOB[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOBEVTTYP11**	**GPIOB[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOBEVTTYP10**	**GPIOB[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOBEVTTYP9**	**GPIOB[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOBEVTTYP8**	**GPIOB[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOB Event Type Low Register (GPIOBEVTTYPLOW)				
Address : 0xC0001082h			*GPIOBEVTTYPLOW Default Value : 16'h0000*	
[15:14]	R/W	**GPIOBEVTTYP7**	**GPIOB[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOBEVTTYP6**	**GPIOB[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOBEVTTYP5**	**GPIOB[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOBEVTTYP4**	**GPIOB[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOBEVTTYP3**	**GPIOB[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOBEVTTYP2**	**GPIOB[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOBEVTTYP1**	**GPIOB[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOBEVTTYP0**	**GPIOB[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
GPIOC Event Type High Register (GPIOCEVTTYPHI) *Address : 0xC00010A4h*			*GPIOCEVTTYPHI Default Value : 16'h0000*	
[15:14]	R/W	**GPIOCEVTTYP15**	**GPIOC[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOCEVTTYP14**	**GPIOC[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOCEVTTYP13**	**GPIOC[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOCEVTTYP12**	**GPIOC[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOCEVTTYP11**	**GPIOC[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOCEVTTYP10**	**GPIOC[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOCEVTTYP9**	**GPIOC[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOCEVTTYP8**	**GPIOC[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOC Event Type Low Register (GPIOCEVTTYPLOW) *Address : 0xC0001084h*			*GPIOCEVTTYPLOW Default Value : 16'h0000*	
[15:14]	R/W	**GPIOCEVTTYP7**	**GPIOC[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOCEVTTYP6**	**GPIOC[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOCEVTTYP5**	**GPIOC[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOCEVTTYP4**	**GPIOC[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOCEVTTYP3**	**GPIOC[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOCEVTTYP2**	**GPIOC[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOCEVTTYP1**	**GPIOC[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOCEVTTYP0**	**GPIOC[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOD Event Type High Register (GPIODEVTTYPHI) *Address : 0xC00010A6h*			*GPIODEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIODEVTTYP13**	**GPIOD[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIODEVTTYP12**	**GPIOD[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIODEVTTYP11**	**GPIOD[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIODEVTTYP10**	**GPIOD[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIODEVTTYP9**	**GPIOD[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[1:0]	W	**GPIODEVTTYP8**	**GPIOD[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOD Event Type Low Register (GPIODEVTTYPLOW) *Address : 0xC0001086h*			*GPIODEVTTYPLOW Default Value : 16'h0000*	
[15:14]	W	**GPIODEVTTYP7**	**GPIOD[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIODEVTTYP6**	**GPIOD[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIODEVTTYP5**	**GPIOD[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIODEVTTYP4**	**GPIOD[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIODEVTTYP3**	**GPIOD[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIODEVTTYP2**	**GPIOD[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIODEVTTYP1**	**GPIOD[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIODEVTTYP0**	**GPIOD[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOD Event Type High Register (GPIODEVTTYPHI) *Address : 0xC00010A6h*			*GPIODEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	**-**	Reserved	-
[13:12]	R	**GPIODEVTTYP13**	**GPIOD[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00-
[11:10]	R	**GPIODEVTTYP12**	**GPIOD[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIODEVTTYP11**	**GPIOD[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIODEVTTYP10**	**GPIOD[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIODEVTTYP9**	**GPIOD[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIODEVTTYP8**	**GPIOD[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIODEVTTYP7**	**GPIOD[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOD Event Type Low Register (GPIODEVTTYPLOW) *Address : 0xC0001086h*			*GPIODEVTTYP HI Default Value : 16'h0000*	
[15:14]	-	**-**	Reserved	-
[13:12]	R	**GPIODEVTTYP6**	**GPIOD[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R	**GPIODEVTTYP5**	**GPIOD[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIODEVTTYP4**	**GPIOD[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIODEVTTYP3**	**GPIOD[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIODEVTTYP2**	**GPIOD[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[3:2]	R	**GPIODEVTTYP1**	**GPIOD[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIODEVTTYP0**	**GPIOD[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOE Event Type High Register (GPIOEEVTTYPHI) *Address : 0xC00010A8h* *GPIOEEVTTYPHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOEEVTTYP15**	**GPIOE[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOEEVTTYP14**	**GPIOE[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOEEVTTYP13**	**GPIOE[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOEEVTTYP12**	**GPIOE[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOEEVTTYP11**	**GPIOE[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOEEVTTYP10**	**GPIOE[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOEEVTTYP9**	**GPIOE[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOEEVTTYP8**	**GPIOE[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOE Event Type Low Register (GPIOEEVTTYPLOW) *Address : 0xC0001088h* *GPIOEEVTTYPLOW Default Value : 16'h0000*				
[15:14]	R/W	**GPIOEEVTTYP7**	**GPIOE[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOEEVTTYP6**	**GPIOE[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOEEVTTYP5**	**GPIOE[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOEEVTTYP4**	**GPIOE[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOEEVTTYP3**	**GPIOE[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOEEVTTYP2**	**GPIOE[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOEEVTTYP1**	**GPIOE[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOEEVTTYP0**	**GPIOE[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOF Event Type High Register (GPIOFEVTTYPHI) *Address : 0xC00010AAh* *GPIOFEVTTYPHI Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[5:4]	-	-	Reserved	-
[3:2]	W	**GPIOFEVTTYP9**	**GPIOF[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOFEVTTYP8**	**GPIOF[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOF Event Type Low Register (GPIOFEVTTYPLOW) *Address : 0xC000108Ah*			*GPIOFEVTTYPLOW Default Value : 16'h0000*	
[15:14]	W	**GPIOFEVTTYP7**	**GPIOF[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOFEVTTYP6**	**GPIOF[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOFEVTTYP5**	**GPIOF[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOFEVTTYP4**	**GPIOF[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOFEVTTYP3**	**GPIOF[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOFEVTTYP2**	**GPIOF[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOFEVTTYP1**	**GPIOF[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOFEVTTYP0**	**GPIOF[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOF Event Type High Register (GPIOFEVTTYPHI) *Address : 0xC00010AAh*			*GPIOFEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOFEVTTYP9**	**GPIOF[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIOFEVTTYP8**	**GPIOF[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOFEVTTYP7**	**GPIOF[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOFEVTTYP6**	**GPIOF[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOFEVTTYP5**	**GPIOF[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOF Event Type Low Register (GPIOFEVTTYPLOW) *Address : 0xC000108Ah*			*GPIOFEVTTYPLOW Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	R	**GPIOFEVTTYP4**	**GPIOF[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[7:6]	R	**GPIOFEVTTYP3**	**GPIOF[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOFEVTTYP2**	**GPIOF[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOFEVTTYP1**	**GPIOF[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOFEVTTYP0**	**GPIOF[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOG Event Type High Register (GPIOGEVTTYPHI) *Address : 0xC00010ACh*			*GPIOGEVTTYPHI Default Value : 16'h0000*	
[15:14]	R/W	**GPIOGEVTTYP15**	**GPIOG[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOGEVTTYP14**	**GPIOG[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOGEVTTYP13**	**GPIOG[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOGEVTTYP12**	**GPIOG[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOGEVTTYP11**	**GPIOG[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOGEVTTYP10**	**GPIOG[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOGEVTTYP9**	**GPIOG[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOGEVTTYP8**	**GPIOG[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOG Event Type Low Register (GPIOGEVTTYPLOW) *Address : 0xC000108Ch*			*GPIOGEVTTYPLOW Default Value : 16'h0000*	
[15:14]	R/W	**GPIOGEVTTYP7**	**GPIOG[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOGEVTTYP6**	**GPIOG[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOGEVTTYP5**	**GPIOG[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOGEVTTYP4**	**GPIOG[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOGEVTTYP3**	**GPIOG[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOGEVTTYP2**	**GPIOG[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOGEVTTYP1**	**GPIOG[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOGEVTTYP0**	**GPIOG[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOH Event Type High Register (GPIOHEVTTYPHI) *Address : 0xC00010AEh*			*GPIOHEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPIOH Event Type Low Register (GPIOHEVTTYPLOW) *Address : 0xC000108Eh* *GPIOHEVTTYPLOW Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOHEVTTYP6**	**GPIOH[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOHEVTTYP5**	**GPIOH[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOHEVTTYP4**	**GPIOH[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOHEVTTYP2**	**GPIOH[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOHEVTTYP1**	**GPIOH[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOHEVTTYP0**	**GPIOH[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOH Event Type High Register (GPIOHEVTTYPHI) *Address : 0xC00010AEh* *GPIOHEVTTYPHI Default Value : 16'h0000*				
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6:5]	R	**GPIOHEVTTYP6**	**GPIOH[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOHEVTTYP5**	**GPIOH[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOHEVTTYP4**	**GPIOH[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[0]	R	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
GPIOH Event Type Low Register (GPIOHEVTTYPLOW) *Address : 0xC000108Eh* *GPIOHEVTTYPLOW Default Value : 16'h0000*				
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[10:9]	-	-	Reserved	-
[8:7]	-	-	Reserved	-
[6]	R	**GPIOHEVTTYP3**	**GPIOH[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[5:4]	R	**GPIOHEVTTYP2**	**GPIOH[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOHEVTTYP1**	**GPIOH[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOHEVTTYP0**	**GPIOH[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOI Event Type High Register (GPIOIEVTTYPHI) *Address : 0xC00010B0h* *GPIOIEVTTYPHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOIEVTTYP15**	**GPIOI[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOIEVTTYP14**	**GPIOI[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOIEVTTYP13**	**GPIOI[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOIEVTTYP12**	**GPIOI[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOIEVTTYP11**	**GPIOI[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOIEVTTYP10**	**GPIOI[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOIEVTTYP9**	**GPIOI[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOIEVTTYP8**	**GPIOI[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOI Event Type Low Register (GPIOIEVTTYPLOW) *Address : 0xC0001090h* *GPIOIEVTTYPLOW Default Value : 16'h0000*				
[15:14]	R/W	**GPIOIEVTTYP7**	**GPIOI[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOIEVTTYP6**	**GPIOI[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOIEVTTYP5**	**GPIOI[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOIEVTTYP4**	**GPIOI[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOIEVTTYP3**	**GPIOI[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOIEVTTYP2**	**GPIOI[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOIEVTTYP1**	**GPIOI[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOIEVTTYP0**	**GPIOI[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOJ Event Type High Register (GPIOJEVTTYPHI) *Address : 0xC00010B2h* *GPIOJEVTTYPHI Default Value : 16'h0000*				
[15:14]	R/W	**GPIOJEVTTYP15**	**GPIOJ[15]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[13:12]	R/W	**GPIOJEVTTYP14**	**GPIOJ[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOJEVTTYP13**	**GPIOJ[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOJEVTTYP12**	**GPIOJ[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOJEVTTYP11**	**GPIOJ[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOJEVTTYP10**	**GPIOJ[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOJEVTTYP9**	**GPIOJ[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOJEVTTYP8**	**GPIOJ[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOJ Event Type Low Register (GPIOJEVTTYPLOW) *Address : 0xC0001092h*			*GPIOJEVTTYPLOW Default Value : 16'h0000*	
[15:14]	R/W	**GPIOJEVTTYP7**	**GPIOJ[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	R/W	**GPIOJEVTTYP6**	**GPIOJ[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R/W	**GPIOJEVTTYP5**	**GPIOJ[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R/W	**GPIOJEVTTYP4**	**GPIOJ[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R/W	**GPIOJEVTTYP3**	**GPIOJ[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R/W	**GPIOJEVTTYP2**	**GPIOJ[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R/W	**GPIOJEVTTYP1**	**GPIOJ[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R/W	**GPIOJEVTTYP0**	**GPIOJ[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOK Event Type High Register (GPIOKEVTTYPHI) *Address : 0xC00010B4h*			*GPIOKEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPIOK Event Type Low Register (GPIOKEVTTYPLOW) *Address : 0xC0001094h*			*GPIOKEVTTYPLOW Default Value : 16'h0000*	

Bit	R/W	Symbol	Description	Reset Value
[15:14]	W	**GPIOKEVTTYP7**	**GPIOK[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOKEVTTYP6**	**GPIOK[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOKEVTTYP5**	**GPIOK[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOKEVTTYP4**	**GPIOK[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOKEVTTYP3**	**GPIOK[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOKEVTTYP2**	**GPIOK[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOKEVTTYP1**	**GPIOK[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOKEVTTYP0**	**GPIOK[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOK Event Type High Register (GPIOKEVTTYPHI) *Address : 0xC00010B4h*			*GPIOKEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOKEVTTYP7**	**GPIOK[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOKEVTTYP6**	**GPIOK[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOKEVTTYP5**	**GPIOK[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOKEVTTYP4**	**GPIOK[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOK Event Type Low Register (GPIOKEVTTYPLOW) *Address : 0xC0001094h*			*GPIOKEVTTYPLOW Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIOKEVTTYP3**	**GPIOK[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOKEVTTYP2**	**GPIOK[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOKEVTTYP1**	**GPIOK[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOKEVTTYP0**	**GPIOK[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOL Event Type High Register (GPIOLEVTTYPHI)				

Bit	R/W	Symbol	Description	Reset Value
Address : 0xC00010B6h			*GPIOLEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	W	**GPIOLEVTTYP14**	**GPIOL[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOLEVTTYP13**	**GPIOL[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOLEVTTYP12**	**GPIOL[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOLEVTTYP11**	**GPIOL[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOLEVTTYP10**	**GPIOL[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOLEVTTYP9**	**GPIOL[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOLEVTTYP8**	**GPIOL[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOL Event Type Low Register (GPIOLEVTTYPLOW)				
Address : 0xC0001096h			*GPIOLEVTTYPLOW Default Value : 16'h0000*	
[15:14]	W	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOLEVTTYP6**	**GPIOL[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOLEVTTYP5**	**GPIOL[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOLEVTTYP4**	**GPIOL[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOLEVTTYP3**	**GPIOL[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOLEVTTYP2**	**GPIOL[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOLEVTTYP1**	**GPIOL[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOLEVTTYP0**	**GPIOL[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOL Event Type High Register (GPIOLEVTTYPHI)				
Address : 0xC00010B6h			*GPIOLEVTTYPHI Default Value : 16'h0000*	
[15]	-	-	Reserved	-
[14:13]	R	**GPIOLEVTTYP14**	**GPIOL[14]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[12:11]	R/W	**GPIOLEVTTYP13**	**GPIOL[13]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[10:9]	R	**GPIOLEVTTYP12**	**GPIOL[12]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[8:7]	R	**GPIOLEVTTYP11**	**GPIOL[11]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[6:5]	R	**GPIOLEVTTYP10**	**GPIOL[10]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOLEVTTYP9**	**GPIOL[9]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOLEVTTYP8**	**GPIOL[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[0]	R	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOL Event Type Low Register (GPIOLEVTTYPLOW) *Address : 0xC0001096h*			*GPIOLEVTTYPLOW Default Value : 16'h0000*	
[15]	-	-	Reserved	-
[14]	R	**GPIOLEVTTYP7**	**GPIOL[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[13:12]	R	**GPIOLEVTTYP6**	**GPIOL[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	R	**GPIOLEVTTYP5**	**GPIOL[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	R	**GPIOLEVTTYP4**	**GPIOL[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	R	**GPIOLEVTTYP3**	**GPIOL[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOLEVTTYP2**	**GPIOL[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOLEVTTYP1**	**GPIOL[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOLEVTTYP0**	**GPIOL[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOM Event Type High Register (GPIOMEVTTYPHI) *Address : 0xC00010B8h*			*GPIOMEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	W	**GPIOMEVTTYP8**	**GPIOM[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOM Event Type Low Register (GPIOMEVTTYPLOW) *Address : 0xC0001098h*			*GPIOMEVTTYPLOW Default Value : 16'h0000*	
[15:14]	W	**GPIOMEVTTYP7**	**GPIOM[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIOMEVTTYP6**	**GPIOM[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIOMEVTTYP5**	**GPIOM[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOMEVTTYP3**	**GPIOM[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00

Bit	R/W	Symbol	Description	Reset Value
[5:4]	W	**GPIOMEVTTYP2**	**GPIOM[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOMEVTTYP1**	**GPIOM[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOMEVTTYP0**	**GPIOM[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOM Event Type High Register (GPIOMEVTTYPHI) *Address : 0xC00010B8h*			*GPIOMEVTTYPHI Default Value : 16'h0000*	
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8:7]	R	**GPIOMEVTTYP8**	**GPIOM[8]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[6:5]	R	**GPIOMEVTTYP7**	**GPIOM[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[4:3]	R	**GPIOMEVTTYP6**	**GPIOM[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[2:1]	R	**GPIOMEVTTYP5**	**GPIOM[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[0]	R	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
GPIOM Event Type Low Register (GPIOMEVTTYPLOW) *Address : 0xC0001098h*			*GPIOMEVTTYPLOW Default Value : 16'h0000*	
[15:13]	-	-	Reserved	-
[12:11]	-	-	Reserved	-
[10:9]	-	-	Reserved	-
[8]	R	**GPIOMEVTTYP4**	**GPIOM[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	0
[7:6]	R	**GPIOMEVTTYP3**	**GPIOM[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIOMEVTTYP2**	**GPIOM[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOMEVTTYP1**	**GPIOM[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOMEVTTYP0**	**GPIOM[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPION Event Type High Register (GPIONEVTTYPHI) *Address : 0xC00010BAh*			*GPIONEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPION Event Type Low Register (GPIONEVTTYPLOW) *Address : 0xC000109Ah* *GPIONEVTTYPLOW Default Value : 16'h0000*				
[15:14]	W	**GPIONEVTTYP7**	**GPION[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[13:12]	W	**GPIONEVTTYP6**	**GPION[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[11:10]	W	**GPIONEVTTYP5**	**GPION[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIONEVTTYP4**	**GPION[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIONEVTTYP3**	**GPION[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIONEVTTYP2**	**GPION[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIONEVTTYP1**	**GPION[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIONEVTTYP0**	**GPION[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPION Event Type High Register (GPIONEVTTYPHI) *Address : 0xC00010BAh* *GPIONEVTTYPHI Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIONEVTTYP7**	**GPION[7]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIONEVTTYP6**	**GPION[6]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIONEVTTYP5**	**GPION[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIONEVTTYP4**	**GPION[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPION Event Type Low Register (GPIONEVTTYPLOW) *Address : 0xC000109Ah* *GPIONEVTTYPLOW Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[9:8]	-	-	Reserved	-
[7:6]	R	**GPIONEVTTYP3**	**GPION[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	R	**GPIONEVTTYP2**	**GPION[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIONEVTTYP1**	**GPION[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIONEVTTYP0**	**GPION[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOO Event Type High Register (GPIOOEVTTYPHI) *Address : 0xC00010BCh*			*GPIOOEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	-	-	Reserved	-
[3:2]	-	-	Reserved	-
[1:0]	-	-	Reserved	-
GPIOO Event Type Low Register (GPIOOEVTTYPLOW) *Address : 0xC000109Ch*			*GPIOOEVTTYPLOW Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	W	**GPIOOEVTTYP5**	**GPIOO[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[9:8]	W	**GPIOOEVTTYP4**	**GPIOO[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[7:6]	W	**GPIOOEVTTYP3**	**GPIOO[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[5:4]	W	**GPIOOEVTTYP2**	**GPIOO[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	W	**GPIOOEVTTYP1**	**GPIOO[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	W	**GPIOOEVTTYP0**	**GPIOO[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOO Event Type High Register (GPIOOEVTTYPHI) *Address : 0xC00010BCh*			*GPIOOEVTTYPHI Default Value : 16'h0000*	
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-

Bit	R/W	Symbol	Description	Reset Value
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOOEVTTYP5**	**GPIOO[5]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOOEVTTYP4**	**GPIOO[4]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOOEVTTYP3**	**GPIOO[3]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOO Event Type Low Register (GPIOOEVTTYPLOW) *Address : 0xC000109Ch* *GPIOOEVTTYPLOW Default Value : 16'h0000*				
[15:14]	-	-	Reserved	-
[13:12]	-	-	Reserved	-
[11:10]	-	-	Reserved	-
[9:8]	-	-	Reserved	-
[7:6]	-	-	Reserved	-
[5:4]	R	**GPIOOEVTTYP2**	**GPIOO[2]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[3:2]	R	**GPIOOEVTTYP1**	**GPIOO[1]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
[1:0]	R	**GPIOOEVTTYP0**	**GPIOO[0]** 00 : Rising Edge 01 : Falling Edge 10 : High Level, 11 : Low Level	00
GPIOx Pull Up Enable Register (GPIOxPUENB) ***Address : C000 10C0h ~ C000 10DCh***				
[15]	R/W	**GPIOxPUENB15**	GPIO[15] pull up enable	3)
[14]	R/W	**GPIOxPUENB14**	GPIO[14] pull up enable	3)
[13]	R/W	**GPIOxPUENB13**	GPIO[13] pull up enable	3)
[12]	R/W	**GPIOxPUENB12**	GPIO[12] pull up enable	3)
[11]	R/W	**GPIOxPUENB11**	GPIO[11] pull up enable	3)
[10]	R/W	**GPIOxPUENB10**	GPIO[10] pull up enable	3)
[9]	R/W	**GPIOxPUENB9**	GPIO[9] pull up enable	3)
[8]	R/W	**GPIOxPUENB8**	GPIO[8] pull up enable	3)
[7]	R/W	**GPIOxPUENB7**	GPIO[7] pull up enable	3)
[6]	R/W	**GPIOxPUENB6**	GPIO[6] pull up enable	3)
[5]	R/W	**GPIOxPUENB5**	GPIO[5] pull up enable	3)
[4]	R/W	**GPIOxPUENB4**	GPIO[4] pull up enable	3)

Bit	R/W	Symbol	Description	Reset Value
[3]	R/W	**GPIOxPUENB3**	GPIO[3] pull up enable	3)
[2]	R/W	**GPIOxPUENB2**	GPIO[2] pull up enable	3)
[1]	R/W	**GPIOxPUENB1**	GPIO[1] pull up enable	3)
[0]	R/W	**GPIOxPUENB0**	GPIO[0] pull up enable	3)
GPIOx Interrupt Enable Register (GPIOxINTENB) ***Address : C000 10E0h ~ C000 10FCh***				
[15]	R/W	**GPIOxINTENB15**	GPIO[15] interrupt enable	1
[14]	R/W	**GPIOxINTENB14**	GPIO[14] interrupt enable	1
[13]	R/W	**GPIOxINTENB13**	GPIO[13] interrupt enable	1
[12]	R/W	**GPIOxINTENB12**	GPIO[12] interrupt enable	1
[11]	R/W	**GPIOxINTENB11**	GPIO[11] interrupt enable	1
[10]	R/W	**GPIOxINTENB10**	GPIO[10] interrupt enable	1
[9]	R/W	**GPIOxINTENB9**	GPIO[9] interrupt enable	1
[8]	R/W	**GPIOxINTENB8**	GPIO[8] interrupt enable	1
[7]	R/W	**GPIOxINTENB7**	GPIO[7] interrupt enable	1
[6]	R/W	**GPIOxINTENB6**	GPIO[6] interrupt enable	1
[5]	R/W	**GPIOxINTENB5**	GPIO[5] interrupt enable	1
[4]	R/W	**GPIOxINTENB4**	GPIO[4] interrupt enable	1
[3]	R/W	**GPIOxINTENB3**	GPIO[3] interrupt enable	1
[2]	R/W	**GPIOxINTENB2**	GPIO[2] interrupt enable	1
[1]	R/W	**GPIOxINTENB1**	GPIO[1] interrupt enable	1
[0]	R/W	**GPIOxINTENB0**	GPIO[0] interrupt enable	1
GPIOx Event Register (GPIOxEVT) ***Address : C000 1100h ~ C000 111Ch***				
[15]	R/W	**GPIOxEVT15**	R : GPIO[15] event status, 0 : event not detected, 1 : event detected W : GPIO[15] event clear, 0 : don't care, 1 : event status register clear	0
[14]	R/W	**GPIOxEVT14**	R : GPIO[14] event status, 0 : event not detected, 1 : event detected W : GPIO[14] event clear, 0 : don't care, 1 : event status register clear	0
[13]	R/W	**GPIOxEVT13**	R : GPIO[13] event status, 0 : event not detected, 1 : event detected W : GPIO[13] event clear, 0 : don't care, 1 : event status register clear	0
[12]	R/W	**GPIOxEVT12**	R : GPIO[12] event status, 0 : event not detected, 1 : event detected	0

Bit	R/W	Symbol	Description	Reset Value
			W : GPIO[12] event clear, 0 : don't care, 1 : event status register clear	
[11]	R/W	**GPIOxEVT11**	R : GPIO[11] event status, 0 : event not detected, 1 : event detected W : GPIO[11] event clear, 0 : don't care, 1 : event status register clear	0
[10]	R/W	**GPIOxEVT10**	R : GPIO[10] event status, 0 : event not detected, 1 : event detected W : GPIO[10] event clear, 0 : don't care, 1 : event status register clear	0
[9]	R/W	**GPIOxEVT9**	R : GPIO[9] event status, 0 : event not detected, 1 : event detected W : GPIO[9] event clear, 0 : don't care, 1 : event status register clear	0
[8]	R/W	**GPIOxEVT8**	R : GPIO[8] event status, 0 : event not detected, 1 : event detected W : GPIO[8] event clear, 0 : don't care, 1 : event status register clear	0
[7]	R/W	**GPIOxEVT7**	R : GPIO[7] event status, 0 : event not detected, 1 : event detected W : GPIO[7] event clear, 0 : don't care, 1 : event status register clear	0
[6]	R/W	**GPIOxEVT6**	R : GPIO[6] event status, 0 : event not detected, 1 : event detected W : GPIO[6] event clear, 0 : don't care, 1 : event status register clear	0
[5]	R/W	**GPIOxEVT5**	R : GPIO[5] event status, 0 : event not detected, 1 : event detected W : GPIO[5] event clear, 0 : don't care, 1 : event status register clear	0
[4]	R/W	**GPIOxEVT4**	R : GPIO[4] event status, 0 : event not detected, 1 : event detected W : GPIO[4] event clear, 0 : don't care, 1 : event status register clear	0
[3]	R/W	**GPIOxEVT3**	R : GPIO[3] event status, 0 : event not detected, 1 : event detected W : GPIO[3] event clear, 0 : don't care, 1 : event status register clear	0
[2]	R/W	**GPIOxEVT2**	R : GPIO[2] event status, 0 : event not detected, 1 : event detected W : GPIO[2] event clear, 0 : don't care, 1 : event status register clear	0
[1]	R/W	**GPIOxEVT1**	R : GPIO[1] event status, 0 : event not detected, 1 : event detected W : GPIO[1] event clear, 0 : don't care, 1 : event status register clear	0
[0]	R/W	**GPIOxEVT0**	R : GPIO[0] event status, 0 : event not detected, 1 : event detected W : GPIO[0] event clear, 0 : don't care, 1 : event status register clear	0
GPIO PAD Selection Register (GPIOPADSEL) **Address : 0xC000 1120h**				
[4]	R/W	**IrDA_IF_PAD**		0

Bit	R/W	Symbol	Description	Reset Value
[3]	R/W	**MPEG_IF_PAD**	MPEG Interface PAD Selection 0 : GPIOM[8:4] GPIOM[8] : TSISYNC GPIOM[7] : TSIDP GPIOM[6] : TSIERR GPIOM[5] : TSIDI0 GPIOM[4] : TSICLK 1 : GPION[7:3] GPION[7] : TSISYNC GPION[6] : TSIDP GPION[5] : TSIERR GPION[4] : TSIDI0 GPION[3] : TSICLK	0
[2]	R/W	**CDROM_IF_PAD**	CDROM Interface PAD Selection 0 : GPIOM[8:6] GPIOM[8] : LRCK GPIOM[7] : BCK GPIOM[6] : SDAT 1 : GPION[5:3] GPION[5] : LRCK GPION[4] : BCK GPION[3] : SDAT	0
[1]	R/W	**USB_PAD_3T**	USB PAD 3 Type 0 : USB Host 1 : USB Device	0
[0]	R/W	**USB_PAD_!T**	USB PAD 1 Type 0 : USB Host 1 : USB Device	0
GPIO Group Event Register (GPIOGREVTSTAT) ***Address : 0xC000 1140h***				
[14]	R	**GPIOOEVTST**	GPIOO event status, 0 : event not detected, 1 : event detected	0
[13]	R	**GPIONEVTST**	GPION event status, 0 : event not detected, 1 : event detected	0
[12]	R	**GPIOMEVTST**	GPIOM event status, 0 : event not detected, 1 : event detected	0
[11]	R	**GPIOLEVTST**	GPIOL event status, 0 : event not detected, 1 : event detected	0
[10]	R	**GPIOKEVTST**	GPIOK event status, 0 : event not detected, 1 : event detected	0
[9]	R	**GPIOJEVTST**	GPIOJ event status, 0 : event not detected, 1 : event detected	0

Bit	R/W	Symbol	Description	Reset Value
[8]	R	**GPIOIEVTST**	GPIOI event status, 0 : event not detected, 1 : event detected	0
[7]	R	**GPIOHEVTST**	GPIOH event status, 0 : event not detected, 1 : event detected	0
[6]	R	**GPIOGEVTST**	GPIOG event status, 0 : event not detected, 1 : event detected	0
[5]	R	**GPIOFEVTST**	GPIOF event status, 0 : event not detected, 1 : event detected	0
[4]	R	**GPIOEEVTST**	GPIOE event status, 0 : event not detected, 1 : event detected	0
[3]	R	**GPIODEVTST**	GPIOD event status, 0 : event not detected, 1 : event detected	0
[2]	R	**GPIOCEVTST**	GPIOC event status, 0 : event not detected, 1 : event detected	0
[1]	R	**GPIOBEVTST**	GPIOB event status, 0 : event not detected, 1 : event detected	0
[0]	R	**GPIOAEVTST**	GPIOA event status, 0 : event not detected, 1 : event detected	0
GPIOx Pin Level Register (GPIOxPINLVL) ***Address : C000 1180h ~ C000 119Ch***				
[15]	R/W	**GPIO_IL15**	GPIO[15] input level	0
[14]	R/W	**GPIO_IL14**	GPIO[14] input level	0
[13]	R/W	**GPIO_IL13**	GPIO[13] input level	0
[12]	R/W	**GPIO_IL12**	GPIO[12] input level	0
[11]	R/W	**GPIO_IL11**	GPIO[11] input level	0
[10]	R/W	**GPIO_IL10**	GPIO[10] input level	0
[9]	R/W	**GPIO_IL9**	GPIO[9] input level	0
[8]	R/W	**GPIO_IL8**	GPIO[8] input level	0
[7]	R/W	**GPIO_IL7**	GPIO[7] input level	0
[6]	R/W	**GPIO_IL6**	GPIO[6] input level	0
[5]	R/W	**GPIO_IL5**	GPIO[5] input level	0
[4]	R/W	**GPIO_IL4**	GPIO[4] input level	0
[3]	R/W	**GPIO_IL3**	GPIO[3] input level	0
[2]	R/W	**GPIO_IL2**	GPIO[2] input level	0
[1]	R/W	**GPIO_IL1**	GPIO[1] input level	0
[0]	R/W	**GPIO_IL0**	GPIO[0] input level	0
GPIOE Output Alive Register (GPIOEOUT_ALIVE) ***Address : 0xC000 11A0h***				
[15:0]	R/W	**GPIOE_AOI**	GPIOE[15:0] alive output level	0
GPIOE Output Enable Alive Register (GPIOEOUTENB_ALIVE)				

Bit	R/W	Symbol	Description	Reset Value
Address : 0xC000 11A2h				
[15:0]	R/W	**GPIOE_AO_ENB**	GPIOE[15:0] alive output enable, 0 : output, 1 : input	0
GPIOE Pull Up Enable Alive Register (GPIOEPUENB_ALIVE) ***Address : 0xC000 11A4h***				
[15:0]	R/W	**GPIOE_APP_ENB**	GPIOE[15:0] alive pull up enable, 0 : pull up disable, 1 : pull up enable	0
GPIOF Output Alive Register (GPIOFOUT_ALIVE) ***Address : 0xC000 11A6h***				
[9:0]	R/W	**GPIOF_AOL**	GPIOF[9:0] alive output level	0
GPIOF Output Enable Alive Register (GPIOFOUTENB_ALIVE) ***Address : 0xC000 11A8h***				
[9:0]	R/W	**GPIOF_AO_ENB**	GPIOF[9:0] alive output enable, 0 : output, 1 : input	0
GPIOF Pull Up Enable Alive Register (GPIOFPUENB_ALIVE) ***Address : 0xC000 11AAh***				
[9:0]	R/W	**GPIOF_AP_ENB**	GPIOF[9:0] alive pull up enable, 0 : disable, 1 : enable	0
GPIOG Output Alive Register (GPIOGOUT_ALIVE) ***Address : 0xC000 11ACh***				
[15:0]	R/W	**GPIOG_AOL**	GPIOG[15:0] alive output level	0
GPIOG Output Enable Alive Register (GPIOGOUTENB_ALIVE) ***Address : 0xC000 11AEh***				
[15:0]	R/W	**GPIOG_AO_ENB**	GPIOG[15:0] alive output enable, 0 : output, 1 : input	0
GPIOG Pull Up Enable Register (GPIOGPUENB_ALIVE) ***Address : 0xC000 11B0h***				
[15:0]	R/W	**GPIOG_AP_ENB**	GPIOG[15:0] alive pull up enable, 0 : disable, 1 : enable	0
GPIOI Output Alive Register (GPIOIOUT_ALIVE) ***Address : 0xC000 11B2h***				
[15:0]	R/W	**GPIOI_AOL**	GPIOI[15:0] alive output level	0
GPIOI Output Enable Alive Register (GPIOIOUTENB_ALIVE) ***Address : 0xC000 11B4h***				
[15:0]	R/W	**GPIOI_AO_ENB**	GPIOI[15:0] alive output enable,	0

Bit	R/W	Symbol	Description	Reset Value
			0 : output, 1 : input	
GPIOI Pull Up Enable Alive Register (GPIOIPUENB_ALIVE) ***Address : 0xC000 11B6h***				
[15:0]	R/W	**GPIOI_AP_ENB**	GPIOI[15:0] alive pull up enable, 0 : disable, 1 : enable	0
GPIOJ Output Alive Register (GPIOJOUT_ALIVE) ***Address : 0xC000 11B8h***				
[15:0]	R/W	**GPIOJ_AOL**	GPIOJ[15:0] alive output level	0
GPIOJ Output Enable Alive Register (GPIOJOUTENB_ALIVE) ***Address : 0xC000 11Bh***				
[15:0]	R/W	**GPIOJ_AO_ENB**	GPIOJ[15:0] alive output enable, 0 : output, 1 : input	0
GPIOJ Pull Up Enable Alive Register (GPIOJPUENB_ALIVE) ***Address : 0xC000 11BCh***				
[15:0]	R/W	**GPIOJ_AP_ENB**	GPIOJ[15:0] alive pull up enable, 0 : disable, 1 : enable	0
Bit	**R/W**	**Symbol**	**Description**	**Reset Value**

TABLE 11-116. GPIO REGISTERS LIST

CHAPTER 12

VIDEO PROCESSOR

12. VIDEO PROCESSOR

12.1 OVERVIEW

MP2520F has a Video Processor to restore compressed images. The Video Processor can decode or encode JPEG, MPEG1/2/4, H.263, etc. with the support of the CPU. The MP2520F contains the blocks to restore and encode the compressed images and these blocks are VLD/VLC, DCT/IDCT, Q/IQ, Prediction, ME, MC, etc. The blocks can be controlled by the CPU. In addition, an internal program can control the blocks in place of the CPU. The block to support the H.263 Annex J In-Loop De-block, as well as the above blocks, is built in. The block for De-block and De-ring are also included to enhance the quality of 'restore image'. Motion Prediction can perform Quarter sample mode interpolation, and one warping point of GMC. In other words, it is fully compatible with DIVX version 5.x .

FEATURES

Decoder

- MPEG1 – Video CD
- MPEG2 MP@ML Decode – DVD playback
- MPEG4 SP/ASP Decode @720 x 480, 30fps – DivX 3.11, 4x, 5x Playback
- H.263 Decode @352 x 288, 30fps – Video Stream Playback(CDMA, WiFi)
- JPEG Decode up to 4M pixels – DSC
- MJPEG Decode @720 x 480, 30fps - Security Cam

Encoder

- MPEG2 SP@ML Encode(Without B frame) – DVD Quality Record
- MPEG4 SP Encoder @720 x 480, 30fps – MPEG4 Camcorder, PVR, MMS
- JPEG Encode up to 4M pixels – DSC
- MJPEG Encode @720 x 480, 30fps - Security Cam

Codec

- MPEG4 SP/H.263 L3 Codec @352 x 288, 30fps – Video Conferencing

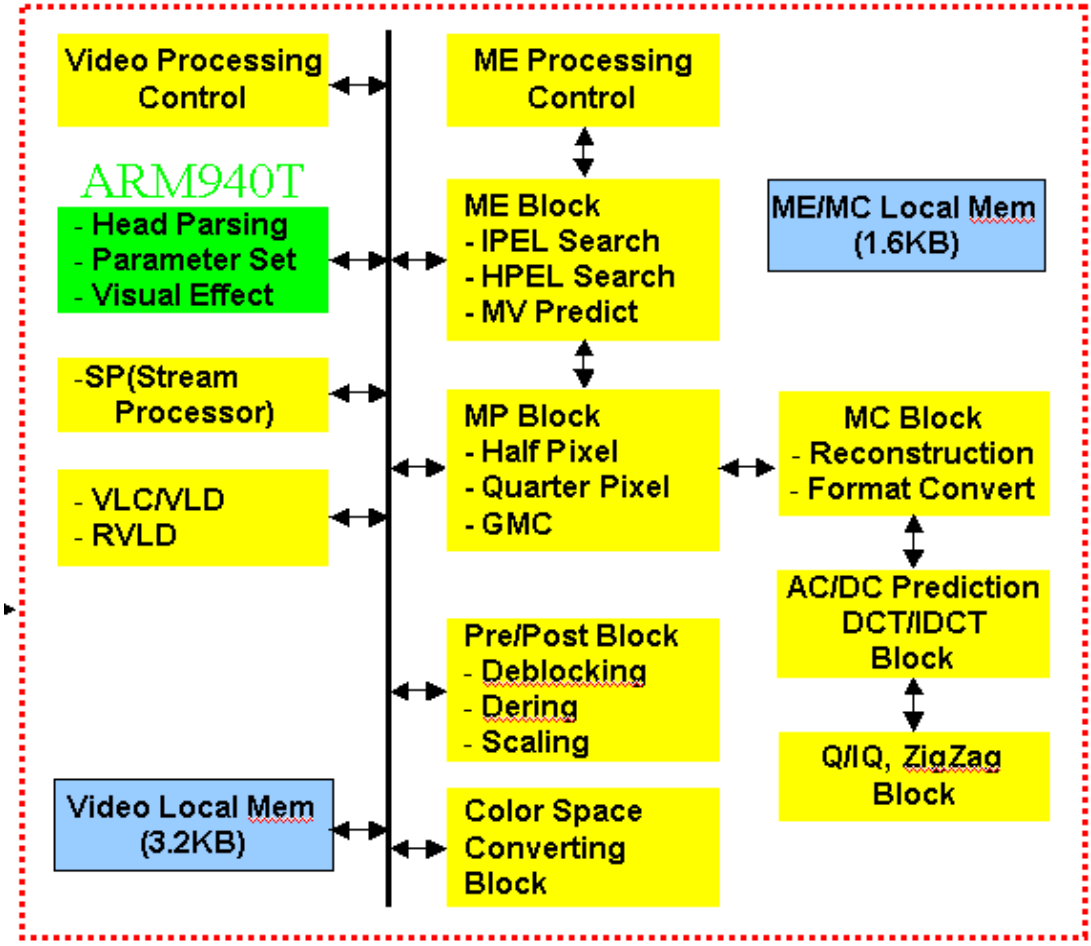


Figure 12-1. VIDEO PROCESSOR

12.2 VLD/VLC

In Decode Mode, VLD/VLC receives 'video stream data' as an input and stores variable length decoded 'run/level data' to the External Memory. In Encode Mode, it receives 'run/level data' as an input and stores 'variable length encoded video stream data' to the External Memory. The MP2520F VLD/VLC block is compatible with MPEG1, MPEG2, MPEG4 RVLD (RVLD table only), H263 and JPEG decode functions. In addition, it is compatible with MPEG2, MPEG4, H263 and JPEG encode functions. For the JPEG function, the VLD/VLC block supports the stuff byte addition or removal function.

12.3 PREDICTION

For MPEG1/2, H.263 and JPEG, the Prediction block only performs predictions about DC. For MPEG4, it performs predictions about both AC and DC.

12.4 QUANTIZATION (Q/IQ)

In Decoder Mode, the Q/IQ block quantizes the Data received from the AC/DC Predictor in reverse. The reverse quantized Data is then transferred to the IDCT block. This block is compatible with MPEG1/2/4, H263 and JPEG.

In Encoder Mode, the Q/IQ block quantizes Data transformed by the DCT in reverse and transfers the quantized coefficients to the AC/DC Predictor. In this case, this block supports MPEG1/2/4 and JPEG. However, when the 2nd quantization method is used for MPEG2 and MPEG4, the available quantized scales are limited to 1, 2, 4, 8 and 16.

12.5 DCT/IDCT

The IDCT block transforms the reverse quantized Data into Pixels or Pixel Differences and transfers it to the Motion Compensation block.

The DCT block is used only in Encode Mode, and transfers the Pixels or the Pixel Differences received from the Motion Prediction block into transformed coefficients. These transformed coefficients are quantized by the Q/IQ block.

12.6 MOTION ESTIMATION

The Motion Estimation block extracts motion vectors in Macro block units from an area with the range of (–64 ~ 63)(horizontal) and (–32 ~ 31) (vertical) in half pixel units.

With a two-stage hierarchical search algorithm, this block supports the unrestricted mode and the H.263 base mode.

12.7 MOTION PREDICTION

The Motion Prediction block creates a prediction image from the Reference Frame using -Motion vector. In addition, this block restores an image by means of Motion compensation, using a created prediction image and a difference image.

For Encoding, this block attains a difference image by comparing the current image to a Reference Image.

Motion Prediction is compatible with the Quarter Sample Mode Interpolation and the Global Motion Compensation (GMC) provided by the MPEG4 Advanced Simple Profile. However, only GMC with one Warping Point is supported for the GMC.

12.8 DEBLOCKING/DERING

Deblocking and Dering are used to remove the compressed distortion between blocks. In MPEG1/2/4, Deblocking is used as a Post-filter. By contrast, in H.263 Annex J, Deblocking is used as an Inloop Filter and Data created by the Deblocking is used as a Reference Frame. In addition, Dering is used toas a Post filter. The Deblocking Filter is compatible with

MPEG4 FDIS Annex F.3.1 and H.236 Annex Q.7 and the De-ring Filter is compatible with MPEG4 FDIS Annex F.3.2

CHAPTER 13

VIDEO POST PROCESSOR

13. VIDEO POST PROCESSOR

13.1 OVERVIEW

The Video Post Processor (VPP) has the Frame Dimension Converter, the Scale Processor, and Multi-Layer Controller Blocks.

The Data Path of each block is as shown in Figure 13.1. However, G Path and H Path are not linked together directly.

BLOCK DIAGRAM

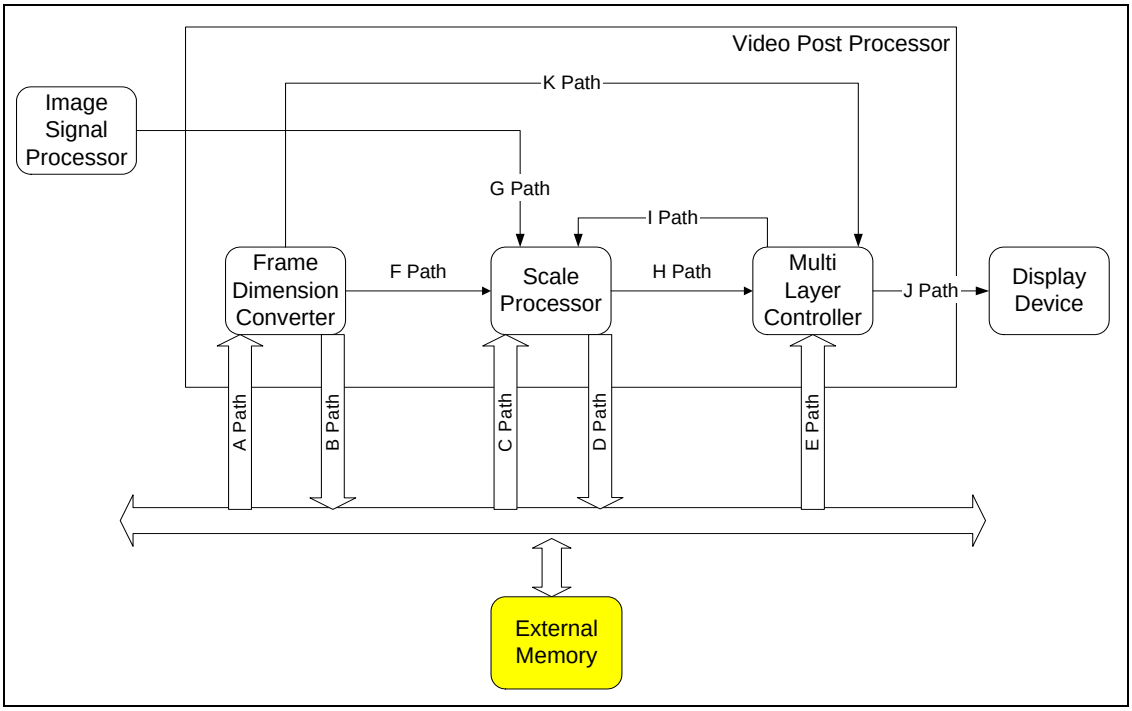


Figure 13-1. Video Post Processor Diagram

13.2 FRAME DIMENSION CONVERTER

13.2.1 Overview

The Frame Dimension Converter (FDC) transforms 2-D data made during the process of Encoding/Decoding MPEG into the 1-D Data format. During this work, 4:2:0 to 4:2:2 format conversion, the scaling about the vertical direction and Rotation are performed.

Features:

- 2-D Frame to 1-D Frame
- 4:2:0, 4:2:2, 4:4:4 à 4:2:2
- Rotation(0, 90, 180, 270)
- Vertical Scaling

Block Diagram

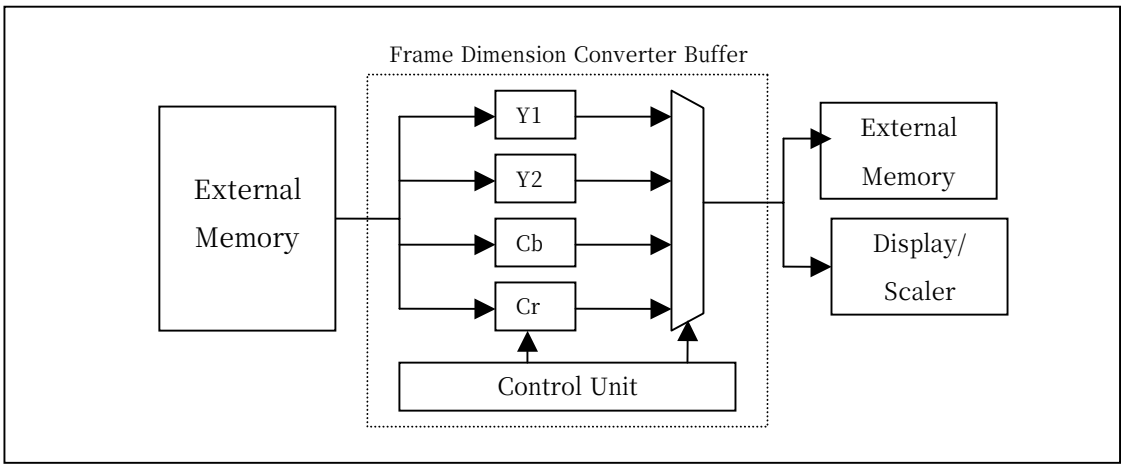


Figure 13-2. Frame Dimension Converter Block Diagram

13.2.2 FDC Register LIST

Control Register (FDC_CNTL)

Address : FDC_BASE + 0x0000

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**STOP**	Clear Format Converter	0
[14]	R/W	**FPC**	Field Polarity Control	0
[13:12]	R/W	**LC**	Lock Control 0 : No Lock Control 1 : 4 words 2 : 8 words 3: Lock Off	2'b10
[11]	R/W	**WRMOD**	Write mode 0: Ext mem --> Ext mem 1: Ext mem --> scaler/display	0
[10]	R/W	**SBFLD**	Bottom Field flag for Source Frame If a source format is a field, inform the position of the bottom field.	0
[9]	R/W	**DBFLD**	Bottom Field flag for Destination Frame If a destination format is a field, inform the field to be sent. However, if VES = 1, receive both the vertical sync input and the bottom input from outside.	0
[8]	R/W	**SFF**	Source Frame format 0 : frame 1 : field	0
[7]	R/W	**DFF**	Destination Frame format 0 : frame 1 : field *Note : When Write mode = 1, a destination format should always be a frame.*	0
[6]	R/W	**VSE**	Vertical Sync Enable (VSE)	0
[5]	R/W	**IsBIG**	Endian 0 : Little-Endian 1 : BIG-Endian	1b
[4:3]	R/W	**ROT**	Rotation 0 : 0 1 : 90 2 : 180 3 : 270 *Note : When the Write mode = 1, a rotation is possible only by 0 degrees and 180 degrees.*	0b
[2:1]	R/W	**CHROMA**	Chroma Format 0 : 420 1 : 422 2 : 444	
[0]	R/W	**START**	FC Start/FC Status	0b
Frame Size (FDC_FRAME_SIZE) ***Address : FDC_BASE + 0x0002***				
[15:8]	R/W	**MBY**	Maximum Macro block number in Y Direction	0
[7:0]	R/W	**MBX**	Maximum Macro block number in X Direction	0

Bit	R/W	Symbol	Description	Reset Value
Luminance Offset Register (FDC_LUMA_OFFSET) ***Address : FDC_BASE + 0x0004***				
[15:8]	R/W	**LUSO**	Screen offset	0
[7:4]	R/W	**LUYO**	Y offset	0
[3:0]	R/W	**LUXO**	X offset	0
Cb Offset Register (FDC_CB_OFFSET) ***Address* : FDC_BASE + 0x0006**				
[15:8]	R/W	**CBSO**	Screen offset	0
[7:4]	R/W	**CBYO**	Y offset	0
[3:0]	R/W	**CBXO**	X offset	0
Cr Offset Register (FDC_CR_OFFSET) ***Address* : FDC_BASE + 0x0008**				
[15:8]	R/W	**CRSO**	Screen offset	0
[7:4]	R/W	**CRYO**	Y offset	0
[3:0]	R/W	**CRXO**	X offset	0
Target Start Address (FDC_DST_BASE_L_L) ***Address* : FDC_BASE + 0x000a (FDC_DST_BASE_L)**				
[15:0]	R/W	**DBAL**	Destination Base Address	0b
Target Start Address (FDC_DST_BASE_H) ***Address* : FDC_BASE + 0x000c (FDC_DST_BASE_H)**				
[15:0]	R/W	**DBAL**	Destination Base Address	0b
Status Register (FDC_STATUS) ***Address* : FDC_BASE + 0x000e**				
[15]	R/W	**BSTEN**	Burst Enable (when wr_mode is 1)	1b
[14:8]	R	**Reserved**	-	-
[7]	R	**REQDI**	Request from Display	0
[6]	R	**REQSC**	Request from Scaler	0
[5]	R	**BFLD**	Bottom filed	0
[4:0]	R	**BUSY**	FC Status	0
Dering Control Register (FDC_DERING) ***Address* : FDC_BASE + 0x0010**				
[15:2]	R	**Reserved**	-	-
[1]	R	**FOE**	Filter Off Enable	0

Bit	R/W	Symbol	Description	Reset Value
[0]	R	**DREN**	Dering Enable	0
Occurrence Control Register (FDC_OCC_CNTL) ***Address*** **: FDC_BASE + 0x0010**				
[15:8]	R	**Reserved**	-	-
[7:0]	R/W	**OCCL**	Occurrence Control Level	0

TABLE 13-1. FRAME DIMENSION CONVERTER

13.3 SCALE PROCESSOR

13.3.1 Overview

The Scale Processor receives data with the Y/Cb/Cr format from the External Memory, the ISP, and the Frame Dimension Converter. In addition, it has the Buffer and the Scale functions. The Buffer function is used when it is connected to a real time ISP. The Scale function consists of the Pre-Scale and the Post-Scale functions. The Pre-Scale is the Coarse Scale without Filtering, and more than two times Down Scaling is exclusively possible. The Post-Scale is the Up/Down Scale with Filtering. The results of the Scale Processor are transferred to the External Memory or to the External Display Devices directly, without interface with the External Memory. The Scale Controller outputs after separating or mixing Y/Cb/Cr and the MPEG Encoder uses the separated Y/Cb/Cr. The separated Y/Cb/Cr format is 4:2:0 or 4:2:2. The Scale Processor has the Filter function that is a part of the Dering.

Features:

- 1350 x 3 bytes of the buffer function
- Coarse Scale and Fine Scale
- Separated Y/Cb/Cr 4:2:0 Format for MPEG Encoder
- Separated Y/Cb/Cr 4:2:2 Format for MPEG Encoder

Block Diagram

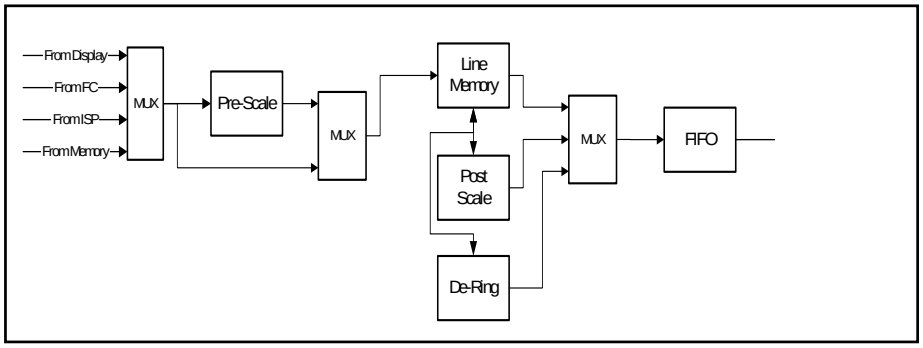


Figure 13-3. Scale Processor Diagra

13.3.2 Operation

13.3.2.1 Pre-Scale

The Pre-Scale is the Coarse Scale function using Data Skip or duplication, not a Filter. The Pre-Scale can choose Horizontal/Vertical Scale, but is fundamental to the Down Scale by powers of two. The Scale Factor of the Vertical Scale is subject to the input from the ISP or the External Memory. If the input is from the ISP, the Scale Factor uses SC_PRE_VRATIO. If, however, the input is from the External Memory, it uses SC_SRC_PXL_WIDTH. For example, in a case of four times of Vertical Scale Down, SC_SRC_PXL_WIDTH is set to a Source width X 4. The Horizontal Scale uses SC_PRE_HRATIO and SC_SRC_PXL_REQCNT is set to the Horizontal Width after the Pre-Scale.

Pre-Scale Ratio (SC_PRE_VRATIO)

Address : C000 1806h

Symbol	R/W	Bit	Description	Reset Value
SC_PRE_VRATIO	R/W	[15:0]	Vertical pre-scale ratio This bit is only valid when input source is ISP. Ratio should be more than 2 . SC_PRE_VRATIO = Ratio × (1024)	0x0400

TABLE 13-2. PRE-SCALE RATIO (SC_PRE_VRATIO)

Pre-Scale Ratio (SC_PRE_HRATIO)

Address : C000 1808h

Symbol	R/W	Bit	Description	Reset Value
SC_PRE_HRATIO	R/W	[15:0]	Horizontal Pre-scale ratio Ratio should be more than 2 . SC_PRE_HRATIO = Ratio × (1024)	0x0400

TABLE 13-3. PRE-SCALE RATIO (SC_PRE_HRATIO)

Pre-Scale Ratio (SC_SRC_PXL_WIDTH)

Address : C000 1820h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_PXL_WIDTH	R/W	[12:0]	Horizontal Source Pixel Width	0x140

TABLE 13-4. PRE-SCALE RATIO

Pre-Scale Ratio (SC_SRC_PXL_REQCNT)

Address : C000 1822h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_PXL_REQ CNT	R/W	[12:0]	When Pre-Scale mode, Horizontal Pixel width of Pre-scale output When not Pre-Scale mode, Horizontal Source Pixel size	0x140

TABLE 13-5. PRE-SCALE RATIO

13.3.2.2 Post-Scale

The Post-Scale is the Fine Scale function using a Filter. The Post Scale can choose Up/Down Scale in the Horizontal or the Vertical directions and has no limit for its multiplying power. If, however, the Width of Horizontal Source Data is more than 1350 pixels, the Post-Scale is executed after changing the Horizontal Width into 1350 pixels using the Pre-Scale. The Scale Factor of the Vertical Scale uses SC_POST_VRATIO, and the Scale Factor of the Horizontal Factor uses SC_POST_HRATIO.

Post-Scale Ratio (SC_POST_VRATIO)

Address : C000 180Ah
Address : C000 180Ch

Symbol	R/W	Bit	Description	Reset Value
SC_POST_VRATIOL	R/W	[15:0]	Vertical Post-Scale ratio (Low) SC_POST_VRATIO= Ratio × 0x4000	0x4000
SC_POST_VRATIOH	R/W	[15:0]	Vertical Post-Scale ratio (High)	0x0000

TABLE 13-6. POST-SCALE VRATIO

Post-Scale (SC_POST_HRATIO)

Address : C000 180Eh
Address : C000 1810h

Symbol	R/W	Bit	Description	Reset Value
SC_POST_HRATIOL	R/W	[15:0]	**Horizontal Post-Scale ratio (Low)** **SC_POST_HRATIO= Ratio × 0x4000**	0x4000
SC_POST_HRATIOH	R/W	[15:0]	**Horizontal Post-Scale ratio (High)**	0x0000

TABLE 13-7. POST-SCALE HRATIO

The Characteristics of the Filter are as follows:

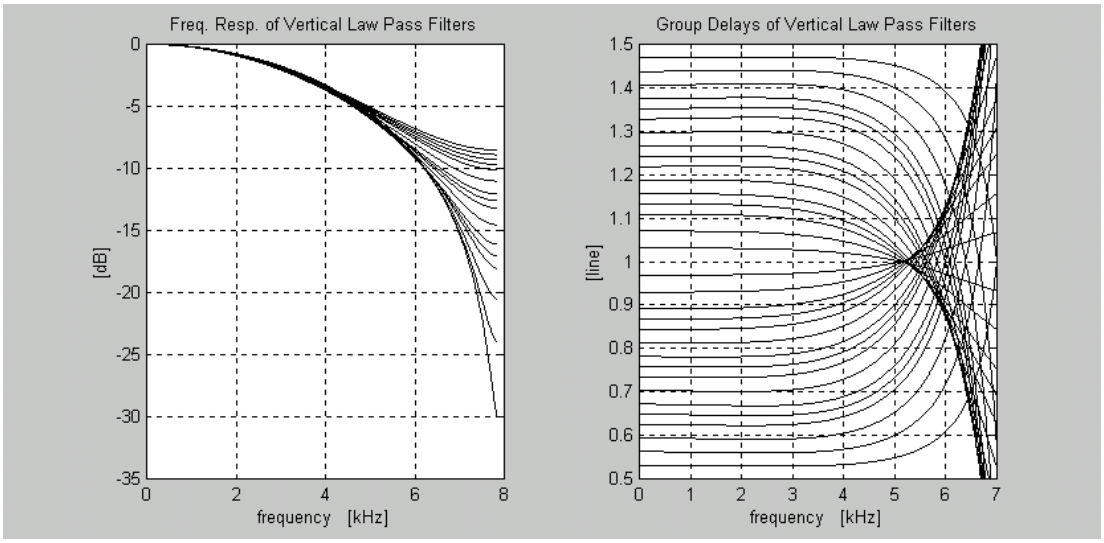


Figure 13-4. Characteristics of Digital Filter

13.3.2.3 Buffer Function

The Scale Block has a Buffer of 1350 x 3 bytes. This buffer is useful when it connects to the ISP in real time. In order to use this function, the Post Scale function must be 'Off'.

13.3.2.4 De-ring Function

The De-ring of the MMSP uses several Blocks, but has only the function to write to a Filter and a Memory in the Scale Block. In order to use this function, all Scale functions must be "Off".

13.3.2.5 Y/Cb/Cr Separating Function

The Data structure on the Memory of the MMSP exists as the linear Address form intergrating Y/Cb/Cr. Namely, Data[31:0] = {Cr,Y,Cb,Y}. However, the Y/Cb/ Cr must be separated for the MPEG Decoder or the JPEG Encoder. The separated Y/Cb/Cr is used to write Data on the Memory of the Scale Processor. In this case, the Horizontal Width must be in multiples of 32. If the desired Horizontal Width is 630 (32 x 19.6875), the 630 (32 x 19.6875) is once set on SC_DST_PXL_WIDTH.

Y/Cb/Cr Separation (SC_DST_PXL_WIDTH)

Address : C000 1826h

Symbol	R/W	Bit	Description	Reset Value
SC_DST_PXL_WIDTH	R/W	[12:0]	Horizontal Destination Pixel Width. SC_DST_PXL_WIDTH = SC_SRC_PXL_WIDTH / H-Ratio. This bit must be an even number.	0x140

TABLE 13-8. Y/CB/CR SEPARATION FUNCTION

Y/Cb/Cr Separation (SC_DST_WPXL_WIDTH)

Address : C000 1828h

Symbol	R/W	Bit	Description	Reset Value
SC_DST_WPXL_WIDTH	R/W	[12:0]	Horizontal Wide Destination Pixel Width. This bit must be an even number.	0x140

TABLE 13-9. Y/CB/CR SEPARATION FUNCTION

13.3.2.6 Mirror Function

The Scale Processor has the function to mirror Source or Destination Data in the Horizontal or the Vertical directions of the MMSP. That is, it mirrors when it reads Data or writes to the External memory. It can Mirror only the Memory Interface.

Status Register (SC_MIRROR)

Address : C000 1804h

Symbol	R/W	Bit	Description	Reset Value
Reserved	R/W	[15:6]		0
SC_DATA_FMT	R/W	[5:4]	Scale Source Data Format 0: YUY2 (DATA[31:0] = {V0, Y1, U0, Y0 }) 1: YVYU (DATA[31:0] = { U0, Y1, V0, Y0 }) 2: UYVY (DATA[31:0] = { Y1, V0, Y0, U0}) 3: VYUY (DATA[31:0] = { Y1, U0, Y0, V0})	0
SC_DST_VMRR	R/W	[3]	Vertical Mirror of Destination Data 0: Disable 1: Mirror	0
SC_DST_HMRR	R/W	[2]	Horizontal Mirror of Destination Data 0: Disable 1: Mirror	0
SC_SRC_VMRR	R/W	[1]	Vertical Mirror of Source Data 0: Disable 1: Mirror	0
SC_SRC_HMRR	R/W	[0]	Horizontal Mirror of Source Data 0: Disable 1: Mirror	0

TABLE 13-10. STATUS REGISTER(SC_MIRROR)

13.3.2.7 Field/ Frame Function

The Scale Processor can read or write a Field Picture and a Frame Picture. It distinguishes between an Odd Field and an Even Field by means of the Field Signal of the ISP when it receives Data from the ISP. In addition, when it sends Data to the Multi Layer Controller, it distinguishes between an Odd Field and an Even Field by means of the Field Signal of the Display Controller. If it brings Data from an External Memory, it brings the Data after setting its Odd/Even Address. In case of Frame Processing, the values of the Odd/Even Address may be made the same. The ways to write Data on an External Memory are different between Field Mode and Frame Mode. The SC_FIELD Register determines the modes. In the Odd Field of the Frame Mode, it writes every Horizontal Line from the address specified by SC_DST_ADDR skipping one line by one line. For the Even Field, it writes skipping one line by one line from the address where the Horizontal Width is added to SC_DST_ADDR. In the Frame Mode, it writes Data consecutively.

Source / Destination Address Starting Point (SC_SRC_ ADDR/ SC_DST_ADDR)

Address : C000 1812h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_ODD_ADDR L	R/W	[15:0]	Source Address Starting point of Odd Field (Low bits)	0x0000

TABLE 13-11. SOURCE / DESTINATION ADDRESS STARTING POINT

Address : C000 1814h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_ODD_ADDR H	R/W	[15:0]	Source Address Starting point of Odd Field (High bits)	0x0000

TABLE 13-12. SOURCE / DESTINATION ADDRESS STARTING POINT

Address : C000 1816h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_EVEN_ADD RL	R/W	[15:0]	Source Address Starting point of Even Field (Low bits)	0x0000

TABLE 13-13. SOURCE / DESTINATION ADDRESS STARTING POINT

Address : C000 1818h

Symbol	R/W	Bit	Description	Reset Value
SC_SRC_ EVEN _ADDRH	R/W	[15:0]	Source Address Starting point of Even Field (High bits)	0x0000

TABLE 13-14. SOURCE / DESTINATION ADDRESS STARTING POINT

Address : C000 181Ah

Symbol	R/W	Bit	Description	Reset Value
SC_DST_ADDRL	R/W	[15:0]	Destination Address Starting point of Odd Field (Low bits)	0x0000

TABLE 13-15. SOURCE / DESTINATION ADDRESS STARTING POINT

TABLE 13-16. SOURCE / DESTINATION ADDRESS STARTING POINT

Address : C000 181Ch

Status Register (SC_STATUS)

Address : C000 1802h

Symbol	R/W	Bit	Description	Reset Value
Reserved	R/W	[15:13]		
Reserved	R/W	[12:11]		0
SC_FIELD	R/W	[10]	Frame or Field Operation when Scale Processor writes data to external memory 0: Frame Mode 1: Field Mode	0
SC_FIELD_POL	R/W	[9]	Polarity of Field Signal coming from ISP/DISPLAY 0: Memory 1: Inversion	0
SC_ISP_FIELD	R	[8]	Field Status of ISP	0
SC_DISP_FIELD	R	[7]	Field Status of Display Controller	0
Reserved		[6:4]		0
SC_BUSY	R	[3]	Scale Busy Status 0: Idle 1: Busy	0
SC_DONE	R	[2]	Scale Done Status 0: Active 1: Done	0
Reserved		[1:0]		

TABLE 13-17. STATUS REGISTER (SC_STATUS)

13.3.2.8 Scale Processor Paths by Function

The Scale Processor receives Data from the ISP, External Memory, Frame Dimension Converter, and Multi Layer Controller. It buffers and scales these data, and then transfers them to the External Memory and the Multi Layer Controller. Operations by Data Path are listed in the following table:

Input	Pre-Scale (down)	Post-Scale (up/down)	Operation	Output Data Type (Integrated Data = {Y,Cb,Y,Cr} Separated Data = Y/Cb/Cr Separation)
Ext Memory	ON / OFF	ON / OFF	1 Frame	Display= **Integrated** Data Memory = **Integrated** Data/ Separated Data
Frame Dimension Converter	OFF	ON / OFF	1 Frame or stop command	Display= **Integrated** Data Memory **= Integrated** Data
Frame Dimension Converter For De-ring	OFF	OFF	1 Frame	Memory = **Integrated** Data
ISP	ON / OFF	ON / OFF	1 Frame or stop command	Memory = **Integrated** Data/ **Separated** Data
Multi Layer Controller	OFF	ON / OFF	1 Frame or stop command	Display= **Integrated** Data Memory = **Integrated** Data/ **Separated** Data

TABLE 13-18. SCALE PROCESSOR PATHS BY FUNCTION

13.3.3 SCALE PROCESS REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
Scale Control Register (SC_CMD) ***Address : C000 1800h***				
[15]	R/W	**SC_DERING**	De-Ring Filter Enable in Scale Processor	0
[14]	R/W	**SC_START**	Start Signal (1 : Start)	0
[13]	R/W	**SC_ENABLE**	Scale Processor Enable Signal	0
[12]	R/W	**SC_FROM_FMT**	Source of Scale Processor 0 : Memory 1 : Format Converter	0
[11]	R/W	**SC_FROM_ISP**	Source of Scale Processor 0 : Memory 1 : Image Signal Processor	0
[10]	R/W	**SC_FROM_DISP**	Source of Scale Processor 0 : Memory 1 : Display Processor	0
[9]	R/W	**Reserved**	-	-
[8]	R/W	**SC_ONE_TIME**	The number of Scaling and buffering per Frame 0 : Forever 1 : One times	0
[7]	R/W	**SC_PRESCLE**	Pre- Scaling Down Enable Signal Pre- Scaling is Down Scale and don't use filter. 0 : Disable 1 : Enable	0
[6]	R/W	**SC_POSTSCLE**	Post-Scaling Enable Signal Post- Scaling is Up/Down scaling and use Filter. 0 : Disable 1 : Enable	0
[5]	R/W	**SC_POSTVSCLE**	Scale Down or Scale up in the vertical direction 0 : Scale Down 1 : Scale UP	0
[4]	R/W	**SC_POSTHSCLE**	Scale Down or Scale up in the horizontal direction 0 : Scale Down 1 : Scale UP	0
[3]	R/W	**SC_F422**	Separated Writing Format(Y/Cb/Cr) 0 : 4:2:0 1 : 4:2:2	0
[2]	R/W	**SC_DEST_MEM**	Destination is external Memory 0 : Disable 1 : Enable	0
[1]	R/W	**SC_DEST_DISP**	Destination is Display. 0 : Disable 1 : Enable	0
[0]	R/W	**SC_WR_TYPE**	Write Data (Y/Cb/Cr) separately 0: Data[31:0]={Cr, Y, Cb, Y} 1: Separated Data (Y/Cb/Cr)	0

Bit	R/W	Symbol	Description	Reset Value
Scale Status Register (SC_STATUS) ***Address : C000 1802h***				
[15:13]	R/W	**Reserved**	-	-
[12:11]	R/W	**Reserved**	-	-
[10]	R/W	**SC_FIELD**	Frame or Field Operation when Scale Processor writes data to external memory 0 : Frame Mode 1 : Field Mode	0
[9]	R/W	**SC_FIELD_POL**	Field Signal polarity out of the ISP/Display 0 : Memory 1 : Inversion	0
[8]	R	**SC_ISP_FIELD**	Field Status of ISP	0
[7]	R	**SC_DISP_FIELD**	Field Status of Multi Layer Controller	0
[6:4]		**Reserved**	-	-
[3]	R	**SC_BUSY**	Scaling Busy Status 0 : Idle 1 : Busy	0
[2]	R	**SC_DONE**	Scaling Done Status 0 : Active 1 : Done	0
[1:0]		**Reserved**	-	-
Mirror Register (SC_MIRROR) ***Address : C000 1804h***				
[15:6]	R/W	**Reserved**	-	-
[5:4]	R/W	**SC_DATA_FMT**	Scale Source Data Format 0: YUY2 (DATA[31:0] = {V0, Y1, U0, Y0 }) 1: YVYU (DATA[31:0] = { U0, Y1, V0, Y0 }) 2: UYVY (DATA[31:0] = { Y1, V0, Y0, U0}) 3: VYUY (DATA[31:0] = { Y1, U0, Y0, V0})	0
[3]	R/W	**SC_DST_VMRR**	Vertical Mirror of Destination Data 0 : Disable 1 : Mirror	0
[2]	R/W	**SC_DST_HMRR**	Horizontal Mirror of Destination Data 0 : Disable 1 : Mirror	0
[1]	R/W	**SC_SRC_VMRR**	Vertical Mirror of Source Data 0 : Disable 1 : Mirror	0
[0]	R/W	**SC_SRC_HMRR**	Horizontal Mirror of Source Data 0 : Disable 1 : Mirror	0

Bit	R/W	Symbol	Description	Reset Value
Pre-Scale Ratio (SC_PRE_RATIO) ***Address : C000 1806h***				
[15:0]	R/W	**SC_PRE_VRATIO**	Vertical pre-scale ratio. This bit is only valid when input source is ISP. Ratio should be more than 2. SC_PRE_VRATIO = Ratio × (1024)	0x0400
Address : C000 1808h				
[15:0]	R/W	**SC_PRE_HRATIO**	Horizontal Pre-scale ratio. Ratio should be more than 2. SC_PRE_HRATIO = Ratio × (1024)	0x0400
Post-Scale Ratio (SC_POST_RATIO) ***Address : C000 180Ah*** ***Address : C000 180Ch***				
[15:0]	R/W	**SC_POST_VRATIOL**	Vertical Post-Scaling ratio (Low) SC_POST_VRATIO= Ratio × 0x4000	0x4000
[15:0]	R/W	**SC_POST_VRATIOH**	Vertical Post-Scaling ratio (High)	0x0000
Address : C000 180Eh ***Address : C000 1810h***				
[15:0]	R/W	**SC_POST_HRATIOL**	Horizontal Post-Scaling ratio (Low) SC_POST_HRATIO= Ratio × 0x4000	0x4000
[15:0]	R/W	**SC_POST_HRATIOH**	Horizontal Post-Scaling ratio (High)	0x0000
Source / Destination Address Starting Point (SC_SRC_ ADDR/ SC_DST_ADDR) ***Address : C000 1812h***				
[15:0]	R/W	**SC_SRC_ODD_ADDRL**	Source Address Starting point of Odd Field (Low bits)	0x0000
Address : C000 1814h				
[15:0]	R/W	**SC_SRC_ODD_ADDRH**	Source Address Starting point of Odd Field (High bits)	0x0000
Address : C000 1816h				
[15:0]	R/W	**SC_SRC_EVEN_ADDRL**	Source Address Starting point of Even Field (Low bits)	0x0000
Address : C000 1818h				
[15:0]	R/W	**SC_SRC_ EVEN _ADDRH**	Source Address Starting point of Even Field (High bits)	0x0000
Address : C000 181Ah				
[15:0]	R/W	**SC_DST_ADDRL**	Destination Address Starting point of Odd Field (Low bits)	0x0000
Address : C000 181Ch				
[15:0]	R/W	**SC_DST_ADDRH**	Destination Address Starting point of Odd Field (High bits)	0x0000

Bit	R/W	Symbol	Description	Reset Value
Pixel Size (SC_PIX_SIZE) ***Address : C000 181Eh***				
[11:0]	R/W	**SC_SRC_PXL_HEIGHT**	Vertical Source Pixel Height	0xF0
Address : C000 1820h				
[12:0]	R/W	**SC_SRC_PXL_WIDTH**	Horizontal Source Pixel Width	0x140
Address : C000 1822h				
[12:0]	R/W	**SC_SRC_PXL_REQCNT**	When Pre-Scale Mode, Horizontal Pixel width of Pre-scale output When No pre-scale mode, Horizontal Source Pixel size	0x140
Address : C000 1824h				
[11:0]	R/W	**SC_DST_PXL_HEIGHT**	Vertical Destination Pixel Height SC_DST_PXL_HEIGHT = SC_SRC_PXL_HEIGHT / V-Ratio	0x140
Address : C000 1826h				
[12:0]	R/W	**SC_DST_PXL_WIDTH**	Horizontal Destination Pixel Width. SC_DST_PXL_WIDTH = SC_SRC_PXL_WIDTH / H-Ratio. This bit must be an even number.	0x140
Address : C000 1828h				
[12:0]	R/W	**SC_DST_WPXL_WIDTH**	Horizontal Wide Destination Pixel Width. This bit must be an even number.	0x140
Two Dimensional Destination Address of Luminance and Chrominance (SC_SEP_ADDR) ***Address : C000 1828h***				
[15:8]	R/W	**SC_LUMA_BASE_OFFSET**	Luminance Base Offset	0x00
[7:4]	R/W	**SC_LUMA_Y_OFFSET**	Vertical Luminance Offset	0x00
[3:0]	R/W	**SC_LUMA_X_OFFSET**	Horizontal Luminance Offset	0x00
Address : C000 182Ah				
[15:8]	R/W	**SC_CB_BASE_OFFSET**	Cb Base Offset	0x00
[7:4]	R/W	**SC_CB_Y_OFFSET**	Vertical Cb Offset	0x00
[3:0]	R/W	**SC_CB_X_OFFSET**	Horizontal Cb Offset	0x00
Address : C000 182Ch				
[15:8]	R/W	**SC_CR_BASE_OFFSET**	Cr Base Offset	0x00
[7:4]	R/W	**SC_CR_Y_OFFSET**	Vertical Cr Offset	0x00
[3:0]	R/W	**SC_CR_X_OFFSET**	Horizontal Cr Offset	0x00

Bit	R/W	Symbol	Description	Reset Value
Luminance and Chrominance Path Delay (SC_DELAY) ***Address : C000 182Eh***				
[7:4]	R/W	**LUMA_DELAY**	Pipe Line Delay Control in the Luminance Path	0x7
[3:0]	R/W	**CHOMA_DELAY**	Pipe Line Delay Control in the Chrominance Path	0x3
Memory Control (SC_MEM_CNTR) ***Address : C000 1830h***				
[15]	R/W	**SC_BRST_OFF**	Memory Burst Mode Disable 0 : Burst Mode 1 : Non Burst Mode	0x0
[14:8]	R/W	**Reserved**	-	-
[7:5]	R/W	**Reserved**	-	-
[4:0]	R/W	**SC_MEM_RD_SZ**	Memory Read Request Size by word 8 ~ 16 word / (one request)	0x10
Interrupt Control (SC_IRQ) ***Address : C000 1834h***				
[3]	W/R	**SC_IRQ_EN**	Interrupt Control of Scale Processor 0 : Disable 1 : Enable	0
[2]	W/R	**SC_IRQ_CLEAR**	Scale Interrupt Status and Clear bits. This bit is set after one frame is scaled. This bit is clear after this bit is written. 0 : No Interrupt pending 1 : Interrupt pending	0
[1]	W/R	**FC_IRQ_EN**	Interrupt Control of Frame Dimension Converter 0 : Disable 1 : Enable	0
[0]	W/R	**FC_IRQ_CLEAR**	Scale Interrupt Status and Clear bits. This bit is set after one frame is scaled. This bit is clear after the bit is written. 0 : No Interrupt pending 1 : Interrupt pending	0
Reserved () ***Address : C000 1836h***				
	HW	**Reserved**	-	0x2330

TABLE 13-19. SCALE PROCESSOR REGISTERS LIST

13.4 MULTI LAYER CONTROLLOR

13.4.1 Overview

The Multi Layer Controller receives data from the Scale Block, Frame Dimension Converter, and the External Memory. The Data Format for the Multi Layer Controller is the Y/Cb/Cr, the RGB, the Indexed Color, the OSD and the Sub-picture or Cursor Data Format. The Multi Layer Controller takes Visual effect by means of the Alpha blending and the Color Key functions and has the Mirroring function for the 4-division display of Y/Cb/Cr Data. It enhances the image quality of Luminance Data by means of Contrast, Brightness, and enhances Chrominance Data by means of Hue and Saturation. The Color Space Converter transforms Y/Cb/Cr Data into RGB Data. In addition, The Multi Layer Controller enhances the image quality of RGB Data by means of Dithering and Gamma correction. It Scales Up/Down the Y/Cb/Cr, the RGB, and the Indexed Color Formats. The Scaling about the OSD and the Sub-Picture is performed by the Scale Processor.

Features:

- Various Data Input Paths
  - Scale Processor
  - Frame Dimension Converter to transform the separated Y/Cb/Cr data into the {Y, Cb, Y, Cr} format
  - Memory Control Unit to bring Data directly into the Memory
- Treatment of Y/Cb/Cr, RGB, Indexed Data, OSD, Sub-picture, and H/W Cursor Data
- Alpha Blending and Color Key
- Scaling, Mirroring, and 4-divided Display On/Off functions for the Y/Cb/Cr Format
- Coarse Scale and 5-region Display On/Off functions for RGB and Indexed Data
- OSD of 2/4/8 BPP and Compressed Data
- Image enhancement via Contrast, Brightness, Hue, Saturation, Dithering, and Gamma correction
- Interface with the Scale Processor for the OSD and the Sub-Picture

Block Diagram

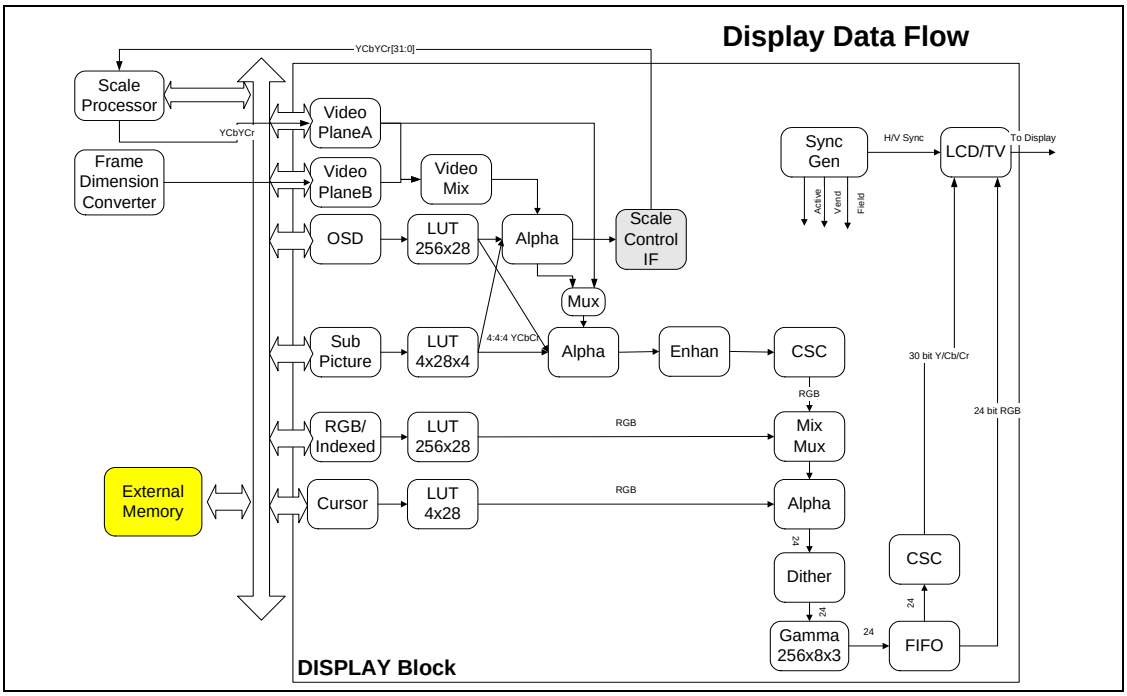


Figure 13-5. Multi Layer Controller Block Diagram

13.4.2 Operation

13.4.2.1 YUV Layer (Y/Cb/CR)

The YUV Layer can handle only Y/Cb/Cr Data format. This Block has Scale, Mirrors, and 4-division Display functions and receives Data from the Scale Processor, the Frame Dimension Converter, and the External Memory. The YUV Layer is divided into Region A and Region B, and each Region is divided into Top Region and Bottom Region. Region A and Region B receive Data from External Memory/Scale Processor and External Memory/Frame Dimension Converter respectively. The YUV Layer also has 4-division function. Each divided region has its own Address, so it displays different Data from each other. In addition, each region has its own Scale and Mirror functions. If Region A and Region B of the YUV Layer are overlapped, the Mux function has one Data displayed by selecting the Data.

The Y/CbCr format is as follows:

Pixel Data	Cr0[7:0]	Y1[7:0]	Cb0[7:0]	Y0[7:0]
32bits Data	D[31:24]	D[23:16]	D[15:8]	D[7:0]
Memory Address	N + 3	N + 2	N + 1	N + 0

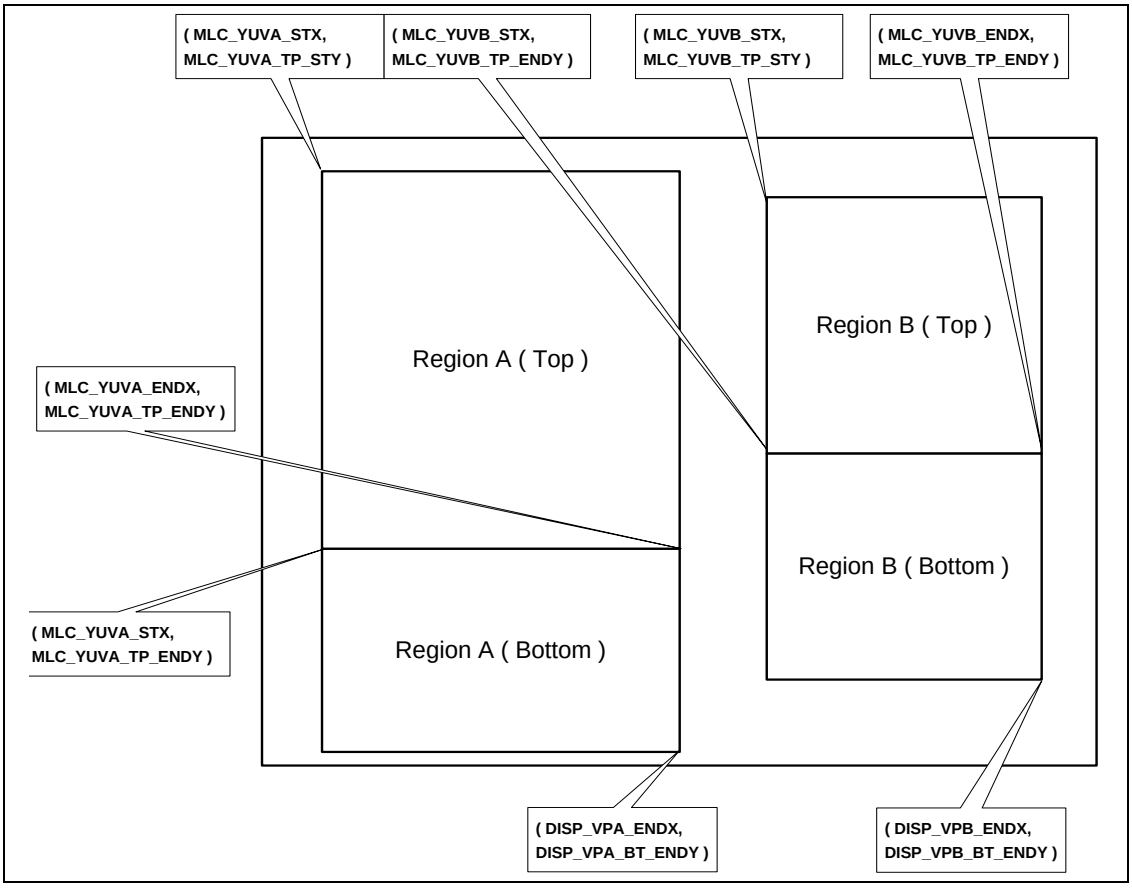


Figure 13-6. 4-Division of YUV Layer

The Registers related to the setting of he YUV Layer are listed below:

4 Division Display				
	Region A (Top)	Region A (Bottom)	Region B (Top)	Region B (Bottom)
Region Selection	MLC_YUVA_ON<=1 MLC_YUVA_BT <=0	MLC_YUVA_ON<=1 MLC_YUVA_BT <=1	MLC_YUVB_ON <=1 MLC_YUVB_BT <=0	MLC_YUVB_ON <=1 MLC_YUVB_BT <=1
DRAM Address	MLC_YUVA_TP_OADR MLC_YUVA_TP_EADR	MLC_YUVA_BT_OADR MLC_YUVA_BT_EADR	MLC_YUVB_TP_OADR MLC_YUVB_TP_EADR	MLC_YUVB_BT_OADR MLC_YUVB_BT_EADR
coordinate	MLC_YUVA_STX MLC_YUVA_ENDX MLC_YUVA_TP_STY MLC_YUVA_TP_ENDY	MLC_YUVA_STX MLC_YUVA_ENDX MLC_YUVA_TP_ENDY MLC_YUVA_BT_ENDY	MLC_YUVB_STX MLC_YUVB_ENDX MLC_YUVB_TP_STY MLC_YUVB_TP_ENDY	MLC_YUVB_STX MLC_YUVB_ENDX MLC_YUVB_TP_ENDY MLC_YUVB_BT_ENDY
Source Image Pixel Width	MLC_YUVA_TP_PXW	MLC_YUVA_BT_PXW	MLC_YUVB_TP_PXW	MLC_YUVB_BT_PXW
Scale				
	Region A (Top)	Region A (Bottom)	Region B (Top)	Region B (Bottom)
Horizontal Scale Factor	MLC_YUVA_TP_HSC	MLC_YUVA_BT_HSC	MLC_YUVB_TP_HSC	MLC_YUVB_BT_HSC
Vertical Scale Factor	MLC_YUVA_TP_VSC	MLC_YUVA_BT_VSC	MLC_YUVB_TP_VSC	MLC_YUVB_BT_VSC
Mirror				
	Region A (Top)	Region A (Bottom)	Region B (Top)	Region B (Bottom)
Horizontal Mirror	MLC_YUVA_TP_MR_H	MLC_YUVA_BT_MR_H	MLC_YUVB_TP_MR_H	MLC_YUVB_BT_MR_H
Vertical Mirror	MLC_YUVA_TP_MR_V	MLC_YUVA_BT_MR_V	MLC_YUVB_TP_MR_V	MLC_YUVB_BT_MR_V
Input Data Path				
	Region A (Top)	Region A (Bottom)	Region B (Top)	Region B (Bottom)
From Scale Processor or Frame Dimension Converter	MLC_SC2DP_A = 1	MLC_SC2DP_A = 1	MLC_FC2DP_B = 1	MLC_FC2DP_B = 1
From DRAM	MLC_SC2DP_A = 0	MLC_SC2DP_A = 0	MLC_FC2DP_B = 0	MLC_FC2DP_B = 0
Priority (Region A and Region B)				
	MLC_YUV_PRIO			

TABLE 13-20. YUV LAYER LIST

Effect of Video Image (MLC_YUV_EFECT)

Address : C000 2882h

Bit	R/W	MLC_VL_EFECT	Description	Reset Value
[9]	R/W	**MLC_VLB_BT**	Divide Region B of Video (Y/Cb/Cr) Layer with Top and Bottom Region. 0 : Disable 1 : Enable	0x0
[8]	R/W	**MLC_VLB_TP_MR_H**	Horizontal Mirror of Top Region B at Video (Y/Cb/Cr) Layer.	0x0
[7]	R/W	**MLC_VLB_TP_MR_V**	Vertical Mirror of Top Region B at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[6]	R/W	**MLC_VLB_BT_MR_H**	Horizontal Mirror of Bottom Region B at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[5]	R/W	**MLC_VLB_BT_MR_V**	Vertical Mirror of Bottom Region B at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[4]	R/W	**MLC_VLA_BT**	Divide Region A of Video (Y/Cb/Cr) Layer with Top and Bottom Region. 0 : Disable 1 : Enable	0x0
[3]	R/W	**MLC_VLA_TP_MR_H**	Horizontal Mirror of Top Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[2]	R/W	**MLC_VLA_TP_MR_V**	Vertical Mirror of Top Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[1]	R/W	**MLC_VLA_BT_MR_H**	Horizontal Mirror of Bottom Region A at Video(Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[0]	R/W	**MLC_VLA_BT_MR_V**	Vertical Mirror of Bottom Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0

TABLE 13-21. EFFECT OF VIDEO IMAGE (MLC_YUV_EFECT)

Video Image Control Register (MLC_YUV_CNTL)

Address : C000 2884h

Bit	R/W	MLC_VL_CNTL	Description	Reset Value
[13]	R/W	**MLC_VLA_ALP1SKP**	Skip Alpha Blending of Video (Y/Cb/Cr) Layer Region A. When MLClay to Scale Processor and Scale Processor to Display Mode, this bit should be skipped. 0 : No Skip 1 : Skip	0x0
[12]	R/W	**MLC_SC2DP_A**	Input Data Path of Video (Y/Cb/Cr) Layer Region A. 0 : External Memory 1 : Scale Processor	0x0
Bit	**R/W**	**MLC_VL_CNTL**	**Description**	**Reset Value**
[11]	R/W	**MLC_FDC2DP_B**	Input Data Path of Video (Y/Cb/Cr) Layer Region B.	0x0

			0 : External Memory 1 : Frame Dimension Converter	
[10]	R/W	**MLC_VL_PRIO**	Priority of Region A and Region B at Video (Y/Cb/Cr) Layer. 0 : Region A 1 : Region B	0x0
[9:0]		**Reserved**		

TABLE 13-22. VIDEO IMAGE CONTROL REGISTER (MLC_YUV_CNTL)

Scale Factor Register of Region A (MLC_YUVA_TP_HSC)

Address : C000 2886h

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**MLC_VLA_TP_HSC**	Horizontal Scale Factor of Top Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_TP_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

TABLE 13-23. SCALE FACTOR REGISTER OF REGION A (MLC_YUVA_TP_HSC)

Scale Factor Register of Region A (MLC_YUVA_BT_HSC)

Address : C000 2888h

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**MLC_VLA_BT_HSC**	Horizontal Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer MLC_VLA_BT_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

TABLE 13-24. SCALE FACTOR REGISTER OF REGION A (MLC_YUVA_BT_HSC)

Scale Factor Register of Region A (MLC_YUVA_TP_HSCL, MLC_YUVA_TP_HSCH)

Address : C000 288Ah

Address : C000 288Ch

Bit	R/W	Symbol	Description	Reset Value
[24:0]	R/W	**MLC_VLA_TP_VSC**	Vertical Scale Factor of Top Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_TP_VSC = Ratio x MLC_VLA_TP_PXW Scale Down = Ratio > 1	00

TABLE 13-25. SCALE FACTOR REGISTER OF REGION A (MLC_YUVA_TP_HSCL, MLC_YUVA_TP_HSCH)

Scale Factor Register of Region A (MLC_YUVA_BT_HSCL, MLC_YUVA_BT_HSCH)

Address : C000 288Eh

Address : C000 2890h

Bit	R/W	Symbol	Description	Reset Value
[24:0]	R/W	MLC_VLA_BT_VSC	Vertical Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_BT_VSC = Ratio x MLC_VLA_BT_PXW Scale Down = Ratio > 1	00

TABLE 13-26. SCALE FACTOR REGISTER OF REGION A (MLC_YUVA_BT_HSCL, MLC_YUVA_BT_HSCH)

Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW)

Address : C000 2892h

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**MLC_VLA_TP_PXW**	Horizontal Pixel Width of Top Region A at Video (Y/Cb/Cr) Layer.	00

TABLE 13-27. HORIZONTAL PIXEL WIDTH REGISTER OF REGION A (MLC_YUVA_TP_PXW)

Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW)

Address : C000 2894h

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**MLC_VLA_BT_PXW**	Horizontal Pixel Width of Bottom Region A at Video (Y/Cb/Cr) Layer.	00

TABLE 13-28. HORIZONTAL PIXEL WIDTH REGISTER OF REGION A (MLC_YUVA_TP_PXW)

Coordinate Register of Region A (MLC_YUVA_STX)

Address : C000 2896h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLA_STX**	Horizontal Starting Point of Top/Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-29. COORDINATE REGISTER OF REGION A (MLC_YUVA_STX)

Coordinate Register of Region A (MLC_YUVA_ENDX)

Address : C000 2898h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLA_ENDX**	Horizontal Ending Point of Top/Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-30. COORDINATE REGISTER OF REGION A (MLC_YUVA_ENDX)

Coordinate Register of Region A (MLC_YUVA_TP_STY)

Address : C000 289Ah

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLA_TP_STY**	Vertical Starting Point of Top Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-31. COORDINATE REGISTER OF REGION A (MLC_YUVA_TP_STY)

Coordinate Register of Region A (MLC_YUVA_TP_ENDY)

Address : C000 289Ch

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLA_TP_ENDY**	Vertical Ending Point of Top Region A and Vertical Starting Point of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-32. COORDINATE REGISTER OF REGION A (MLC_YUVA_TP_ENDY)

Coordinate Register of Region A (MLC_YUVA_BT_ENDY)

Address : C000 289Eh

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLA_BT_ENDY**	Vertical Ending Point of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-33. COORDINATE REGISTER OF REGION A (MLC_YUVA_BT_ENDY)

Source Address of Region A (MLC_YUVA_TP_OADRL, MLC_YUVA_TP_OADRH)

Address : C000 28A0h

Address : C000 28A2h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLA_TP_OADR**	Source and Odd Field Address of Top Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-34. SOURCE ADDRESS OF REGION A (MLC_YUVA_TP_OADRL, MLC_YUVA_TP_OADRH)

Source Address of Region A (MLC_YUVA_TP_EADRL, MLC_YUVA_TP_EADRH)

Address : C000 28A4h

Address : C000 28A6h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLA_TP_EADR**	Source and Even Field Address of Top Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-35. SOURCE ADDRESS OF REGION A (MLC_YUVA_TP_EADRL, MLC_YUVA_TP_EADRH)

Source Address of Region A (MLC_YUVA_BT_OADRL, MLC_YUVA_BT_OADRH)

Address : C000 28A8h

Address : C000 28Aah

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLA_BT_OADR**	Source and Odd Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-36. SOURCE ADDRESS OF REGION A (MLC_YUVA_BT_OADRL, MLC_YUVA_BT_OADRH)

Source Address of Region A (MLC_YUVA_BT_EADRL, MLC_YUVA_BT_EADRH)

Address : C000 28ACh

Address : C000 28Aeh

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLA_BT_EADR**	Source and Even Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-37. SOURCE ADDRESS OF REGION A (MLC_YUVA_BT_EADRL, MLC_YUVA_BT_EADRH)

Scale Factor Register of Region B (MLC_YUVB_TP_HSC)

Address : C000 28B0h

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**MLC_VLB_TP_HSC**	Horizontal Scale Factor of Top Region B at Video (Y/Cb/Cr) Layer. MLC_VLB_TP_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

TABLE 13-38. SCALE FACTOR REGISTER OF REGION B (MLC_YUVB_TP_HSC)

Scale Factor Register of Region B (MLC_YUVB_BT_HSC)

Address : C000 28B2h

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**MLC_VLB_BT_HSC**	Horizontal Scale Factor of Bottom Region B at Video (Y/Cb/Cr) Layer. MLC_VLB_BT_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

TABLE 13-39. SCALE FACTOR REGISTER OF REGION B (MLC_YUVB_BT_HSC)

Scale Factor Register of Region B (MLC_YUVB_TP_VSCL, MLC_YUVB_TP_VSCH)

Address : C000 28B4h

Address : C000 28B6h

Bit	R/W	Symbol	Description	Reset Value
[24:0]	R/W	**MLC_VLB_TP_VSC**	Vertical Scale Factor of Top Region B at Video (Y/Cb/Cr) Layer. MLC_VLB_TP_VSC = Ratio x MLC_VLB_TP_PXW Scale Down = Ratio > 1	00

TABLE 13-40. SCALE FACTOR REGISTER OF REGION B (MLC_YUVB_TP_VSCL, MLC_YUVB_TP_VSCH)

Scale Factor Register of Region B (MLC_YUVB_BT_VSCL, MLC_YUVB_BT_VSCH)

Address : C000 28B8h

Address : C000 28Bah

Bit	R/W	Symbol	Description	Reset Value
[24:0]	R/W	**MLC_VLB_BT_VSC**	Vertical Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer. MLC_VLB_BT_VSC = Ratio x MLC_VLB_BT_PXW Scale Down = Ratio > 1	00

TABLE 13-41. SCALE FACTOR REGISTER OF REGION B (MLC_YUVB_BT_VSCL, MLC_YUVB_BT_VSCH)

Horizontal Pixel Width Register of Region B(MLC_YUVB_TP_PXW)

Address : C000 28BCh

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**MLC_VLB_TP_PXW**	Horizontal Pixel Width of Top Region B at Video (Y/Cb/Cr) Layer.	00

TABLE 13-42. HORIZONTAL PIXEL WIDTH REGISTER OF REGION B(MLC_YUVB_TP_PXW)

Horizontal Pixel Width Register of Region B(MLC_YUVB_BT_PXW)

Address : C000 28Beh

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**MLC_VLB_BT_PXW**	Horizontal Pixel Width of Bottom Region B at Video (Y/Cb/Cr) Layer.	00

TABLE 13-43. HORIZONTAL PIXEL WIDTH REGISTER OF REGION B(MLC_YUVB_BT_PXW)

Coordinate Register of Region B (MLC_YUVB_STX)

Address : C000 28C0h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLB_STX**	Horizontal Starting Point of Top/Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-44. COORDINATE REGISTER OF REGION B (MLC_YUVB_STX)

Coordinate Register of Region B (MLC_YUVB_ENDX)

Address : C000 28C2h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLB_ENDX**	Horizontal Ending Point of Top/Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-45. COORDINATE REGISTER OF REGION B (MLC_YUVB_ENDX)

Coordinate Register of Region B (MLC_YUVB_TP_STY)

Address : C000 28C4h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLB_TP_STY**	Vertical Starting Point of Top Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-46. COORDINATE REGISTER OF REGION B (MLC_YUVB_TP_STY)

Coordinate Register of Region B (MLC_YUVB_TP_ENDY)

Address : C000 28C6h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLB_TP_ENDY**	Vertical Ending Point of Top Region A and Vertical Starting Point of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-47. COORDINATE REGISTER OF REGION B (MLC_YUVB_TP_ENDY)

Coordinate Register of Region B (MLC_YUVB_BT_ENDY)

Address : C000 28C8h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_VLB_BT_ENDY**	Vertical Ending Point of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-48. COORDINATE REGISTER OF REGION B (MLC_YUVB_BT_ENDY)

Source Address of Region B(MLC_YUVB_TP_OADR)

Address : C000 28CAh

Address : C000 28CCh

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLB_TP_OADR**	Source and Odd Field Address of Top Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-49. SOURCE ADDRESS OF REGION B(MLC_YUVB_TP_OADR)

Source Address of Region B(MLC_YUVB_TP_EADR)

Address : C000 28CEh

Address : C000 28D0h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLB_TP_EADR**	Source and Even Field Address of Top Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-50. SOURCE ADDRESS OF REGION B(MLC_YUVB_TP_EADR)

Source Address of Region B(MLC_YUVB_BT_OADR)

Address : C000 28D2h

Address : C000 28D4h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLB_BT_OADR**	Source and Odd Field Address of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-51. SOURCE ADDRESS OF REGION B(MLC_YUVB_BT_OADR)

Source Address of Region B(MLC_YUVB_BT_EADR)

Address : C000 28D6h

Address : C000 28D8h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_VLB_BT_EADR**	Source and Even Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00

TABLE 13-52. SOURCE ADDRESS OF REGION B(MLC_YUVB_BT_EADR)

13.4.2.2 OSD

The OSD handles 2, 4, or 8 bits of Indexed Data. The 8-bit Indexed Data supports compressed Data. The OSD File Format consists of Top Header, Palette, Frame or Region Header by Field and Bit map (or Run Length Encoding). The ARM CPU handles the Top Header and the Palette and then writes on a Palette RAM and a Register. The OSD Decoder handles Region Header and Pixel Data.

The OSD starts from the Register set by the CPU (Address of a Top Header) whenever Vertical Sync. The OSD can have windows as many as the number of Region Headers, but several windows cannot be placed on the same Horizontal Line at the same time. The Data of the OSD Mix/Mux with other images. The Mixing function has Global Weight Value and Local Weight Value. The Global Weight value is present at the Header and the Local Weigh Value is placed on the Palette Ram. 'Two pixels per data' function reduce the size of OSD Data. The Compressed Data is the Run Length method. The Compressed Data Format consists of {"11", Run_Length[5:0]} + Pixel Data format and Pixel Data + Pixel Data format. The former means that Pixel Data numbers are the same as the Run_length, the letter means that different data are consecutive. The OSD can also change the processing order with Sub-Picture.

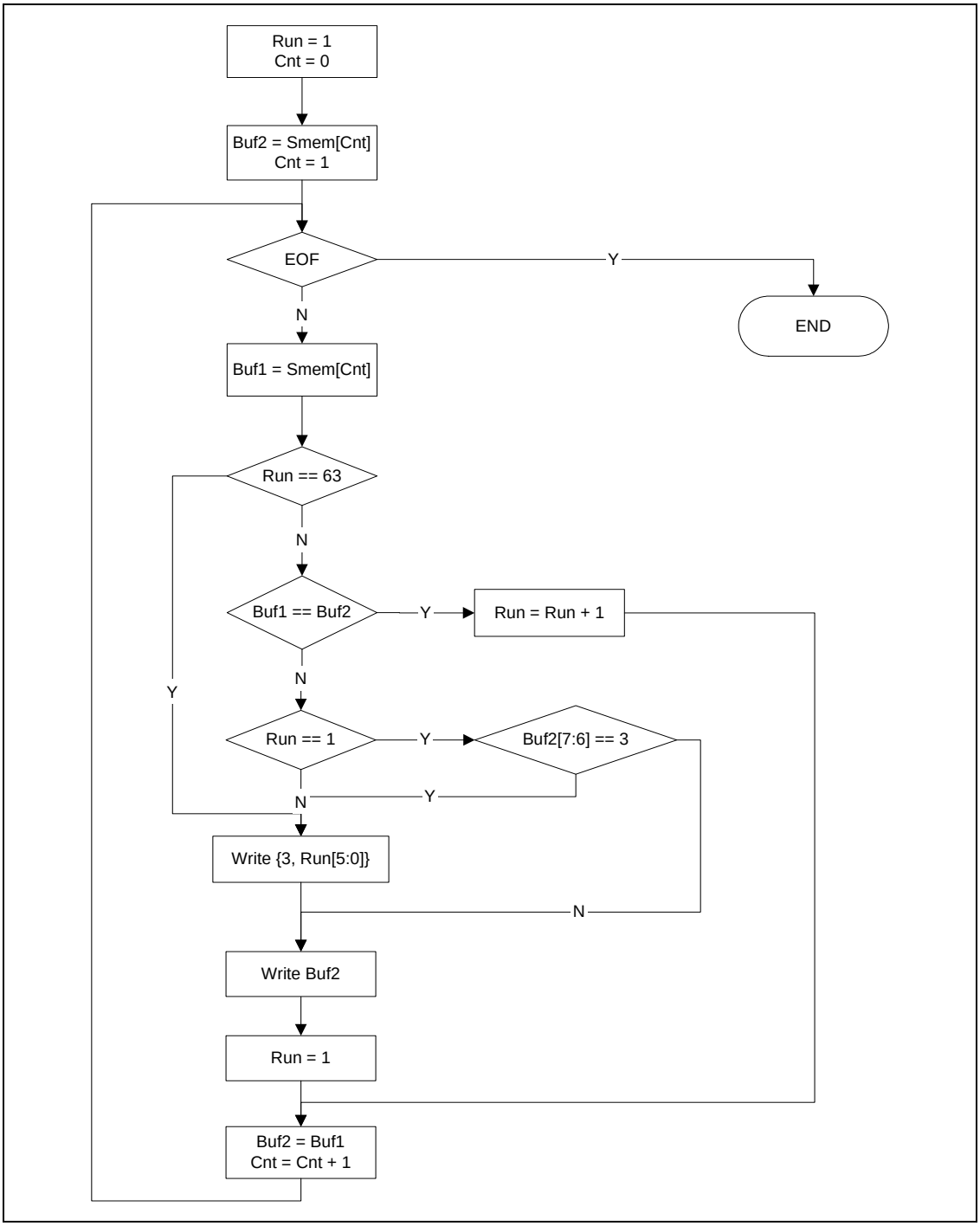


Figure 13-7. 8 bit Compressed Data Flow Chart

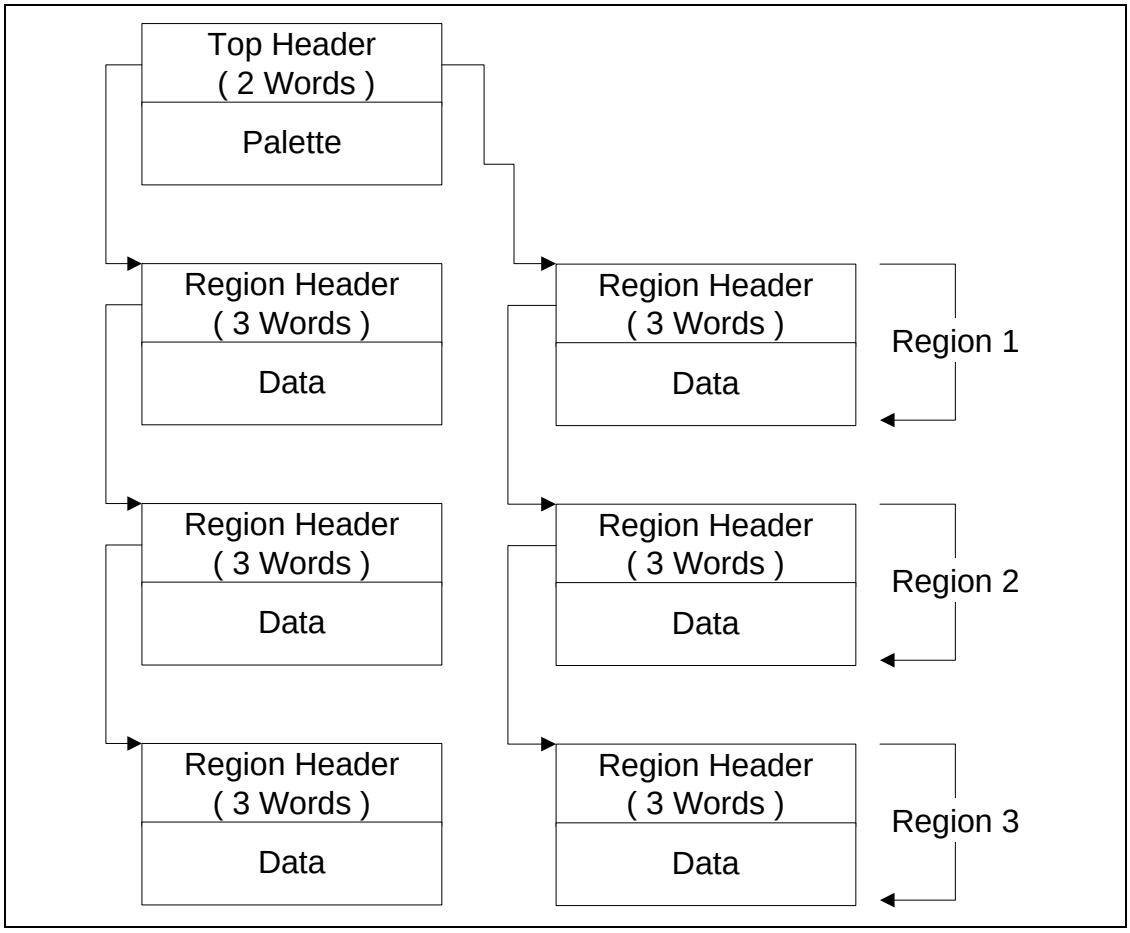


Figure 13-8. OSD FileStructure

OSD Top Header

Bit	Size	Description	Reset Value
31:0	32	DRAM Address of Odd Field Region header. word aligned	
31:0	32	DRAM Address of Even Field Region header. word aligned	

TABLE 13-53. OSD TOP HEADER

OSD Region Header

Header	Bit	Size	Description	Reset Value
Header0	31:0	32	DRAM Address of the next region header. word aligned.	
Header1	30	1	Last Region Header 1 : Last Header	0b
	29	1	Compressed data with PCX like 0 : bit-map 1 : Compressed data	0b
	28	2	Bit per pixel. When bit-map, Valid 0 : 2 bit 1 : 4 bits 2 : 8 bits 3 : reserved	0b
	27	1	Resolution. When bit-map, Valid 0 : 1 pel 1 : 2 pel	0b
	26	1	Global Mix Weight Enable 0 : use mix weight in palette 1 : use Global Mix Weight	
	25:22	4	Mix Weight when Global Mix Weight is enabled, Valid 0 : transparent (0 %), 15 : opaque (100 %)	
	21:11	11	Y Top	
	10:0	11	Y Bottom	
Header2	30	1	Transparent Enable when Global Mix Weight is enabled, Valid	
	29:22	8	Transparent Value. when Transparency is enabled, Valid	
	21:11	11	X Left	
	10:0	11	Y Right	

TABLE 13-54. OSD REGION HEADER

OSD Palette

Palette Data	Alpha[3:0]	Y[7:0]	Cb[7:0]	Cr[7:0]
32 bits	D[31:24]	D[23:16]	D[15:8]	D[7:0]
DRAM Address	N + 3	N + 2	N + 1	N + 0

TABLE 13-55. OSD PALETTE

The Registers to be used for the OSD are shown below:

Mode	Register	Register
OSD Enable	MLC_OSD	
Priority	MLC_SWAP	
DRAM Address	MLC_OSD_OADR	MLC_OSD_EADR
Palette RAM IF	MLC_OSD_PALLT_A	MLC_OSD_PALLT_D

TABLE 13-56. OSD REGISTER

Source Address of OSD(MLC_OSD_OADRL, MLC_OSD_OADRH)

Address : C000 2916h / C000 2918h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	MLC_OSD_OADR	**Odd Field Source Address of OSD**	0x00

TABLE 13-57. SOURCE ADDRESS OF OSD(MLC_OSD_OADRL, MLC_OSD_OADRH)

Source Address of OSD(MLC_OSD_EADRL, MLC_OSD_EADRH)

Address : C000 291Ah / C000 291Ch

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	MLC_OSD_EADR	**Even Field Source Address of OSD**	0x00

TABLE 13-58. SOURCE ADDRESS OF OSD(MLC_OSD_EADRL, MLC_OSD_EADRH)

13.4.2.3 Sub-Picture Unit

The Sub-Picture Unit (SPU) decodes the sub-picture data of DVD and then outputs it according to the pertinent line. The SPU handles the sub-picture information bringing in a frame unit from an external memory. The SPU is divided into pixel data and control data. In addition, the Control data is again divided into normal, change, and highlight. The priority applied to the actual display is the order of highlight > change > normal.

The Host CPU writes the following information on the SPU register:

-. SPU control & configuration information
SPU on/off, frame/field mode selection, highlight on/off

-. SPU decode start delay value
Delay counter value until SPU starts to decode from vsync

-. Decode information start address
Memory address to read the base information required for decode
The base information must be stored by the host CPU by advance

-. Highlight information start address

Memory address to read highlight information

The highlight information must be stored by the host CPU by advance

-. Palette data

RGB sub-picture palette data

Base Information Format

word/bit position	31 24	23 16	15 8	8 0
word 0			command flag (11)	
word 1	base color (16)		base contrast (16)	
word 2	reserved (6)	display start X (12)	reserved (6)	display end X (12)
word 3	reserved (6)	display start Y (12)	reserved (6)	display end Y (12)
word 4	top field data address offset (32)			
word 5	bottom field data address offset (32)			
word 6	CHG command address (32)			

TABLE 13-59. BASE INFORMATION FORMAT

< Command flag >

[10:1] : maximum x size : Horizontal display size. Display size might different from x size of sub-picture.

[0]: CHG command exist. When CHG_COLCON command is in current SP_DCSQ, this Register is 1.

= If '1', CHG info read & process from CHG command address.
= If '0', the use of only the base color/contrast value.

※ For CPU's easy of updating base command info read address of SPU, base info and CHG info address area should be split. (It always increases 6words as unit)

< PXD (Pixel data) byte position >

Start byte position (0 to 3) of the pixel data corresponding to top/bottom field. If a word is aligned, it is '0'. Otherwise, the start byte position is indicated.

< Pixel Data Base Address >

. Upper 16-bit address of the memory area in which pixel data are stored.

< Top/Bottom Field Pixel Data Address Offset >

Lower 16-bit address of the memory area in which pixel data are stored.

< Change Command address >

Memory address in which change information is stored, if the change command exists.

Change Command Information Format

word/bit position	31 24	23 16	15 8	8 0
word 0	reserved (6)	CHG start line (10)	reserved (6)	CHG end line (10)
word 1	change color (16)		change contrast (16)	
word 2	last(1) reserve(5)	CHG start X (10)	reserved (6)	CHG end X (10)
word 1	change color (16)		change contrast (16)	
word 2	last(1) reserve(5)	CHG start X (10)	reserved (6)	CHG end X (10)

TABLE 13-60. CHANGE COMMAND INFORMATION FORMAT

-. If last flag = 0, the pixel change information about next two words exists.

-. If last flag = 1, next one word has the line change information or the change end information (= 32'hffff_ffff).

-. If line change word = end pattern, the CHG information is not read anymore, and the remaining display lines use base color/contrast.

-. Word 0 and word 1/2 include the LN_CTLI information and the PX_CTLI information respectively.

-. The pixel change information needs the change end pixel information.

Highlight Information Format

word/bit position	31 24	23 16	15 8	8 0
word 0	reserved (6)	button start X (10)	reserved (6)	button end X (10)
word 1	reserved (6)	button start Y (10)	reserved (6)	button end Y (10)
word 2	button color (16)		button contrast (16)	

TABLE 13-61. HIGHLIGHT INFORMATION FORMAT

13.4.2.4 RGB Layer

RGB Data supports 8/16/24 bits and has functions for Scale Up/Down, Color Key, and Alpha Blending. The RGB Layer brings Data from an External Memory after selecting the area to display RGB utilizing 5 areas. Each area has independent functions for Alpha Blending and Color Key.

The RGB Format is shown below:

Bits	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
RGB 8bits	P3[7:0]		P2[7:0]		P1[7:0]		P0[7:0]	
RGB 16bits	R1[4:0]	G1[5:0]	B1[4:0]		R0[4:0]	G0[5:0]	B0[4:0]	
RGB 24bits	B1[7:0]		R0[7:0]		G0[7:0]		B0[7:0]	

TABLE 13-62. RGB LAYER

The following figure shows that only Region1 and Region5 have RGB Data (Indexed Data) and the other areas have different Data.

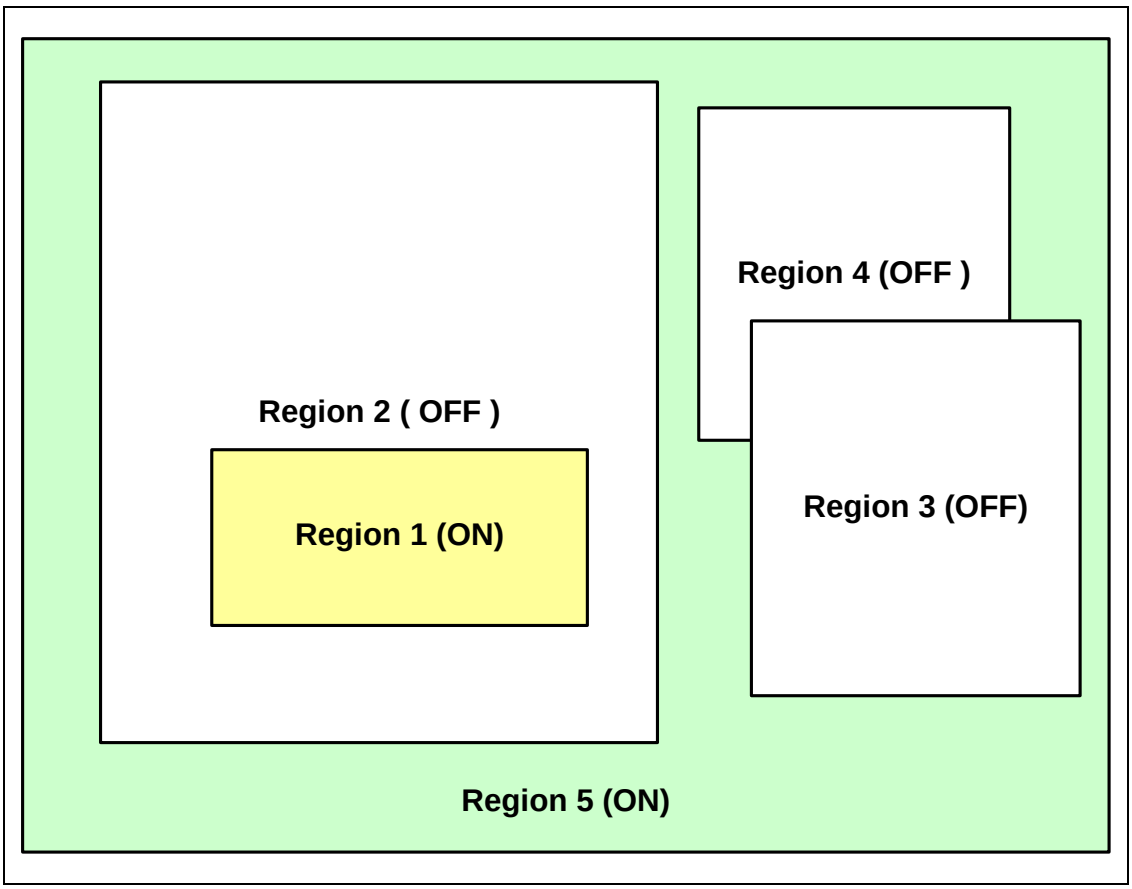


Figure 13-9. RGB Display Mode

Registers for RGB (Indexed Data) Plane are listed in the following table:

Mode	Region 5	Region 4	Region 3	Region 2	Region 1
Enable	MLC_RGB5EN	MLC_RGB4EN	MLC_RGB3EN	MLC_RGB2EN	MLC_RGB1EN
Region Control	MLC_RGB5ACT	MLC_RGB5ACT	MLC_RGB5ACT	MLC_RGB5ACT	MLC_RGB5ACT
Mix / Mux Control	MLC_RGB5_MIXMUX	MLC_RGB4_MIXMUX	MLC_RGB3_MIXMUX	MLC_RGB2_MIXMUX	MLC_RGB1_MIXMUX
Alpha Value	MLC_RGB5_ALPHA	MLC_RGB4_ALPHA	MLC_RGB3_ALPHA	MLC_RGB2_ALPHA	MLC_RGB1_ALPHA
Coordinate of Displayed Region	Full Region (Setting in Display Controller)	MLC_RGB4_STX MLC_RGB 4_ENDX MLC_RGB4_STY MLC_RGB4_ENDY	MLC_RGB3_STX MLC_RGB3_ENDX MLC_RGB3_STY MLC_RGB3_ENDY	MLC_RGB2_STX MLC_RGB2_ENDX MLC_RGB2_STY MLC_RGB2_ENDY	MLC_RGB1_STX MLC_RGB1_ENDX MLC_RGB1_STY MLC_RGB1_ENDY
Bit per pixel	MLC_RGB_BPP				
Color Key	MLC_RGB_CKEY_B, MLC_RGB_CKEY_G, MLC_RGB_CKEY_R				
Scale Factor	MLC_RGB_HSC, MLC_RGB_VSC				
Source Data Information	MLC_RGB_HW				
DRAM Address	MLC_RGB_OADR, MLC_RGB_EADR				

TABLE 13-63. RGB PLANE REGISTERS LIST

Still Image Control Register (MLC_STL_CNTL)

Address : C000 28Dah

Bit	R/W	Symbol	Description	Reset Value
[10:9]	R/W	**MLC_STL_BPP**	Bit Per Pixel of Still Image(RGB) Layer 0 = 4bpp 1= 8bpp 2 = 16bpp 3 = 24bpp	0x0
[8]	R/W	**MLC_STL5ACT**	Activate Region 5 of Still Image(RGB) Layer.	0x0
[7]	R/W	**Reserved**	Fix "1"	
[6]	R/W	**MLC_STL4ACT**	Activate Region 4 of Still Image(RGB) Layer.	0x0
[5]	R/W	**Reserved**	Fix "1"	
[4]	R/W	**MLC_STL3ACT**	Activate Region 3 of Still Image(RGB) Layer.	0x0
[3]	R/W	**Reserved**	Fix "1"	
[2]	R/W	**MLC_STL2ACT**	Activate Region 2 of Still Image(RGB) Layer.	0x0
[1]	R/W	**Reserved**	Fix "1"	

[0]	R/W	**MLC_STL1ACT**	Activate Region 1 of Still Image(RGB) Layer.	0x0

TABLE 13-64. STILL IMAGE CONTROL REGISTER (MLC_STL_CNTL)

Mix/ Mux Control Register (MLC_STL_MIXMUX)

Address ***: C000 28DCh***

Bit	R/W	Symbol	Description	Reset Value
[9:8]	R/W	**MLC_STL5_MIXMUX**	Mix/Mux of Region 5 at Still Image(RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[7:6]	R/W	**MLC_STL4_MIXMUX**	Mix/Mux of Region 4 at Still Image(RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[5:4]	R/W	**MLC_STL3_MIXMUX**	Mix/Mux of Region 3 at Still Image(RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[3:2]	R/W	**MLC_STL2_MIXMUX**	Mix/Mux of Region 2 at Still Image(RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[1:0]	R/W	**MLC_STL1_MIXMUX**	Mix/Mux of Region 1 at Still Image(RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0

TABLE 13-65. MIX/ MUX CONTROL REGISTER (MLC_STL_MIXMUX)

Alpha Blending Value Register (MLC_RGB_ALPHAL)

Address : C000 28Deh

Bit	R/W	Symbol	Description	Reset Value
[11:8]	R/W	**MLC_RGB3_ALPHA**	Alpha Value of Region 3	0x00
[7:4]	R/W	**MLC_RGB2_ALPHA**	Alpha Value of Region 2	0x00
[7:4]	R/W	**MLC_RGB1_ALPHA**	Alpha Value of Region 1	0x00

TABLE 13-66. ALPHA BLENDING VALUE REGISTER (MLC_RGB_ALPHAL)

Alpha Blending Value register (MLC_STL_ALPHAL)

Address : C000 28Deh

Bit	R/W	Symbol	Description	Reset Value
[11:8]	R/W	**MLC_STL3_ALPHA**	Alpha Value of Region 3 at Still Image (RGB) Layer	0x00
[7:4]	R/W	**MLC_STL2_ALPHA**	Alpha Value of Region 2 at Still Image (RGB) Layer	0x00
[7:4]	R/W	**MLC_STL1_ALPHA**	Alpha Value of Region 1 at Still Image (RGB) Layer	0x00

TABLE 13-67. ALPHA BLENDING VALUE REGISTER (MLC_STL_ALPHAL)

Alpha Blending Value Register (MLC_STL_ALPHAH)

Address : C000 28E0h

Bit	R/W	Symbol	Description	Reset Value
[7:4]	R/W	**MLC_STL5_ALPHA**	Alpha Value of Region 5 at Still Image (RGB) Layer	0x00
[3:0]	R/W	**MLC_STL4_ALPHA**	Alpha Value of Region 4 at Still Image (RGB) Layer	0x00

TABLE 13-68. ALPHA BLENDING VALUE REGISTER (MLC_STL_ALPHAH)

Coordinate Register of Still Image (RGB) Layer (MLC_STL1_STX, MLC_STL2_STX, MLC_STL3_STX, MLC_STL4_STX)

Address : C000 28E2h / C000 28EAh / C000 28F2h / C000 28Fah

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_STLn_STX**	Horizontal Starting Point of Region n at Still Image (RGB) Layer	0x00

TABLE 13-69. COORDINATE REGISTER OF STILL IMAGE (RGB) LAYER(MLC_STL1_STX, MLC_STL2_STX, MLC_STL3_STX, MLC_STL4_STX)

Coordinate Register of Still Image (RGB) Layer (MLC_ STL1_ENDX, MLC_ STL2_ENDX, MLC_ STL3_ENDX, MLC_ STL4_ENDX)

Address : C000 28E4h / C000 28ECh / C000 28F4h / C000 28FCh

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_STLn_ENDX**	Horizontal Ending Point of Region n at Still Image (RGB) Layer	0x00

TABLE 13-70. COORDINATE REGISTER OF STILL IMAGE (RGB) LAYER(MLC_ STL1_ENDX, MLC_ STL2_ENDX, MLC_ STL3_ENDX, MLC_ STL4_ENDX)

Coordinate Register of Still Image (RGB) Layer (MLC_ STL1_STY, MLC_ STL2_STY, MLC_ STL3_STY, MLC_ STL4_STY)

Address : C000 28E6h / C000 28EEh / C000 28F6h / C000 28Feh

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_STLn_STY**	Vertical Starting Point of Region n at Still Image (RGB) Layer	0x00

TABLE 13-71. COORDINATE REGISTER OF STILL IMAGE (RGB) LAYER(MLC_ STL1_STY, MLC_ STL2_STY, MLC_ STL3_STY, MLC_ STL4_STY)

Coordinate Register of Still Image (RGB) Layer (MLC_ STL1_ENDY, MLC_ STL2_ENDY, MLC_ STL3_ENDY, MLC_ STL4_ENDY)

Address : C000 28E8h / C000 28F0h / C000 28F8h / C000 2900h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_STLn_ENDY**	Vertical Ending Point of Region n at Still Image (RGB) Layer	0x00

TABLE 13-72. COORDINATE REGISTER OF STILL IMAGE (RGB) LAYER(MLC_ STL1_ENDY, MLC_ STL2_ENDY, MLC_ STL3_ENDY, MLC_ STL4_ENDY)

Color Key register of Still Image (RGB) Layer (MLC_STL_CKEY_GR)

Address : C000 2902h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_STL_CKEYG**	Color Key of G Color	0x00
[7:0]	R/W	**MLC_STL_CKEYB**	Color Key of B Color	0x00

TABLE 13-73. COLOR KEY REGISTER OF STILL IMAGE (RGB) LAYER (MLC_STL_CKEY_GR)

Color Key Register of Still Image (RGB) Layer (MLC_STL_CKEY_R)

Address : C000 2904h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**MLC_STL_CKEYB**	Color Key of R Color	0x00

TABLE 13-74. COLOR KEY REGISTER OF STILL IMAGE (RGB) LAYER (MLC_STL_CKEY_R)

Scale Factor Register of Still Image (RGB) Layer (MLC_STL_HSC)

Address : C000 2906h

Bit	R/W	Symbol	Description	Reset Value
[13:0]	R/W	**MLC_STL_HSC**	Horizontal Scale Factor of Still Image (RGB) Layer MLC_STL_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

TABLE 13-75. SCALE FACTOR REGISTER OF STILL IMAGE (RGB) LAYER (MLC_STL_HSC)

Scale Factor Register of Still Image(RGB) Layer (MLC_STL_VSCL, MLC_STL_VSCH)

Address : C000 2908h / C000 290Ah

Bit	R/W	Symbol	Description	Reset Value
[24:0]	R/W	**MLC_STL_VSC**	Vertical Scale Factor of Still Image (RGB) Layer ISP_STL_VSC = Ratio x MLC_STL_HW When Ration > 1, Scale Down	00

TABLE 13-76. SCALE FACTOR REGISTER OF STILL IMAGE(RGB) LAYER (MLC_STL_VSCL, MLC_STL_VSCH)

Horizontal Width Register of Still Image(RGB) Layer (MLC_STL_HW)

Address : C000 290Ch

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**MLC_STL_HW**	Horizontal Pixel Width of Still Image(RGB) Layer When MLC_STL_BPP = 24bit, MLC_VLA_TP_HW = Pixel Width x 3 When MLC_STL_BPP =16bit, MLC_VLA_TP_HW = Pixel x 2 When MLC_STL_BPP =8bit, MLC_VLA_TP_HW = Pixel x 1 When MLC_STL_BPP =4bit, MLC_VLA_TP_HW = Pixel / 2	00

TABLE 13-77. HORIZONTAL WIDTH REGISTER OF STILL IMAGE(RGB) LAYER (MLC_STL_HW)

Source Address of Still Image (RGB) Layer (MLC_STL_OADRL, MLC_STL_OADRH)

Address : C000 290Eh / C000 2910h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_STL_OADR**	Source and Odd Field Address of Still Image (RGB) Layer	0x00

TABLE 13-78. SOURCE ADDRESS OF STILL IMAGE (RGB) LAYER (MLC_STL_OADRL, MLC_STL_OADRH)

Source Address of Still Image (RGB) Layer (MLC_STL_EADRL, MLC_STL_EADRH)

Address : C000 2912h / C000 2914h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_STL_EADR**	Source and Even Field Address of Still Image (RGB) Layer	0x00

TABLE 13-79. SOURCE ADDRESS OF STILL IMAGE (RGB) LAYER (MLC_STL_EADRL, MLC_STL_EADRH)

13.4.2.5 Hardware Cursor

The BPP (bits per pixel) and the Size of a Hardware Cursor are two-BPP and 32-bit or 64-bit respectively. The Hardware Cursor Data is per the table below. Alpha Blending supports Background Color and Foreground Color.

Cursor Pattern Data

Bit	Description
00b	Fore Ground Color

Bit	Description
01b	Background Color
10b	Transparency
11b	Invert Transparency

TABLE 13-80. CURSOR PATTERN DATA

Ex) For example, if the cursor pattern is 8x8 as below:

Bits	[1:0]	[3:2]	[5:4]	[7:6]	[9:8]	[11:10]	[13:12]	[15:14]	Binary value	Hex value
							10	10	10100101_01010101	0xa555
		00	00	00		10	10	10	10101001_00000001	0xa901
		00	00		10	10	10	10	10101010_01000001	0xaa41
		00		00		10	10	10	10101001_00010001	0xa911
			10		00		10	10	10100100_01100101	0xa465
		10	10	10		00		10	10010001_10101001	0x91a9
10	10	10	10	10			00		01000110_10101010	0x46aa
10	10	10	10	10	10			10	10011010_10101010	0x9aaa

Figure 13-10. 8x8 Cursor Pattern

Where,

	01	Background color
	10	Transparency Area
	00	Foreground color

Registers for H/W cursor are listed in the following table:

Mode	Foreground	Background	Transparency	Inverted Transparency
Enable	MLC_CURSOR			
Size	MLC_HWC_SZ			
Position	MLC_HWC_STX, MLC_HWC_STY			
DRAM Address	MLC_HWC_OADR, MLC_HWC_EADR			
Alpha Value	MLC_HWC_FALPH	MLC_HWC_BALPH		
Color	MLC_HWC_FG MLC_HWC_FR MLC_HWC_FB	MLC_HWC_BG MLC_HWC_BR MLC_HWC_BB		

TABLE 13-81. HARDWARE CURSOR REGISTERS

Hardware Cursor Control Register (MLC_HWC_CNTR)

Address : C000 291Eh

Bit	R/W	Symbol	Description	Reset Value
[15:12]	R/W	**MLC_HWC_FALPH**	Foreground Alpha Value of Hardware Cursor	0x0
[11:8]	R/W	**MLC_HWC_FALPH**	Background Alpha Value of Hardware Cursor	0x0
[6:0]	R/W	**MLC_HWC_SZ**	Cursor Pixel Size 0x20: 32x32 pixel 0x40: 64x64 pixel	0x00

TABLE 13-82. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_CNTR)

Hardware Cursor Control Register (MLC_HWC_STX, MLC_HWC_STY)

Address : C000 2920h / C000 2922h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MLC_HWC_STX**	Horizontal Starting Position of Hardware Cursor	0x00
[11:0]	R/W	**MLC_HWC_STY**	Vertical Starting Position of Hardware Cursor	0x00

TABLE 13-83. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_STX, MLC_HWC_STY)

Hardware Cursor Control Register (MLC_HWC_FGR)

Address : C000 2924h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_HWC_FG**	Foreground Color (Green) of Hardware Cursor	0x00
[7:0]	R/W	**MLC_HWC_FR**	Foreground Color (Red) of Hardware Cursor	0x00

TABLE 13-84. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_FGR)

Hardware Cursor Control Register (MLC_HWC_FB)

Address : C000 2926h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**MLC_HWC_FB**	Foreground Color (Blue) of Hardware Cursor	0x00

TABLE 13-85. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_FB)

Hardware Cursor Control Register (MLC_HWC_BGR)

Address : C000 2928h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_HWC_BG**	Background Color (Green) of Hardware Cursor	0x00
[7:0]	R/W	**MLC_HWC_BR**	Background Color (Red) of Hardware Cursor	0x00

TABLE 13-86. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_BGR)

Hardware Cursor Control Register (MLC_HWC_BB)

Address : C000 292Ah

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**MLC_HWC_BB**	Background Color (Blue) of Hardware Cursor	0x00

TABLE 13-87. HARDWARE CURSOR CONTROL REGISTER (MLC_HWC_BB)

Source Address of Hardware Cursor (MLC_HWC_OADRL, MLC_HWC_OADRH)

Address : C000 292Ch

Address : C000 292Eh

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_HWC_OADR**	Source and Odd Field Address of Hardware Cursor	0x00

TABLE 13-88. SOURCE ADDRESS OF HARDWARE CURSOR (MLC_HWC_OADRL, MLC_HWC_OADRH)

Source Address of Hardware Cursor (MLC_HWC_EADRL, MLC_HWC_EADRH)

Address : C000 2930h

Address : C000 2932h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**MLC_HWC_EADR**	Source and Even Field Address of Hardware Cursor	0x00

TABLE 13-89. SOURCE ADDRESS OF HARDWARE CURSOR (MLC_HWC_EADRL, MLC_HWC_EADRH)

13.4.2.6 Luminance Enhancement

The Multi Layer Controller adjusts image quality by controlling Contrast and Brightness on Luminance Data. The Contrast uses 8 levels of Contrast Factor, and the Brightness uses 256 levels of Brightness Factor from -128 to 127.

Luminance Enhancement Control Register (MLC_LUMA_ENH)

Address : C000 2934h

Bit	R/W	Symbol	Description	Reset Value
[10:8]	R/W	**MLC_CNTRST**	Contrast control 0 : 1.00 1 : 1.125 2 : 1.25 3 : 1.375 4 : 1.5 5 : 1.625 6 : 1.75 7 : 1.875	0x00
[7:0]	R/W	**MLC_BRIGHT**	Brightness Control 2's complement	0x00

TABLE 13-90. LUMINANCE ENHANCEMENT CONTROL REGISTER (MLC_LUMA_ENH)

13.4.2.7 Chrominance Enhancement

The Multi Layer Controller adjusts image quality by controlling Hue and Saturation on Chrominance Data.

Since the Cos(θ)/ Sin(θ) of the Hue control is between –2 and 2, the Saturation can be adjusted with the Hue Control.

Hue Control uses the following formula:
(B-Y)' = (B-Y) * Cos(θ) - (R-Y) * Sin(θ)
(R-Y)' = (B-Y) * (-Sin(θ)) + (R-Y) * Cos(θ)

The result for each quadrant is obtained from the following equations. At each equation, the Gain factor value range is -2 to +2.
1) 1st quadrant ((B-Y) ³ 0 & (R-Y) ³ 0)
(B-Y)' = (B-Y) x MLC_HUECB1_A + (R-Y) x MLC_HUECB 1_B
(R-Y)' = (B-Y) x MLC_HUECR1_A + (R-Y) x MLC_HUECR1_B
2) 2nd quadrant ((B-Y) < 0 & (R-Y) = 0)
(B-Y)' = (B-Y) x MLC_HUECB2_A + (R-Y) x MLC_HUECB2_B
(R-Y)' = (B-Y) x MLC_HUECR2_A + (R-Y) x MLC_HUECR _B
3) 3rd quadrant ((B-Y) < 0 & (R-Y) < 0)
(B-Y)' = (B-Y) x MLC_HUECB3_A + (R-Y) x MLC_HUECB3_B
(R-Y)' = (B-Y) x MLC_HUECR3_A + (R-Y) x MLC_HUECR3_B
4) 4th quadrant ((B-Y) = 0 & (R-Y) < 0)
(B-Y)' = (B-Y) x MLC_HUECB4_A + (R-Y) x MLC_HUECB4_B
(R-Y)' = (B-Y) x MLC_HUECR4_A + (R-Y) x MLC_HUECR4_B

The example of the Hue Control is shown below:

Register	30 Degree of all quadrant (cos(30°) = 0.866) (sin(30°) = 0.5)	30 degree of 1st quadrant (cos(0°) = 1.0) (sin(0°) = 0.0)
MLC_HUECB1_A	0.866 * 64 * Saturation Gain	0.866 * 64 * Saturation Gain
MLC_HUECB1_B	0.50 * 64 * Saturation Gain	0.50 * 64 * Saturation Gain
MLC_HUECR1_A	-0.50 * 64 * Saturation Gain	-0.50 * 64 * Saturation Gain
MLC_HUECR1_B	0.866 * 64 * Saturation Gain	0.866 * 64 * Saturation Gain
MLC_HUECB2_A	0.866 * 64 * Saturation Gain	1.00 * 64 * Saturation Gain
MLC_HUECB2_B	0.50 * 64 * Saturation Gain	0.00 * 64 * Saturation Gain
MLC_HUECR2_A	-0.50 * 64 * Saturation Gain	-0.00 * 64 * Saturation Gain
MLC_HUECR2_B	0.866 * 64 * Saturation Gain	1.0 * 64 * Saturation Gain 2.0

Register	30 Degree of all quadrant (cos(30°) = 0.866) (sin(30°) = 0.5)	30 degree of 1st quadrant (cos(0°) = 1.0) (sin(0°) = 0.0)
MLC_HUECB3_A	0.866 * 64 * Saturation Gain	1.00 * 64 * Saturation Gain
MLC_HUECB3_B	0.50 * 64 * Saturation Gain	0.00 * 64 * Saturation Gain
MLC_HUECR3_A	-0.50 * 64 * Saturation Gain	-0.00 * 64 * Saturation Gain
MLC_HUECR3_B	0.866 * 64 * Saturation Gain	1.00 * 64 * Saturation Gain
MLC_HUECB4_A	0.866 * 64 * Saturation Gain	1.00 * 64 * Saturation Gain
MLC_HUECB4_B	0.50 * 64 * Saturation Gain	0.00 * 64 * Saturation Gain
MLC_HUECR4_A	-0.50 * 64 * Saturation Gain	-0.00 * 64 * Saturation Gain
MLC_HUECR4_B	0.866 * 64 * Saturation Gain	1.00 * 64 * Saturation Gain

TABLE 13-91. HUE CONTROL

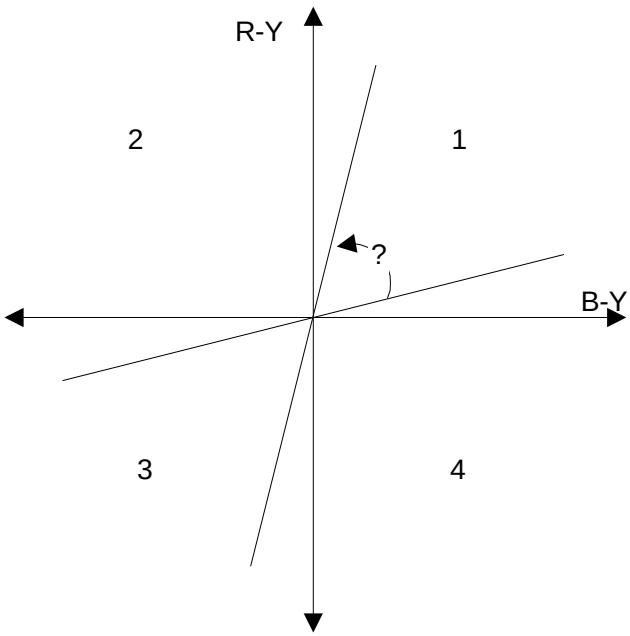


Figure 13-11. The basic Concept of Hue Control

Chrominance Enhancement Control Register (MLC_HUECB1AB, MLC_HUECB2AB, MLC_HUECB3AB, MLC_HUECB4AB)

Address : C000 2936h / C000 293Ah / C000 293Eh / C000 2942h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_HUECBnA**	Gain is -2 to +2 Decimal Point = [6.5][1] 2's complement	0x40
[7:0]	R/W	**MLC_HUECBnB**	Gain is –2 to +2 Decimal Point = [6.5][1] 2's complement	0x00
			At each Coordinate, input the result of following equations: (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer to Figure 22-9. The basic Concept of Hue Control	

TABLE 13-92. CHROMINANCE ENHANCEMENT CONTROL REGISTER(MLC_HUECB1AB, MLC_HUECB2AB, MLC_HUECB3AB, MLC_HUECB4AB)

Chrominance Enhancement Control Register (MLC_HUECR1AB, MLC_HUECR2AB, MLC_HUECR3AB, MLC_HUECR4AB)

Address : C000 2938h / C000 293Ch / C000 2940h / C000 2944h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_HUECRnA**	Gain is -2 to +2, Decimal Point = [6.5][1] 2's complement	0x00
[7:0]	R/W	**MLC_HUECRnB**	Gain is -2 to +2, Decimal Point = [6.5][1] 2's complement	0x40
			At each Coordinate, input the result of following equations: (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer to Figure 22-9. The Basic Concept of Hue Control	

TABLE 13-93. CHROMINANCE ENHANCEMENT CONTROL REGISTER (MLC_HUECR1AB, MLC_HUECR2AB, MLC_HUECR3AB, MLC_HUECR4AB)

(MLC_HUECB1AB, MLC_HUECB2AB, MLC_HUECB3AB, MLC_HUECB4AB)

Note 1: Decimal Point = [6.5] :
8 bits = [21 20 1/2 1/4 1/8 1/16 1/32 1/64]

For Example.
"0100_0000"=64/64=1, "0010_0000"=32/64=0.5, "1000_0000"=(-128)/64=(-2), "1100_0000"=(-64)/64=(-1)

13.4.2.8 Dithering

If the BPP (bits per pixel) of Source Data are bigger than the BPP of Display Data, Data loss is generated. In the case of Data loss, the Dithering makes image quality much more smooth. The Dithering supports 2 X 2 and 4 X 4 Types.

Registers for the Dithering are shown below:

Dither Control Register (MLC_DITHER)

Address : C000 2946h

Bit	R/W	Symbol	Description	Reset Value
[1]	R/W	**MLC_DITHER_ON**	Dithering Skip Enable. (0 : Dither ON 1 : Dither OFF)	1
[0]	R/W	**MLC_DITHER_TY**	Dithering Type. (0 : 2x2 1 : 4x4)	0

TABLE 13-94. DITHER CONTROL REGISTER (MLC_DITHER)

13.4.2.9 Gamma Correction

The Gamma Correction uses 256 X 8 RAMs of R/G/B respectively. Therefore, Users are free to select the desired Gamma Curve. A Gamma Table writes a table address on MLC_GAMMA_A. Whenever the Table writes on MLC_GAMMA_D, the Table address is increased automatically.

Registers for the Gamma Correction are shown below:

Mode	Register
Enable	MLC_GAMM_BYPATH
Address	MLC_GAMMA_A
Data Write	MLC_GAMMA_D

TABLE 13-95. GAMMA CORRECTION REGISTERS

Display Table Control (MLC_GAMMA_A, DISP_ GAMMA_D)

Address : C000 295Ch / C000 295Eh

Bit	R/W	Symbol	Description	Reset Value
	R/W	**MLC_GAMMA_A**	Address Interface of Gamma Table	0x00
	R/W	**MLC_ GAMMA_D**	Data Interface of Gamma Table The address will increase automatically after writing the Data	0x00

TABLE 13-96. DISPLAY TABLE CONTROL (MLC_GAMMA_A, DISP_ GAMMA_D)

13.4.2.10 Scale

The Scale of the YUV Layer and the RGB Layer is a Coarse scale. The Scale of the OSD and the Sub-Picture uses a Scale Processor. The Scale information for each mode is shown below:

Data Path	Register
External Memory → YUV , Region A, Top	MLC_YUVA_TP_HSC, MLC_YUVA_TP_VSC
External Memory → YUV , Region A, Bottom	MLC_YUVA_BT_HSC, MLC_YUVA_BT_VSC
External Memory → YUV , Region B, Top	MLC_YUVB_TP_HSC, MLC_YUVB_TP_VSC
External Memory → YUV , Region B, Bottom	MLC_YUVB_BT_HSC, MLC_YUVB_BT_VSC
FDC → YUV , Region B, Top	MLC_YUVB_BT_HSC, MLC_YUVB_BT_VSC
FDC → YUV , Region B, Bottom	Can't Use
External Memory → RGB Layer	MLC_RGB_HSC, MLC_RGB_VSC
External Memory → YUV, OSD, Sub-Picture Layer → Scale Processor	The Scale Parameter of MLC becomes 'Off', and the Register of the Scale Processor is set.

TABLE 13-97. SCALE INFORMATION

13.4.2.11 Interlaced / Progressive Display

The Multi Layer Controller is compatible with both Interlaced Display and Progressive Display. In Interlaced Display, the CPU sets an Even/Odd Starting Address. Then the Field Signal coming from the Display Sync Generation Part is displayed, distinguishing between even address and odd address. In Progressive Display, the CPU may set the same values on the Even/Odd Starting Address.

Registers for Interlaced/Progressive Display are listed below:

Mode	Register
Control	DISP_FLD_POL
Address	Even/Odd Address of each Plane
Pixel Width	Pixel Width of each Plane
Scale Factor	Refer Scale Processor Block.

TABLE 13-98. INTERLACED/PROGRESSIVE DISPLAY REGISTERS LIST

13.4.3 MLC REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
Overlay Control Register (MLC_OVLAY_CNTR) ***Address : C000 2880h***				
[15]	R/W	**DISP_BOTH_PATH**	When Overlay to Scale Processor Mode, Select Data Path. 0 : Display to Scale only 1 : overlay to Scale and overlay to Display	0
[14]	R/W	**DISP_OVLY2SCLE**	Select Overlay to Scale Processor Mode 0 : overlay to Display Mode 1 : overlay to Scale Mode	0
[13]	R/W	**DISP_FLD_POL**	When Field Mode, Select Polarity of Field Signal from Display Sync. Generation Block. 0 : Normal 1 : Inversion	0
[12]	R/W	**DISP_GAMM_BYPATH**	Select Bypath of RGB Gamma Table 0 : Gamma On 1 : By path	0
[11]	R/W	**DISP_SWAP**	Select Priority of OSD and Sub-Picture 0 : OSD Priority 1 : Sub Picture Priority	0
[10]		**Reserved**	-	-
[9]	R/W	**DISP_CURSOR**	Cursor Enable / Disable 0 : Cursor Disable 1 : Cursor Enable	0
[8]	R/W	**DISP_SUBPICTURE**	Sub-Picture Enable/ Disable 0 : Sub-Picture Disable 1 : Sub-Picture Enable	0
[7]	R/W	**DISP_OSD**	OSD Enable/ Disable 0 : OSD Disable 1 : OSD Enable	0
[6]	R/W	**DISP_STL5EN**	Region 5 Enable/Disable at Still Image (RGB) Layer 0 : Disable 1 : Enable	0

Bit	R/W	Symbol	Description	Reset Value
[5]	R/W	**DISP_STL4EN**	Region 4 Enable/Disable at Still Image (RGB) Layer 0 : Disable 1 : Enable	0
[4]	R/W	**DISP_STL3EN**	Region 3 Enable/Disable at Still Image (RGB) Layer 0 : Disable 1 : Enable	0
[3]	R/W	**DISP_STL2EN**	Region 2 Enable/Disable at Still Image(RGB) Layer 0 : Disable 1 : Enable	0
[2]	R/W	**DISP_STL1EN**	Region 1 Enable/Disable at Still Image (RGB) Layer 0 : Disable 1 : Enable	0
[1]	R/W	**DISP_VLBON**	Region B Enable/Disable at Video(Y/Cb/Cr) Layer. Data Region B is from External Memory or Frame Dimension Converter. 0 : Disable 1 : Enable	0
[0]	R/W	**DISP_ VIAON**	Region A Enable/Disable at Video(Y/Cb/Cr) Layer. Data Region A is from External Memory or Scale Processor. 0 : Disable 1 : Enable	0
Effect of Video Image (MLC_YUV_EFECT) ***Address : C000 2882h***				
[9]	R/W	**MLC_VLB_BT**	Divide Region B of Video (Y/Cb/Cr) Layer with Top and Bottom Region. 0 : Disable 1 : Enable	0x0
[8]	R/W	**MLC_VLB_TP_MR_H**	Horizontal Mirror of Top Region B at Video (Y/Cb/Cr) Layer.	0x0
[7]	R/W	**MLC_VLB_TP_MR_V**	Vertical Mirror of Top Region B at Video(Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[6]	R/W	**MLC_VLB_BT_MR_H**	Horizontal Mirror of Bottom Region B at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[5]	R/W	**MLC_VLB_BT_MR_V**	Vertical Mirror of Bottom Region B at Video(Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[4]	R/W	**MLC_VLA_BT**	Divide Region A of Video (Y/Cb/Cr) Layer with Top and Bottom Region. 0 : Disable 1 : Enable	0x0
[3]	R/W	**MLC_VLA_TP_MR_H**	Horizontal Mirror of Top Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[2]	R/W	**MLC_VLA_TP_MR_V**	Vertical Mirror of Top Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[1]	R/W	**MLC_VLA_BT_MR_H**	Horizontal Mirror of Bottom Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0
[0]	R/W	**MLC_VLA_BT_MR_V**	Vertical Mirror of Bottom Region A at Video (Y/Cb/Cr) Layer. 0 : Disable 1 : Enable	0x0

Bit	R/W	Symbol	Description	Reset Value
Video Image Control Register (MLC_YUV_CNTL) ***Address : C000 2884h***				
[13]	R/W	**MLC_VLA_ALP1SKP**	Skip Alpha Blending of Video(Y/Cb/Cr) Layer Region A. When MLClay to Scale Processor and Scale Processor to Display Mode, this bit should be skipped. 0 : No Skip 1 : Skip	0x0
[12]	R/W	**MLC_SC2DP_A**	Input Data Path of Video (Y/Cb/Cr) Layer Region A 0 : External Memory 1 : Scale Processor	0x0
[11]	R/W	**MLC_FDC2DP_B**	Input Data Path of Video (Y/Cb/Cr) Layer Region B 0 : External Memory 1 : Frame Dimension Converter	0x0
[10]	R/W	**MLC_VL_PRIO**	Priority of Region A and Region B at Video (Y/Cb/Cr) Layer. 0 : Region A 1 : Region B	0x0
[9:0]		**Reserved**	-	-
Scale Factor Register of Region A (MLC_YUVA_TP_HSC) ***Address : C000 2886h***				
[13:0]	R/W	**MLC_VLA_TP_HSC**	Horizontal Scale Factor of Top Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_TP_HSC = Ratio x 1024 Scale Down = Ratio > 1	00
Scale Factor Register of Region A (MLC_YUVA_BT_HSC) ***Address : C000 2888h***				
[13:0]	R/W	**MLC_VLA_BT_HSC**	Horizontal Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_BT_HSC = Ratio x 1024 Scale Down = Ratio > 1	00
Scale Factor Register of Region A (MLC_YUVA_TP_HSCL, MLC_YUVA_TP_HSCH) ***Address : C000 288Ah / C000 288Ch***				
[24:0]	R/W	**MLC_VLA_TP_VSC**	Vertical Scale Factor of Top Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_TP_VSC = Ratio x MLC_VLA_TP_PXW Scale Down = Ratio > 1	00
Scale Factor Register of Region A (MLC_YUVA_BT_HSCL, MLC_YUVA_BT_HSCH) ***Address : C000 288Eh / C000 2890h***				
[24:0]	R/W	**MLC_VLA_BT_VSC**	Vertical Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer. MLC_VLA_BT_VSC = Ratio x MLC_VLA_BT_PXW **Scale Down = Ratio > 1**	00
Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW) ***Address : C000 2892h***				
[14:0]	R/W	**MLC_VLA_TP_PXW**	Horizontal Pixel Width of Top Region A at Video (Y/Cb/Cr) Layer.	00

Bit	R/W	Symbol	Description	Reset Value
Horizontal Pixel Width Register of Region A (MLC_YUVA_TP_PXW) ***Address : C000 2894h***				
[14:0]	R/W	**MLC_VLA_BT_PXW**	Horizontal Pixel Width of Bottom Region A at Video (Y/Cb/Cr) Layer.	00
Coordinate Register of Region A (MLC_YUVA_STX) ***Address : C000 2896h***				
[11:0]	R/W	**MLC_VLA_STX**	Horizontal Starting Point of Top/Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region A (MLC_YUVA_ENDX) ***Address : C000 2898h***				
[11:0]	R/W	**MLC_VLA_ENDX**	Horizontal Ending Point of Top/Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region A (MLC_YUVA_TP_STY) ***Address : C000 289Ah***				
[11:0]	R/W	**MLC_VLA_TP_STY**	Vertical Starting Point of Top Region A at Video (Y/Cb/Cr) Layer**.**	0x00
Coordinate Register of Region A (MLC_YUVA_TP_ENDY) ***Address : C000 289Ch***				
[11:0]	R/W	**MLC_VLA_TP_ENDY**	Vertical Ending Point of Top Region A and Vertical Starting Point of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region A (MLC_YUVA_BT_ENDY) ***Address : C000 289Eh***				
[11:0]	R/W	**MLC_VLA_BT_ENDY**	Vertical Ending Point of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region A (MLC_YUVA_TP_OADRL, MLC_YUVA_TP_OADRH) ***Address : C000 28A0h / C000 28A2h***				
[31:0]	R/W	**MLC_VLA_TP_OADR**	Source and Odd Field Address of Top Region A at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region A (MLC_YUVA_TP_EADRL, MLC_YUVA_TP_EADRH) ***Address : C000 28A4h / C000 28A6h***				
[31:0]	R/W	**MLC_VLA_TP_EADR**	Source and Even Field Address of Top Region A at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region A (MLC_YUVA_BT_OADRL, MLC_YUVA_BT_OADRH) ***Address : C000 28A8h / C000 28AAh***				
[31:0]	R/W	**MLC_VLA_BT_OADR**	Source and Odd Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region A (MLC_YUVA_BT_EADRL, MLC_YUVA_BT_EADRH) ***Address : C000 28Ach / C000 28AEh***				
[31:0]	R/W	**MLC_VLA_BT_EADR**	Source and Even Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Scale Factor register of Region B (MLC_YUVB_TP_HSC) ***Address : C000 28B0h***				
[13:0]	R/W	**MLC_VLB_TP_HSC**	Horizontal Scale Factor of Top Region B at Video (Y/Cb/Cr) Layer. MLC_VLB_TP_HSC = Ratio x 1024 Scale Down = Ratio > 1	00

Bit	R/W	Symbol	Description	Reset Value
Scale FactorRregister of Region B (MLC_YUVB_BT_HSC) ***Address : C000 28B2h***				
[13:0]	R/W	**MLC_VLB_BT_HSC**	Horizontal Scale Factor of Bottom Region B at Video(Y/Cb/Cr) Layer. MLC_VLB_BT_HSC = Ratio x 1024 Scale Down = Ratio > 1	00
Scale Factor Register of Region B (MLC_YUVB_TP_VSCL, MLC_YUVB_TP_VSCH) ***Address : C000 28B4h / C000 28B6h***				
[24:0]	R/W	**MLC_VLB_TP_VSC**	Vertical Scale Factor of Top Region B at Video (Y/Cb/Cr) Layer. MLC_VLB_TP_VSC = Ratio x MLC_VLB_TP_PXW Scale Down = Ratio > 1	00
Scale Factor Register of Region B (MLC_YUVB_BT_VSCL, MLC_YUVB_BT_VSCH) ***Address : C000 28B8h / C000 28BAh***				
[24:0]	R/W	**MLC_VLB_BT_VSC**	Vertical Scale Factor of Bottom Region A at Video (Y/Cb/Cr) Layer. MLC_VLB_BT_VSC = Ratio x MLC_VLB_BT_PXW Scale Down = Ratio > 1	00
Horizontal Pixel Width Register of Region B (MLC_YUVB_TP_PXW) ***Address : C000 28BCh***				
[14:0]	R/W	**MLC_VLB_TP_PXW**	Horizontal Pixel Width of Top Region B at Video (Y/Cb/Cr) Layer.	00
Horizontal Pixel Width Register of Region B (MLC_YUVB_BT_PXW) ***Address : C000 28BEh***				
[14:0]	R/W	**MLC_VLB_BT_PXW**	Horizontal Pixel Width of Bottom Region B at Video (Y/Cb/Cr) Layer.	00
Coordinate Register of Region B (MLC_YUVB_STX) ***Address : C000 28C0h***				
[11:0]	R/W	**MLC_VLB_STX**	Horizontal Starting Point of Top/Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region B (MLC_YUVB_ENDX) ***Address : C000 28C2h***				
[11:0]	R/W	**MLC_VLB_ENDX**	Horizontal Ending Point of Top/Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region B (MLC_YUVB_TP_STY) ***Address : C000 28C4h***				
[11:0]	R/W	**MLC_VLB_TP_STY**	Vertical Starting Point of Top Region B at Video (Y/Cb/Cr) Layer	0x00
Coordinate register of Region B (MLC_YUVB_TP_ENDY) ***Address : C000 28C6h***				
[11:0]	R/W	**MLC_VLB_TP_ENDY**	Vertical Ending Point of Top Region A and Vertical Starting Point of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00
Coordinate Register of Region B (MLC_YUVB_BT_ENDY) ***Address : C000 28C8h***				
[11:0]	R/W	**MLC_VLB_BT_ENDY**	Vertical Ending Point of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00

Bit	R/W	Symbol	Description	Reset Value
Source Address of Region B (MLC_YUVB_TP_OADR) ***Address : C000 28Cah / C000 28CCh***				
[31:0]	R/W	**MLC_VLB_TP_OADR**	Source and Odd Field Address of Top Region B at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region B(MLC_YUVB_TP_EADR) ***Address : C000 28Ceh / C000 28D0h***				
[31:0]	R/W	**MLC_VLB_TP_EADR**	Source and Even Field Address of Top Region B at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region B(MLC_YUVB_BT_OADR) ***Address : C000 28D2h / C000 28D4h***				
[31:0]	R/W	**MLC_VLB_BT_OADR**	Source and Odd Field Address of Bottom Region B at Video (Y/Cb/Cr) Layer.	0x00
Source Address of Region B(MLC_YUVB_BT_EADR) ***Address : C000 28D6h / C000 28D8h***				
[31:0]	R/W	MLC_VLB_BT_EADR	Source and Even Field Address of Bottom Region A at Video (Y/Cb/Cr) Layer.	0x00
Still Image Control Register (MLC_STL_CNTL) ***Address : C000 28DAh***				
[10:9]	R/W	**MLC_STL_BPP**	Bit Per Pixel of Still Image(RGB) Layer 0 : 4bpp 1 : 8bpp 2 : 16bpp 3 : 24bpp	0x0
[8]	R/W	**MLC_STL5ACT**	Activate Region 5 of Still Image (RGB) Layer.	0x0
[7]	R/W	**Reserved**	-	
[6]	R/W	**MLC_STL4ACT**	Activate Region 4 of Still Image (RGB) Layer.	0x0
[5]	R/W	**Reserved**	Fix "1"	
[4]	R/W	**MLC_STL3ACT**	Activate Region 3 of Still Image (RGB) Layer.	0x0
[3]	R/W	**Reserved**	Fix "1"	
[2]	R/W	**MLC_STL2ACT**	Activate Region 2 of Still Image (RGB) Layer.	0x0
[1]	R/W	**Reserved**	Fix "1"	
[0]	R/W	**MLC_STL1ACT**	Activate Region 1 of Still Image (RGB) Layer.	0x0
Mix/ Mux Control Register (MLC_STL_MIXMUX) ***Address : C000 28DCh***				
[9:8]	R/W	**MLC_STL5_MIXMUX**	Mix/Mux of Region 5 at Still Image (RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[7:6]	R/W	**MLC_STL4_MIXMUX**	Mix/Mux of Region 4 at Still Image (RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[5:4]	R/W	**MLC_STL3_MIXMUX**	Mix/Mux of Region 3 at Still Image (RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0

Bit	R/W	Symbol	Description	Reset Value
[3:2]	R/W	**MLC_STL2_MIXMUX**	Mix/Mux of Region 2 at Still Image (RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
[1:0]	R/W	**MLC_STL1_MIXMUX**	Mix/Mux of Region 1 at Still Image (RGB) Layer 0 : STL 1 : Color Key 2 : Alpha Blending	0x0
Alpha Blending ValueRregister (MLC_RGB_ALPHAL) ***Address : C000 28DEh***				
[11:8]	R/W	**MLC_RGB3_ALPHA**	Alpha Value of Region 3	0x00
[7:4]	R/W	**MLC_RGB2_ALPHA**	Alpha Value of Region 2	0x00
[7:4]	R/W	**MLC_RGB1_ALPHA**	Alpha Value of Region 1	0x00
Alpha Blending Value Register (MLC_STL_ALPHAL) ***Address : C000 28DEh***				
[11:8]	R/W	**MLC_STL3_ALPHA**	Alpha Value of Region 3 at Still Image (RGB) Layer	0x00
[7:4]	R/W	**MLC_STL2_ALPHA**	Alpha Value of Region 2 at Still Image (RGB) Layer	0x00
[7:4]	R/W	**MLC_STL1_ALPHA**	Alpha Value of Region 1 at Still Image (RGB) Layer	0x00
Alpha Blending Value Register (MLC_STL_ALPHAH) ***Address : C000 28E0h***				
[7:4]	R/W	**MLC_STL5_ALPHA**	Alpha Value of Region 5 at Still Image (RGB) Layer	0x00
[3:0]	R/W	**MLC_STL4_ALPHA**	Alpha Value of Region 4 at Still Image (RGB) Layer	0x00
Coordinate Register of Still Image(RGB) Layer (MLC_STL1_STX, MLC_STL2_STX, MLC_STL3_STX, MLC_STL4_STX) ***Address : C000 28E2h / C000 28EAh / C000 28F2h / C000 28FAh***				
[11:0]	R/W	**MLC_STLn_STX**	Horizontal Starting Point of Region n at Still Image (RGB) Layer.	0x00
Coordinate Register of Still Image (RGB) Layer (MLC_ STL1_ENDX, MLC_ STL2_ENDX, MLC_ STL3_ENDX, MLC_ STL4_ENDX) ***Address : C000 28E4h / C000 28ECh / C000 28F4h / C000 28FCh***				
[11:0]	R/W	**MLC_STLn_ENDX**	Horizontal Ending Point of Region n at Still Image (RGB) Layer.	0x00
Coordinate Register of Still Image (RGB) Layer (MLC_ STL1_STY, MLC_ STL2_STY, MLC_ STL3_STY, MLC_ STL4_STY) ***Address : C000 28E6h / C000 28EEh / C000 28F6h / C000 28FEh***				
[11:0]	R/W	**MLC_STLn_STY**	Vertical Starting Point of Region n at Still Image (RGB) Layer.	0x00
Coordinate Register of Still Image(RGB) Layer (MLC_ STL1_ENDY, MLC_ STL2_ENDY, MLC_ STL3_ENDY, MLC_ STL4_ENDY) ***Address : C000 28E8h / C000 28F0h / C000 28F8h / C000 2900h***				
[11:0]	R/W	**MLC_STLn_ENDY**	Vertical Ending Point of Region n at Still Image (RGB) Layer.	0x00
Color Key Register of Still Image (RGB) Layer (MLC_STL_CKEY_GR) ***Address : C000 2902h***				
[15:8]	R/W	**MLC_STL_CKEYG**	Color Key of G Color	0x00
[7:0]	R/W	**MLC_STL_CKEYB**	Color Key of B Color	0x00

Bit	R/W	Symbol	Description	Reset Value
Color Key Register of Still Image (RGB) Layer (MLC_STL_CKEY_R) ***Address : C000 2904h***				
[7:0]	R/W	**MLC_STL_CKEYB**	Color Key of R Color	0x00
Scale Factor Register of Still Image (RGB) Layer (MLC_STL_HSC) ***Address : C000 2906h***				
[13:0]	R/W	**MLC_STL_HSC**	Horizontal Scale Factor of Still Image (RGB) Layer MLC_STL_HSC = Ratio x 1024 Scale Down = Ratio > 1	00
Scale Factor Register of Still Image (RGB) Layer (MLC_STL_VSCL, MLC_STL_VSCH) ***Address : C000 2908h / C000 290Ah***				
[24:0]	R/W	**MLC_STL_VSC**	Vertical Scale Factor of Still Image (RGB) Layer ISP_STL_VSC = Ratio x MLC_STL_HW When Ration > 1, Scale Down	00
Horizontal Width Register of Still Image(RGB) Layer (MLC_STL_HW) ***Address : C000 290Ch***				
[14:0]	R/W	**MLC_STL_HW**	Horizontal Pixel Width of Still Image (RGB) Layer When MLC_STL_BPP = 24 bit, MLC_VLA_TP_HW = Pixel Width x 3 When MLC_STL_BPP =16 bit, MLC_VLA_TP_HW = Pixel x 2 When MLC_STL_BPP =8 bit, MLC_VLA_TP_HW = Pixel x 1 When MLC_STL_BPP =4 bit, MLC_VLA_TP_HW = Pixel / 2	00
Source Address of Still Image (RGB) Layer (MLC_STL_OADRL, MLC_STL_OADRH) ***Address : C000 290Eh / C000 2910h***				
[31:0]	R/W	**MLC_STL_OADR**	Source and Odd Field Address of Still Image (RGB) Layer	0x00
Source Address of Still Image(RGB) Layer (MLC_STL_EADRL, MLC_STL_EADRH) ***Address : C000 2912h / C000 2914h***				
[31:0]	R/W	**MLC_STL_EADR**	Source and Even Field Address of Still Image (RGB) Layer.	0x00
Source Address of OSD (MLC_OSD_OADRL, MLC_OSD_OADRH) ***Address : C000 2916h / C000 2918h***				
[31:0]	R/W	**MLC_OSD_OADR**	Source and Odd Field Address of OSD	0x00
Source Address of OSD (MLC_OSD_EADRL, MLC_OSD_EADRH) ***Address : C000 291Ah / C000 291Ch***				
[31:0]	R/W	**MLC_OSD_EADR**	Source and Even Field Address of OSD	0x00
Hardware Cursor Control Register (MLC_HWC_CNTR) ***Address : C000 291Eh***				
[15:12]	R/W	**MLC_HWC_FALPH**	Foreground Alpha Value of Hardware Cursor	0x0
[11:8]	R/W	**MLC_HWC_FALPH**	Background Alpha Value of Hardware Cursor	0x0

Bit	R/W	Symbol	Description	Reset Value
[6:0]	R/W	**MLC_HWC_SZ**	Cursor Pixel Size 0x20: 32x32 pixel 0x40: 64x64 pixel	0x00
Hardware Cursor Control Register (MLC_HWC_STX, MLC_HWC_STY) ***Address : C000 2920h / C000 2922h***				
[11:0]	R/W	**MLC_HWC_STX**	Horizontal Starting Position of Hardware Cursor	0x00
[11:0]	R/W	**MLC_HWC_STY**	Vertical Starting Position of Hardware Cursor	0x00
Hardware Cursor Control Register (MLC_HWC_FGR) ***Address : C000 2924h***				
[15:8]	R/W	**MLC_HWC_FG**	Foreground Color (Green) of Hardware Cursor	0x00
[7:0]	R/W	**MLC_HWC_FR**	Foreground Color (Red) of Hardware Cursor	0x00
Hardware Cursor Control Register (MLC_HWC_FB) ***Address : C000 2926h***				
[7:0]	R/W	**MLC_HWC_FB**	Foreground Color (Blue) of Hardware Cursor	0x00
Hardware Cursor Control Register (MLC_HWC_BGR) ***Address : C000 2928h***				
[15:8]	R/W	**MLC_HWC_BG**	Background Color (Green) of Hardware Cursor	0x00
[7:0]	R/W	**MLC_HWC_BR**	Background Color (Red) of Hardware Cursor	0x00
Hardware Cursor Control Register (MLC_HWC_BB) ***Address : C000 292Ah***				
[7:0]	R/W	**MLC_HWC_BB**	Background Color (Blue) of Hardware Cursor	0x00
Source Address of Hardware Cursor (MLC_HWC_OADRL, MLC_HWC_OADRH) ***Address : C000 292Ch / C000 292Eh***				
[31:0]	R/W	**MLC_HWC_OADR**	Source and Odd Field Address of Hardware Cursor	0x00
Source Address of Hardware Cursor (MLC_HWC_EADRL, MLC_HWC_EADRH) ***Address : C000 2930h / C000 2932h***				
[31:0]	R/W	**MLC_HWC_EADR**	Source and Even Field Address of Hardware Cursor	0x00
Luminance Enhancement Control Register (MLC_LUMA_ENH) ***Address : C000 2934h***				
[10:8]	R/W	**MLC_CNTRST**	Contrast control 0 : 1.00 1 : 1.125 2 : 1.25 3 : 1.375, 4 : 1.5, 5 : 1.625 6 : 1.75 7 : 1.875	0x00
[7:0]	R/W	**MLC_BRIGHT**	Brightness Control 2's compliment	0x00
Chrominance Enhancement Control Register (MLC_HUECB1AB, MLC_HUECB2AB, MLC_HUECB3AB, MLC_HUECB4AB) ***Address : C000 2936h / C000 293Ah / C000 293Eh / C000 2942h***				

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**MLC_HUECBnA**	Gain is -2 to +2 Decimal Point = [6.5][1] 2's complement	0x40
[7:0]	R/W	**MLC_HUECBnB**	Gain is –2 to +2 Decimal Point = [6.5][1] 2's complement	0x00
			At each Coordinate, input the result of following equations: (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer to Figure 22-9. The Basic Concept of Hue Control	
Chrominance Enhancement Control Register (MLC_HUECR1AB, MLC_HUECR2AB, MLC_HUECR3AB, MLC_HUECR4AB) ***Address : C000 2938h / C000 293Ch / C000 2940h / C000 2944h***				
[15:8]	R/W	**MLC_HUECRnA**	Gain is -2 to +2, Decimal Point = [6.5][1] 2's complement	0x00
[7:0]	R/W	**MLC_HUECRnB**	Gain is -2 to +2, Decimal Point = [6.5][1] 2's complement	0x40
			At each Coordinate, input the result of following equations: (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer to Figure 22-9. The Basic Concept of Hue Control	
Dither Control Register (MLC_DITHER) ***Address : C000 2946h***				
[1]	R/W	**MLC_DITHER_ON**	Dithering Skip Enable. (0 : Dither ON 1 : Dither OFF)	1
[0]	R/W	**MLC_DITHER_TY**	Dithering Type. (0 : 2x2 1 : 4x4)	0
Reserved Register ***Address : C000 2948h ~ C000 294Ah***				
[15:0]		**Reserved**		
[15:0]		**Reserved**		
Display Table Control (MLC_OSD_PALLT_A, MLC_OSD_PALLT_D) ***Address : C000 2954h / C000 2956h***				
[15:0]	R/W	**MLC_OSD_PALLT_A**	Address Interface of OSD palette Table	0x00
[15:0]	R/W	**MLC_OSD_PALLT_D**	Data Interface of OSD palette Table The address will increase automatically after writing the Data	0x00
Display Table Control (MLC_STL_PALLT_A, MLC_STL_PALLT_D) ***Address : C000 2958h / C000 295Ah***				
[15:0]	R/W	**MLC_STL_PALLT_A**	Address Interface of STL palette Table	0x00
[15:0]	R/W	**MLC_STL_PALLT_D**	Data Interface of STL palette Table	0x00

Bit	R/W	Symbol	Description	Reset Value
			The address will increase automatically after writing the Data	
Display Table Control (MLC_GAMMA_A, MLC_ GAMMA_D) ***Address : C000 295Ch / C000 295Eh***				
[15:0]	R/W	**MLC_GAMMA_A**	Address Interface of Gamma Table	0x00
[15:0]	R/W	**MLC_ GAMMA_D**	Data Interface of Gamma Table The address will increase automatically after writing the Data	0x00
Sub-Picture Unit Control (MLC_SPU_CTRL) ***Address : C000 2974h***				
[2]	R/W	**MLC_SPU_HL_ON**	Highlight mode on/off (1 = on)	0
[1]	R/W	**MLC_SPU_DISP_MODE**	Frame/Field display mode selection. 0 : frame mode 1 : field mode	0
[0]	R/W	**MLC_SPU_ON**	SPU block enable/disable bit. 0 : SPU disable 1 : SPU enable	0
Sub-Picture Decode Start Delay (MLC_SPU_DELAY) ***Address : C000 2976h***				
[9:0]	R/W	**MLC_SPU_DELAY_VAL**	SPU decode start delay. The actual sub-picture decode operation is initiated after the cycle delay the number of this register value from Vsync.	0
Sub-Picture Base Information Start Address (MLC_SPU_BASEI_ADDR) ***Address : C000 2978h / C000 297Ah***				
[31:0]	R/W	**MLC_SPU_BASEI_ADDR**	Base command information의 start address	0
Sub-Picture Highlight Information Start Address (MLC_SPU_HLI_ADDR) ***Address : C000 297Ch / C000 297Eh***				
[31:0]	R/W	**MLC_SUP_HLI_ADDR**	Highlight command information start address	0
Sub-Picture Palette (MLC_SPU_PAL) ***Address : C000 2980h ~ C000 29BEh***				
If an Address is the multiple of four (ex. 2980h, 2984h,,,), RG palette 16 bit data.				
If an Address is not the multiple of four (ex. 2982h, 2986h,,,), B palette 8 bit data.				

TABLE 13-99. MLC REGISTER LIST

CHAPTER 14

DISPLAY CONTROLLER

14. DISPLAY CONTROLLER

14.1 Overview

The Display Controller (DPC) creates signals and data to connect to external display devices. Such external devices are TFT LCD, Video Encoder, DAC, etc. The connection to external devices requires various kinds of Synchronized Signals and Data Formats. The DPC can be set to a variety of Modes according to the types of external display devices. In addition, this block creates signals to be used for the Display FIFO in the Multi Layer Controller (MLC).

Feature

- Support for Display sizes of up to 1024 x 768 pixels
- Programmable HSYNC/VSYNC generation
- Supports Composite Sync.
- Supports CCIR601 and CCIR656
- Supports YCbCr 3x8/3x10 Mode(CCUR656 Like)
- Supports DAC Interface
- Programmable polarity for all outputs (VD, DE, HSYNC,VSYNC,POL, FG, PS, XDOFF, STV, STH)
- Programmable pixel clock phase
- Supports RGB, Multiplexed RGB(MRGB), and YCbCr
- Programmable PAD Configuration for VD, HSYNC, DE

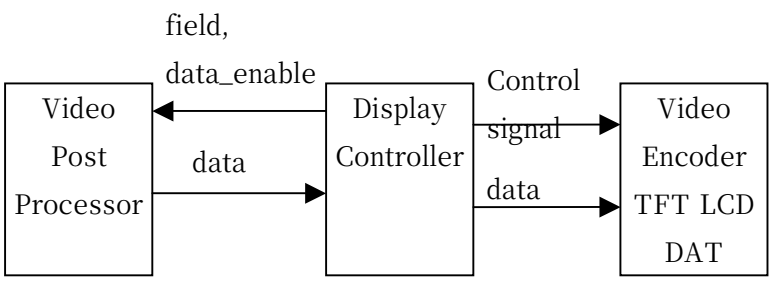


Figure 14-1. Display Controller.

14.2 Operation

14.2.1 Display Clock Control

The DPC has three Clock Sources. The First Clock emerges from the PLL and the Second Clock is entered from the outside directly. Finally, the Image Signal Processor (ISP) Clock can be used. In addition, the last clock is used for the DPC, synchronized with the ISP.

Once a clock source is determined, two clocks (CLK1 and CLK2) are created. The two created clocks are set differently according to the operation mode.

The following figure, 14-2, shows how CLK1 and CLK2 are controlled.

For RGB, one pixel per clock is transferred. Therefore, CLK1 and ClK2 have to be set as the same frequency. However, the MRGB and the CCIR656 transfer one pixel of data per two clocks. So, CLK2 has to be twice as fast as CLK1 in these cases.

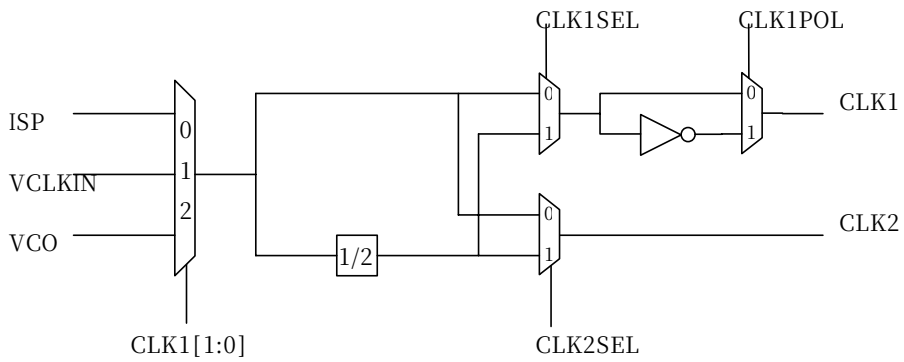


Figure 14-2. Display Controller Clock Control

Address : C000 2848h

Bit	R/W	Symbol	Description	Reset Value
[6]	R/W	**_656DATOUTEN**	656 Data Out Enable	0
[5]	R/W	**_656CLKOUTEN**	656 CLK Output Enable	0
[4:3]	R/W	**CLKSRC**	Display Source Clock 0 : ISP clock 1 : External Video Clock Input(VCLKIN). 2 : PLL,	0
[2]	R/W	**CLK2SEL**	CLK2 Selection (0: 1DCLK, 1:1/2DCLK)	0
[1]	R/W	**CLK1SEL**	CLK1 Selection(0: 1DCLK, 1:1/2DCLK)	0
[0]	R/W	**CLK1POL**	CLK1 polarity control. (0: Normal, 1: Inversion)	0

TABLE 14-1. CLOCK CONTROL REGISTER (DPC_CLKCNTL)

14.2.2 Horizontal Sync(HSYNC) Control

The HSYNC is determined by four parameters (T2,T3,T7, and T8) as shown in Figure 14.3.

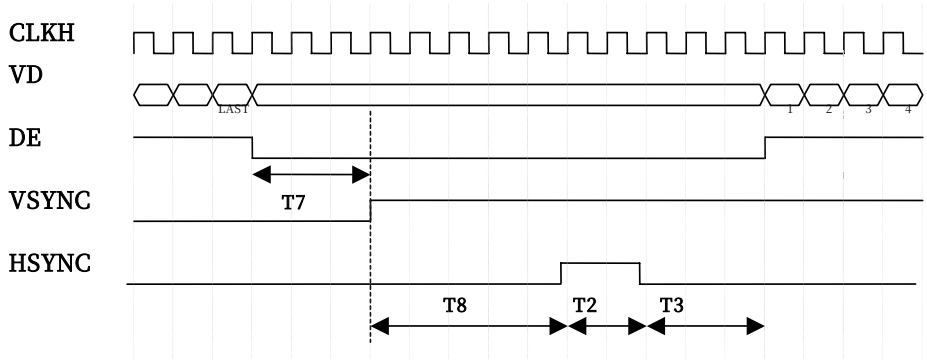


Figure 14-3. HSYNC Timing Diagram

T7 and T8 indicate the Front Porch of Horizontal Sync(FPHS). Especially, T7 shows the turning point of VSYNC between HSYNC and DE. T2 is the HSYNC width and T3 is the Back Porch of Horizontal Sync(BFHS). The following tables from 14-2 to 14-5 list the registers to be used for the parameter setting for T2, T3, T7 and T8.

The HSYNC Pin can be set to several kinds of Modes according to the types of external display devices. The HSYNC PAD Configuration is determined by the HSPADCFG setting in Table 14-2. If the HSPADCFG is set to '0', the HSYNC Pin is used as a horizontal sync signal.

Address : C000 281Ah

Bit	R/W	Symbol	Description	Reset Value
[10]	R/W	**SFTDIR**	Shift direction control for pixel data (0 : Right, 1 : Left)	1
[9:8]	R/W	**HSPADCFG**	HSYNC PAD Configuration. 2'b00 : HSYNC pin outputs horizontal sync signal(HSYNC). 2'b01 : HSYNC pin outputs the latch pulse(LP). 2'b10 : HSYNC pin outputs the Data Enable(DE) 2'b11 : HSYNC pin outputs the Composite Sync(CSYNC)	2'b00
[7:0]]	R/W	**T2(HSWID)**	HSYNC Width	0

TABLE 14-2. HSYNC WIDTH REGISTER (DPC_HS_WIDTH)

Address : C000 281Ch

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	T8(HSSTR)	HSYNC Start Position.	0

TABLE 14-3. HSYNC START REGISTER(DPC_HS_STR)

Address : C000 281Eh

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**T7(HSEND)**	HSYNC End position	0

TABLE 14-4. HSYNC END REGISTER(DPC_HS_END)

Address : C000 2826h

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th><th>Reset Value</th></tr>
<tr><td>[15:14]</td><td>R/W</td><td>DEPADCFG]</td><td>DE PAD Configuration.
Be caution. When DOF is 3x10 mode(DOF==3),DE outputs Cr[1].
<table>
<tr><th>DOF[1:0]</th><th>DESEL[1:0]</th><th>SIGNAL</th></tr>
<tr><td>3</td><td>Xx</td><td>Cr[1]</td></tr>
<tr><td>Xx</td><td>0</td><td>DE</td></tr>
<tr><td>Xx</td><td>1</td><td>STH</td></tr>
<tr><td>Xx</td><td>2</td><td>CSYNC</td></tr>
</table></td><td>0</td></tr>
<tr><td>[13]</td><td>R/W</td><td></td><td>Enable DE during blank area.</td><td>0</td></tr>
<tr><td>[12]</td><td>R/W</td><td>DEMOD</td><td>DE mode.
0 : Enable Mode 1: Pulse Mode</td><td>0</td></tr>
<tr><td>[11:4]</td><td>R/W</td><td>T3(DESTR)</td><td>DE Start position.</td><td>0</td></tr>
<tr><td>[3:0]</td><td>R/W</td><td>T14(DEWID)</td><td>STH Pulse Width (when DEMode = 1 and DESel = 0) (T14)
DE Delay (when DEMode = 0 and DESel = 0).
4’bxx00 0 delay
4’b0x01 +1 delay
4’b0x10 +2 delay
4’b0x11 +3 delay
4’b1x01 -1 delay
4’b1x10 -2 delay
4’b1x11 -3 delay</td><td>0</td></tr>
</table>

TABLE 14-5. DE CONTROL REGISTER(DPC_DE)

14.2.3 Vertical Sync(VSYNC) Control

The VSYNC is determined by T9, T10, and T11 parameters. T10 indicates the Front Porch of Vertical Sync(FPVS). T11 points out the Vertical Sync Width. T9 is the Vertical Blank Line Width. In other words, the Back Porch of vertical Sync(BFVS) can be designated using T9, T10 and T11. The timing diagram for the VSYNC is as shown in Figure 14-4. The following tables from 14-5 to 14-6 list the registers to set T9, T10 and T11.

Address : C000 2820h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**T10(VSSTR)**	VSYNC Start Position.	0
[7]	R/W	**VSFLDEN**	Vertical Sync Field Enable.	0
[6]	R/W	**VSFLDPOL**	Vertical Sync Field polarity.	0
[5:4]	R/W	**VSPADCFG**	VSYNC PAD Configuration. 2'b00 : FVSYNC pin outputs vertical sync signal(VSYNC). 2'b01 : FVSYNC pin outputs the start of First line(STV). 2'b1x : FVSYNC pin outputs the field.	2'b00
[3:0]	R/W	**T11(VSWID)**	VSYNC Width	0

TABLE 14-6. VERTICAL SYNC CONTROL REGISTER(DPC_V_SYNC)

Address : C000 2822h

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**NOSYMBNKFLD**	Select field has T9-1 Bank lines.	0
[14]	R/W	**NOSYMBNKLINE**	Each field has not same lines for blank lines.	0
[13]	R/W	**NOSYMATVLINE**	Select field has yMax[?] – 1 active lines	0
[12]	R/W	**NOSYMATVLINE**	Each field has not same lines for active lines	0
[11]	R/W	**SCANDIR**	Scan direction control for line data (0 : Down, 1 : Up)	1(UP)
[10]	R/W	**POLSTRLVL**	Toggle start level of POL per frame.	0
[9]	R/W		SMPTE 274M Interface Flag. (If its value is '1" in Interface Mode, the periods needed for the first field and the second field vertical syncs are different. The second field period is 1H longer than the first period.	0
[8:0]	R/W	**T9(VSEND)**	VSYNC End position.	0

TABLE 14-7. VERTICAL SYNC END REGISTER(DPC_VS_END)

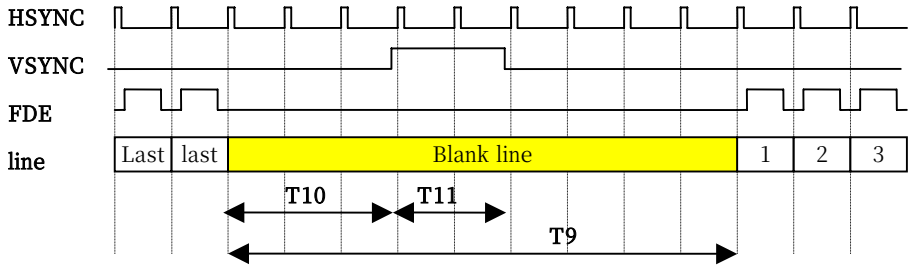


Figure 14-4. Vertical Sync Timing Diagram

14.2.4 Data Enable(DE) Control

According to the types of external display devices, the DE PAD can be set as Data Enable(DE), Start of Horizontal Pixel(STH), or Data Start Pulse. In addition, it can be used as the Composite Sync(CSYNC) output.

Registers to control the DE are listed in Table 14-5.The table has three Modes by the setting of the DEPADCFG and the DEMOD.

1. DE Mode (DEPADCFG=0, DEMOD=0)

This Mode is activated only when Pixel data is outgoing. In addition, a phase can be shifted from 3 pixels to –3 pixels at the base of the effective pixel. The phase is determined by the DEWID Register value in Table 14-5. The timing diagram on the DE Mode operation is as shown in Figure 14-5.

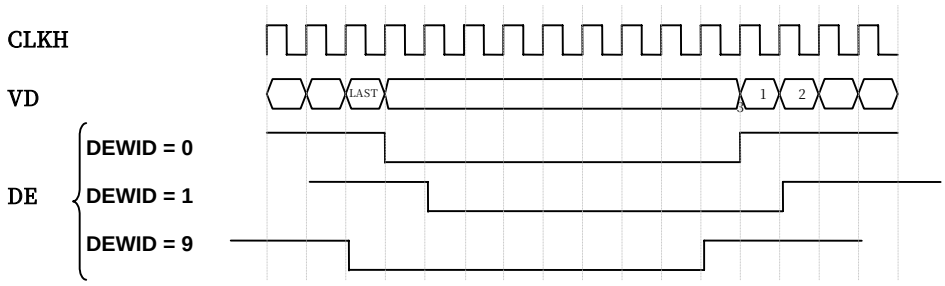


Figure 14-5. DE timing Diagram in the Data Enable Mode

2. STH Mode (DEPADCFG=1, DEMOD=0)

In STH Mode, the DE PAD generates a pulse on the verge of the first pixel data transmission. The timing diagram on the DE Mode operation is as shown in Figure 14-6.

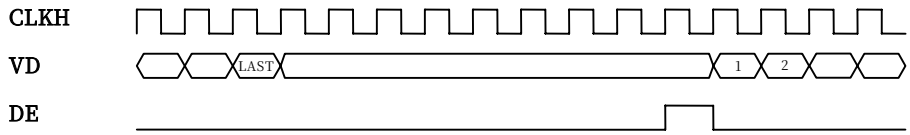


Figure 14-6. DE Timing Diagram in the STH Mode

3. PULSE Mode (DEPADCFG=0, DEMOD = 1)

In PULSE mode, a pulse is generated at the same time as the first pixel data transmission. The pulse width is determined by the DEWID Register value in Table 14-5. In other words, the DEWID is used to adjust the DE phase in the DE Mode or the Pulse width in the PULSE Mode. The adjustable maximum pulse width is 16 Pixel Clocks.

The timing diagram on the PULSE Mode operation is as shown in Figure 14-7.

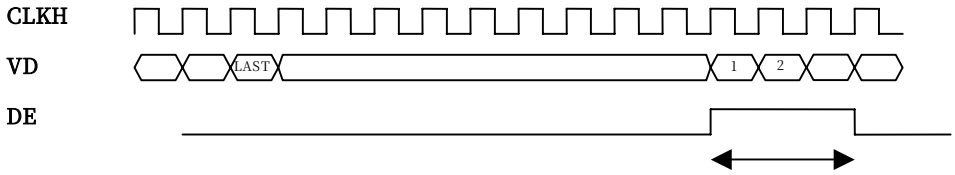


Figure 14-7. DE Timing Diagram in the PULSE Mode

4. When DEPADCFG =2, the CSYNC signal comes out through DE PAD.

14.2.5 Pixel Clock(CLKH) Control

The CLKH is the base clock used for the external display devices to read pixels. Therefore, the phase between Data and Pixel Data needs the adjustment under different circumstances. The CHPAHSE in Table 14-8 is used to control the CLKH phase. In addition, the CHPOL in Table 14-9 is used to reverse the CHLK Phase.

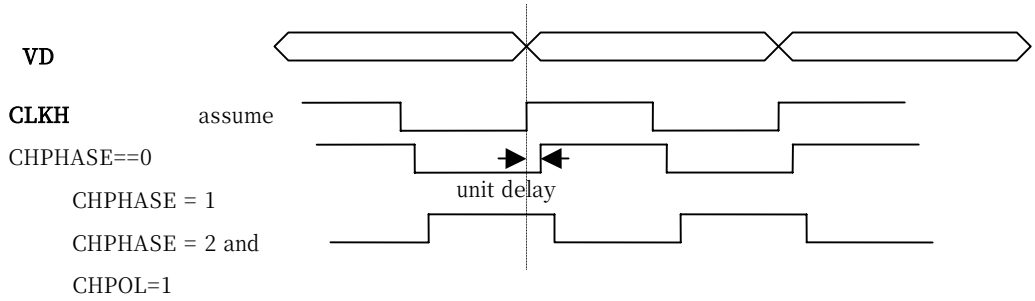


Figure 14-8 shows the Phase adjustment between the CLKH and a PIXEL Data

Figure 14-8. CLKH and Pixel Data

Address : C000 2802h

Bit	R/W	Symbol	Description	Reset Value
[15:13]	R/W	**CHPHASE**	Select the phase for CLKH	000b
[12]	R/W	**CHMSKBNK**	Mask pixel clock during blank area.	0b
[11:3]	R	**Reserved**	-	-
[2]	R/W	**PADSYNC**	Sync Enable for ALL PAD Output. 0 : bypass , 1 : 1 clock delay	0
[1]	R/W	**HSMSKBNK**	Mask HSYNC during the vertical blank	0b
[0]	R/W	**PADHZ**	Disable all PADs for LCDC(VD, CLKH,CLKV, DE, FHSYNC,FVSYNC)	0b

TABLE 14-8. PAD CONTROL REGISTER(DPC_FPICNTL)

Address : C000 2804h

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved.**	-	-
[9]	R/W	**FLDPOL**	Polarity control for field signal.	0
[8]	R/W	**POLPOL**	Polarity control for POL/o_Y[0]	0b
[7]	R/W	**XDOFFPOL**	Polarity control for XDOFF_BLANK/o_Y[1]	0b
[6]	R/W	**PSPOL**	Polarity control for PS /o_Cb[0]	0b
[5]	R/W	**CVPOL**	Polarity control for CLKV/o_Cb[1]	0b
[4]	R/W	**CHPOL**	Polarity control for CLKH	0b
[3]	R/W	**FGPOL**	Polarity control for FG_SYNCT/o_Cr[0]	0b
[2]	R/W	**DEPOL**	Polarity control for DE/o_Cr[1]	0b
[1]	R/W	**HSPOL**	Polarity control for HSYNC	0b
[0]	R/W	**VSPOL**	Polarity control for VSYNC	0b

TABLE 14-9. PAD POLARITY CONTROL REGISTER(DPC_FPIPOL1)

14.2.6 Active Display Size

The Display Size can be adjusted up to 2048 X 2048 in maximum. However, the real Display Size is determined by the system memory bandwidth used. Display Sizes are designated by T12 and T13.

In Interlace Mode, the Display Size has to be designated to half of the Active Display Size in the vertical direction since the Interlace Mode sends even fields and odd fields respectively.

Registers to be used for the setting of T12 and T13 are listed in Table 14-10 and Table 14-11.

Address : C000 2816h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**T12(XMAX)**	X width	719

TABLE 14-10. ACTIVE HORIZONTAL WIDTH (DPC_X_MAX)

Address : C000 2818h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**T13(YMAX)**	Y width	479

TABLE 14-11. ACTIVE VERTICAL HEIGHT (DPC_Y_MAX)

14.2.7 Video Data Bus(VD) Configuration

To transmit Data to external display devices, there are a total of 30 bits allocated. Out of these bits, 24 bits are allocated in the VD and the remaining are used with control signals. The 24-bit Data Bus is set to various Modes according to external devices.

Table 14-12 shows the VD setting in accordance with the types of Data.

DOF	0	1	2	3
RGB	4:4:4	5:6:5	6:6:6	8:8:8
MRGB	5:5:5	5:6:5	8:8:8a	8:8:8b
YCbCr	CCIR656	CCIR601	3 x 8 Mode	3 x 10 Mode

TABLE 14-12. BUS SETTING IN ACCORDANCE WITH THE TYPES OF DATA

Registers to be used for the setting of DOF and DOT are listed in Table 14-13.

Address : C000 2800h

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**SLVHV**	Slave Sync Mode 0: HSYNC & FIELD, 1: HSYNC & VSYHC…..	0
[14]	R/W	**SLVAE**	Slave mode 0 : Master mode, 1: Slave mode	0b
'[13]	R/W	**CSYNC**	Composite SYNC Mode	
[12]	R/W	**PAL**	NTSC/PAL Mode.	
[11]	R/W	**CISCYNC**	Get sync signal form ISP	0b
[10]	R/W	**HDTV**	TV Type 0 : SDTV, 1: HDTV	0b
[9]	R/W	**ENC**	External Device Mode 0 : DAC, 1: TV Encoder	0b
[8]	R/W	**TVMODE**	TV Mode enable 0 : LCD, 1: TV	0b
[7:6]	R/W	**DOT**	Data Output Type 0 : RGB 1 : Multiplexed RGB(MRGB) 2 : YcbCr 3 : Reserved	00b
[5]	R/W	**INTERACE**	TV Interface Mode 0 : progressive mode, 1: interface mode	0b
[4]	R/W	**SYNCCBCR**	Add sync level for Cb and Cr in DAC mode(ENC=0).	0b
[3]	R/W	**ESAVEN**	EAV/SAV Insertion Enable. If /TvOutType is Digital, EAV/SAV is inserted to Data output. If, however, TvOutType is analog, Sysn signals are created using the level of output value instead of the EAV/SAV.	0bj
[2:1]	R/W	**DOF**	**Data Output Format** **DOF** | **0** | **1** | **2** | **3** **RGB** | **4:4:4** | **5:6:5** | **6:6:6** | **8:8:8** **MRGB** | **5:5:5** | **5:6:5** | **888a** | **888b** **YCbCr** | **CCIR656** | **CCIR601** | **3x8 Mode** | **3x 10Mode**	00b
[0]	R/W	**ENB**	LCDC Enable	0b

TABLE 14-13. DPC CONTROL REGISTER(DPC_CNTL)

1. VD Configuration in RGB Mode

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4:4:4													B3	B2	B1	B0	G3	G2	G1	G0	R3	R2	R1	R0
5:6:5									B	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R	R3	R2	R1	R0
6:6:6							B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0
8:8:8	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

TABLE 14-14. VD CONFIGURATION IN RGB MODE

2. VD Configuration in MRGB Mode

Out of 24 bits allocated in the VD, 12 bits are used in the MGRB Mode. Instead, 2 Clocks per pixel are required.

DOF	VD	11	10	9	8	7	6	5	4	3	2	1	0
5:5:5	1st					G5	G4	G3	B7	B6	B5	B4	B3
	2nd						R7	R6	R5	R4	R3	G7	G6
5:6:5	1st					G4	G3	G2	B7	B6	B5	B4	B3
	2nd					R7	R6	R5	R4	R3	G7	G6	G5
8:8:8a	1st	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	2nd	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
8:8:8b	1st	G4	G3	G2	B7	B6	B5	B4	B3	G0	B2	B1	B0
	2nd	R7	R6	R5	R4	R3	G7	G6	G5	R2	R1	R0	G1

TABLE 14-15. VD CONFIGURATION IN MGRB MODE

3. VD Configuration in YCbCr Mode

DOF	VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIR656	1																	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	2																	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	3																	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	4																	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
CIR601	1									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	2									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
3x8		CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
3x10		CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2

TABLE 14-16. VD CONFIGURATION IN YCBCR MODE

14.2.8 EAV/SAV

In the case of the CCIR565 or the CCIR601, a pin for Sync signal is not allocated. The Sync signal is transferred with Data via a Data pin. The Sync Signal is inserted in the front of or at the back of Valid Data in End of Active Video(EAV)/Start of Active Video(SAV) shape. The ENC and ESA VEN in Table 14-13 are set to '1', and EAV/SAV is inserted in the front of or at the back of Data.

The relation between Analog waveform and EAV/SAV is as shown in Figure 14.8.

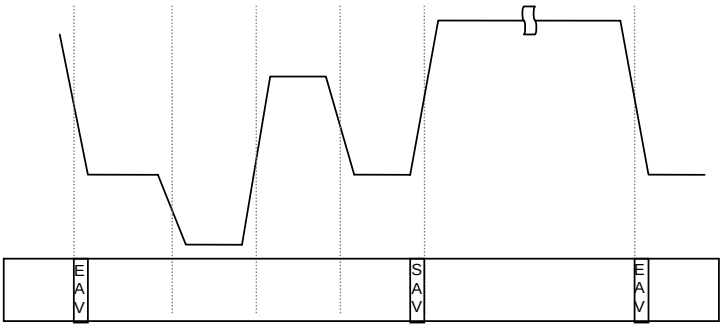


Figure 14-9. Relation Between EAV/SAV and Waveform

EAV/SAV code is made in accordance with Field(F), VSYNC(V) and HSYNC(H). The code values according to Field(F), VSYNC(V), HSYNC(H) are listed in Table 14-17.

Bit		9	8	7	6	5	4	3	2	1	0
Function		1	F	V	H	P3	P2	P1	P0	0	0
(FVH)	0	1	0	0	0	0	0	0	0	0	0
	1	1	0	0	1	1	1	0	1	0	0
	2	1	0	1	0	1	0	1	1	0	0
	3	1	0	1	1	0	1	1	0	0	0
	4	1	1	0	0	0	1	1	1	0	0
	5	1	1	0	1	1	0	1	0	0	0
	6	1	1	1	0	1	1	0	0	0	0
	7	1	1	1	1	0	0	0	1	0	0

TABLE 14-17. EAV/SAV CODE ACCORDING TO F,V,H

Code made by Table 14-17 is inserted into the part corresponding to CODE of Figure 14-9. In Figure 14-9, [FF,00,00,CODE] is used as a Video Timing Reference Code.

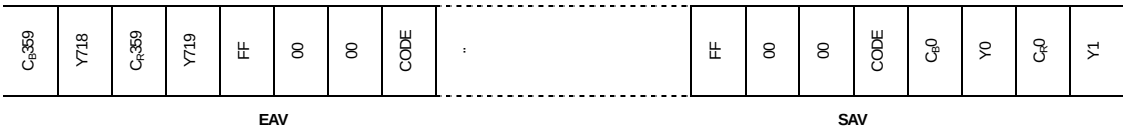


Figure 14-10. Data Stream format for 625 Line Systems.

14.2.9 Composite Sync(CSYNC)

To make Composite Sync (CSYNC), the CSYNC of Table 14-13 has to be set to '1'. As shown in Figure 14-11, the EQUALIZING PULSE and the SERRATION PULSE have to be created in the Vertical blank area.
The timings about the EQUALIZING PULSE and the SERRATION PULSE are as shown in Figure 14-11.

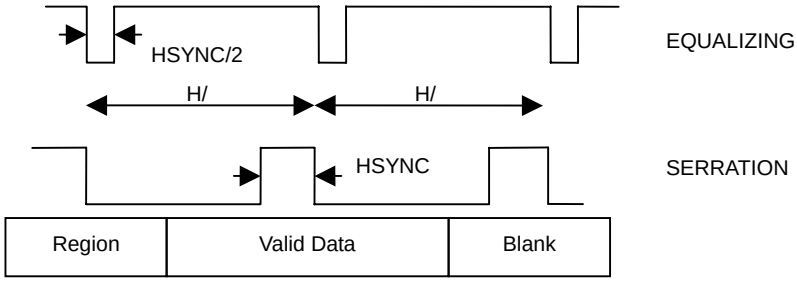


Figure. 14-11. Waveform for EQUALIZING and SERRATION PULSE

As shown in the figure above, the pulse width is determined by the HSYNC width (HSWID, Table 14-13). The pulse position in the middle of the line is determined by MIDSYNCPOS of Table 14-18. This value indicates the position of a valid data area.

Address : C000 2836h

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MIDSYNCPOS**	MID Sync Start position.	00

TABLE 14-18. CSYNC CONTROL REGISTER(DPC_MID_SYNC)

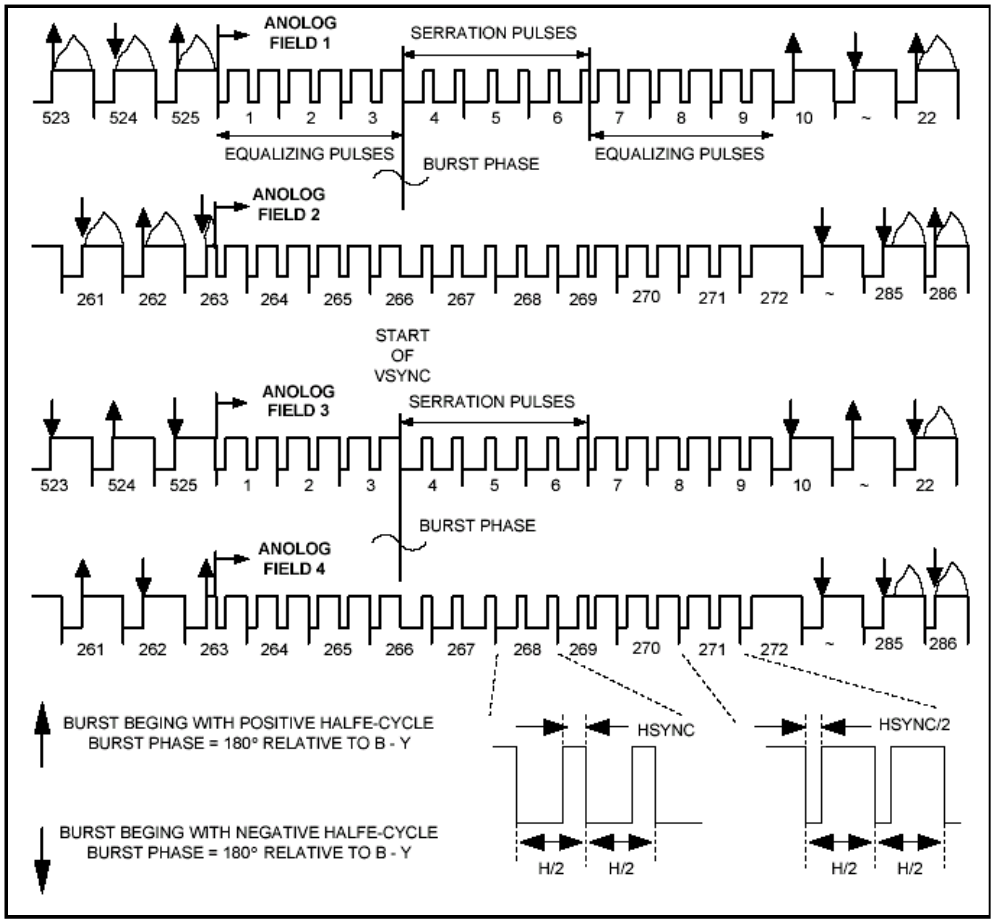


Figure 14-12. Waveform in 525 Line System

The CSYNC can be output through the HSYNC pin or the DE pin. The HSYNC pin is determined by the HSPADCFG value of Table 14-3 and the DE pin is determined by DEPADCFG value of Table 14-5. The following Figure shows the Pin configuration for the HSYNC pin and the DE pin.

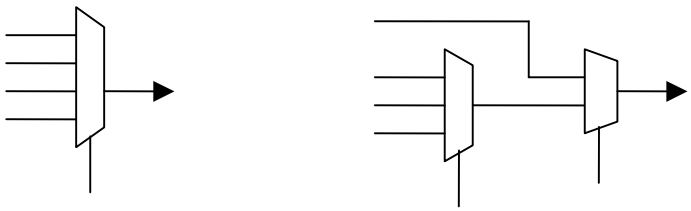


Figure 14-13. Pin Configuration for HSYNC and DE

14.2.10 DAC Interface(YPbPr)

When YPbPr is created via external DAC, Data to create the Sync and Data have to be output together. First, the ENC of Table 14-13 is set to '0' to indicate the Mode to connect to the DAC. In addition, the TVMOD is set to '1' since this Mode is used in only TV Mode. TVs receiving the YpbPr are grossly divided into HDTV and SDTV. They have different Sync signals respectively. The HDTV of Table 14-13 determines the Sync types.
Figure 14-13 shows the YPbPr Waveform for HDTV and SDTV.

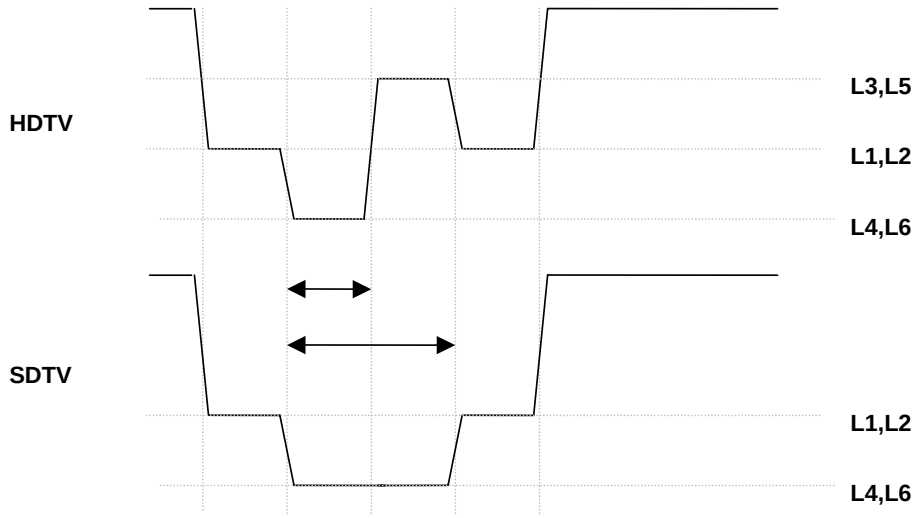


Figure 14-14. Sync Waveform for HDTV and SDTV

As shown in the figure above, three Levels (L1, L3, and L4 or L2, L5, and L6) form each sync signal. L1, L2 and L3 determine the sync levels about Y. In addition, L2, L5 and L6 determine the sync levels about PbPr. To put a sync signal into PbPr, the SYNCCBCR of Table 14-13 has to be set to '1'.
Registers to set each sync level are listed in tables from 14-19 to 14-24.

Address : C000 283Ah

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**L1(YBNKLVL)**	blank for Y.	252

TABLE 14-19. BLANK LEVEL FOR LUMINANCE(DPC_Y_BLANK)

Address : C000 283Ch

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**L2(CBNKLVL)**	blank for Cb or Cr.	212

TABLE 14-20. BLANK LEVEL FOR CHROMINAMCE (DPC_C_BLANK)

Address : C000 283Eh

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**L3(YPOSSYNCLVL)**	Positive Sync level for the luminance	748

TABLE 14-21. POSITIVE SYNC LEVEL FOR LUMINANCE(DPC_YP_CSYNC)

Address : C000 2840h

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**L4(YNEGSYNCLVL)**	Negative Sync level for the luminance	16

TABLE 14-22. NEGATIVE SYNC LEVEL FOR LUMINANCE(DPC_YN_CSYNC)

Address : C000 2842h

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**5(CPOSSYNCLVL)**	Positive Sync level for the chrominance	748

TABLE 14-23. POSITIVE SYNC LEVEL FOR CHROMINANCE(DPC_CP_CSYNC)

Address : C000 2844h

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R/W	**L6(CNEGSYNCLVL)**	Negative Sync level for the chrominance	276

TABLE 14-24. NEGATIVE SYNC LEVEL FOR CHROMINANCE(DPC_CN_CSYNC)

14.2.11 POL Control

The POL signal is used to control the polarity of a Source driver IC. This signal is toggled in the line of frame units.

In case of toggling of line units, the toggling zone of the signal can be an active data area or a blank area. The POLTGLAREA in Table 14-25 is used to indicate the toggling zone. If its value is '0', the POL signal is changed at an active data area. Otherwise, it is changed at a blank area. In addition, the position at each area is determined by the PLOTGLPOS in Table 14-25.

The PLO Signal Toggling Period is determined in line units by the POLPERIOD in Table 14-25. It can have a 4-line period maximum.

The POL signal can simultaneously toggle every frame as well as every line. For toggling in frame units, the PLOTGLEN in Table 14-26 is set to '1'. The lower part of Figure 14-14 shows the changing shape per frame as well as the toggling per line.

Address : C000 2832h

Bit	R/W	Symbol	Description	Resest Value
[15]	R/W	**POLEN**	POL Enable	
[14:13]	R/W	**POLPERIOD**	POL alternating period. (1 ~ 4 HD)	00
[12]	R/W	**POLTGLAREA**	POL transition zone	0
[11:0]	R/W	**T20(POLTGLPOS)**	POL toggle position.	0

TABLE 14-25. POL CONTROL REGISTER(DPC_POL)

Address : C000 2830h

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**POLTGLEN**	Vertical Toggling of POL	0
[14]	R	**Reserved**	-	-
[13]	R/W	**CVEN**	CLKV Enable.	0
[12]	R/W	**CVMSKBNK**	Disable CLKV during vertical blank time	0b
[11:0]	R/W	**T21**	CLKV falling edge position.	0

TABLE 14-26. CLKV CONTROL REGISTER(DPC_CLKVL)

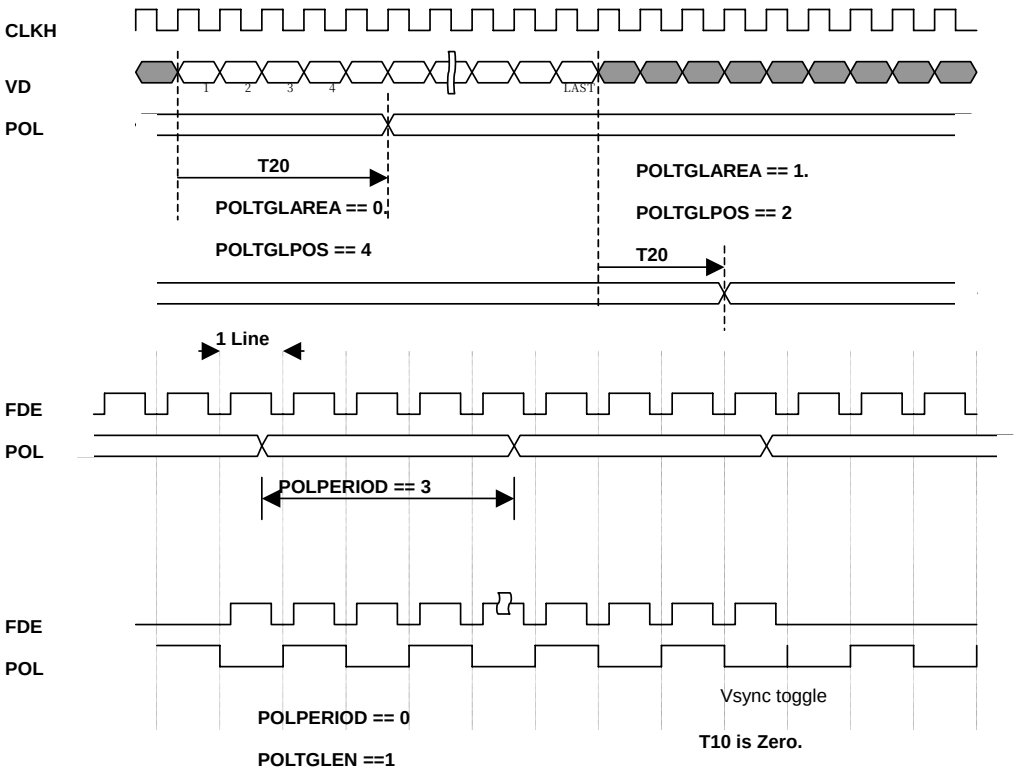


Figure 14-15. POL Waveform

14.2.12 CLKV Control

The CLCK signal is the shift clock for a Gate Driver IC. The waveform for the CLCK is as shown in Figure 14-16. As shown in the figure, the CLCK is determined by T21, T22 and CVATVAREA.

T21 determines the falling position. T22 and the CVATAREA determine the rising position.

In T21, the falling position is placed at the active area. In T22, the rising position can be placed at the active area or the blank area according to the CVATVAREA. As shown in the figure, when CVATVAREA=0, the rising is created at the active area. Otherwise, the rising is generated at the blank area.

Registers related to the CLKV are listed in Table 14-26 and Table 14-27.

Address : C000 282Eh

Bit	R/W	Symbol	Description	Reset Value
[15:13]	R/W	**CVDLY**	CLKV Delay	0
[12]	R/W	**CVATVAREA**	CLKV Active area	0
[11:0]	R/W	**T22(CVRISPOS)**	CLKV rising edge position	0

TABLE 14-27. CLKV CONTROL REGISTER(DPC_CLKVH)

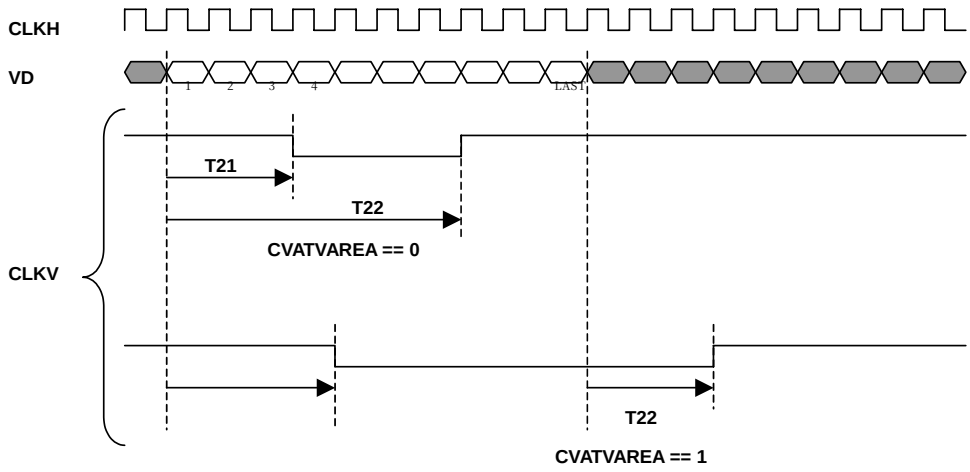


Figure 14-16. CLKV Waveform

14.2.13 LP Control

The LP signal is the latch pulse for a Source Drive IC. The Waveform for the LP signal is determined by 6 parameters (T2, T3, T4, T5, T7 and T8). Figure 14-17 shows the waveform for the LP and STH.

T4 determines the LP Pulse width.

T5 determines the LP Pulse starting position. This value indicates the starting position in clock units when the pulse starts after the last Pixel Data. Registers to set T4 and T5 are listed in Table 14-28.

T7 is used to determine the relation between the HSYNC and the VSYNC as explained in 14.2.2. Notice that the LP has to be within the T7 area. In other words, T4 + T5 < T7.

The HSYNC pin outputs the LP signal. Therefore, HSPADCFG has to be set to '1' as shown in Figure 14-12.

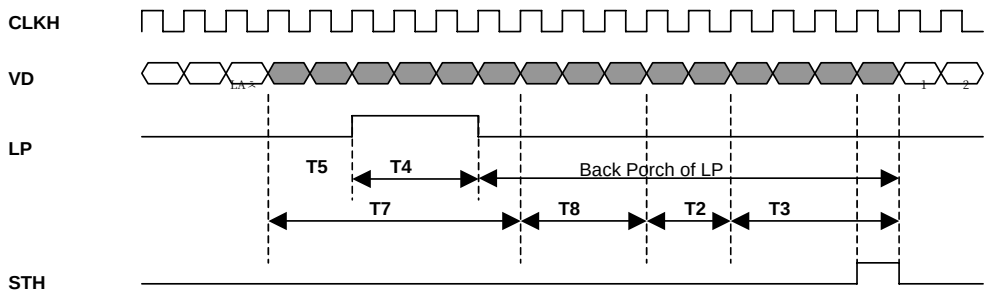


Figure 14-17. Waveform for LP and STH

Address : C000 282Ch

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R	**Reserved**	-	-
[13]	R/W	**LPEN**	LP Enable.	0
[12]	R/W		Disable the LP during blank area	0
[11:8]	R/W	**T5(LPSTR)**	LP start position	0
[7:0]	R/W	**T4(LPWID)**	LP Width	0

TABLE 14-28. LP CONTROL REGISTER(DPC_LP)

14.2.14 FG, XDOFF, and PS Control

The PS is the power save signal for a Source Driver IC. The signal shape is determined by T30 and T31. T30 determines the rising position at an active area, and T31 determines the falling position at a blank area.
Registers to be used to designate T30 and T31 are listed in Table 14-29.

The Waveform for PS is as shown in Figure 14-18.

Address : C000 2828h

Bit	R/W	Symbol	Description	Reset Value
[15:12]	R/W	**T31(PSEND)**	PS End position	0
[11:0]	R/W	**T30(PSSTR)**	PS Start position	0

TABLE 14-29. PS CONTROL REGISTER(DPC_PS)

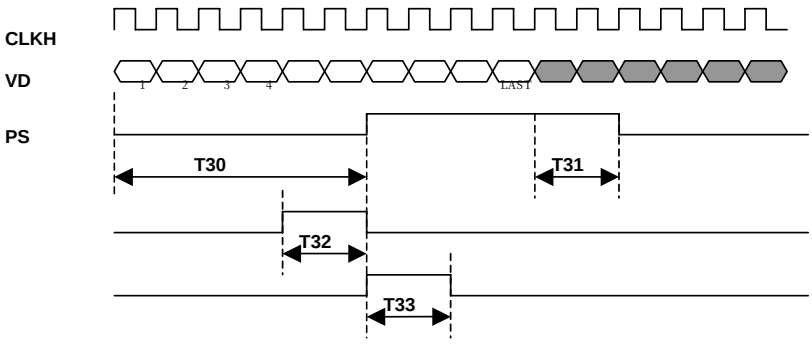


Figure 14-18. Waveform for PS, XDOFF and FG

The XDOFF is the Gate-off control signal for a Gate Driver IC. This signal generates a pulse in the front as much as T32 cycle from T30.
The FG is the clock signal for a Gate Drive IC. This signal generates a pulse at the back as much as T33 cycle from T30.
The relation among XDOFF, FG and PS are as shown in Figure 14-18.

Registers to designate T32 and T33 are listed in Table 14-30.

Address : C000 282Ah

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**PSEN**	Power Saving Enable	0
[14:9]	R	**Reserved**	-	-
[11:8]	R/W	**XDFPLSWID(T32)**	XDOFF pulse width	0
[7:4]	R	**Reserved**	-	-
[3:0]	R/W	**FGWID(T33)**	FG Width	0

TABLE 14-30. FG CONTROL REGISTER(DPC_FG)

14.2.15 Interrupt

When the HSYNC and the VSYNC are produced in the DPC, an interrupt can be initiated. In addition, each interrupt can be set to trigger at the first or the second edge of Sync.

This setting can be performed using the HSINTEDGE/VSINTEDGE in Table 14-31. Figure 14-19 shows when an interrupt initiated.

Once an interrupt is initiated, the VSINTFLAG and the HSINTFLAG in Table 14-31 are changed to '1'. The CPU can check the generation of the interrupt by reading the Flag. If the CPU completes the handling about the pertinent interrupt, the pertinent Flag has to be cleared. To clear the Flag, write '1', to the pertinent bit.

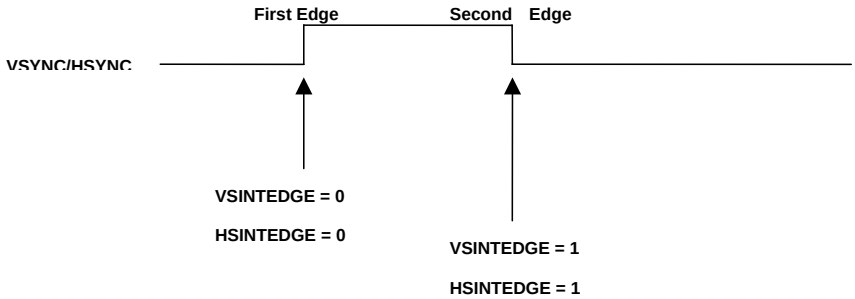


Figure 14-19. HSYNC/VSYNC Interrupt

Address : C000 2846h

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9]	R/W	**VSPLSSEL**	Output selection for ver_sync	
[8:6]	R	**Reserved**	-	-
5	R/W	**VSINTEN**	VSYNC Interrupt Enable	0
4	R/W	**HSINTEN**	HSYNC Interrupt Enable	0
3	R/W	**VSINTEDGE**	Interrupt position for VSYNC (0 : first edge, 1: second edge)	0
2	R/W	**HSINTEDGE**	Interrupt position for HSYNC (0 : first edge, 1: second edge)	0
1	R	**VSINTFLAG**	VSYNC Interrupt Status	0
0	R	**HSINTFLAG**	HSYNC Interrupt Status	0

TABLE 14-31. INTERRUPT CONTROL REGISTER(DPC_INTR)

14.3 Display Controller Registers LIST

Bit	R/W	Symbol	Description	Reset Value
DPC Control Register(DPC_CNTL) ***Address* : C000 2800h**				
[15]	R/W	**SLVHV**	Slave Sync Mode 0: HSYNC & FIELD, 1: HSYNC & VSYHC…..	0
[14]	R/W	**SLVAE**	Slave mode 0 : Master mode, 1: Slave mode	0b
'[13]	R/W	**CSYNC**	COMP SYNC Mode	
[12]	R/W	**PAL**	NTSC/PAL Mode	
[11]	R/W	**CISCYNC**	CIS Sync Mode	0b
[10]	R/W	**HDTV**	TV Type 0 : SDTV, 1: HDTV	0b
[9]	R/W	**ENC**	External Device Mode 0 : DAC, 1: TV Encoder	0b
[8]	R/W	**TVMODE**	TV Mode enable 0 : LCD, 1: TV	0b
[7:6]	R/W	**DOT**	Data Output Type 0 : RGB 1 : Multiplexed RGB(MRGB) 2 : YcbCr 3 : Reserved	00b
[5]	R/W	**INTERACE**	TV Interace Mode 0 : progressive mode, 1: interace mode	0b
[4]	R/W	**SYNCCBCR**	Add sync level for Cb and Cr in DAC mode(ENC=0)	0b
[3]	R/W	**ESAVEN**	EAV/SAV Insertion Enable. If /TvOutType is Digital, EAV/SAV is inserted to Data output. If, however, TvOutType is analog, Sysn signals is created using the level of output value instead of the EAV/SAV.	0bj
[2:1]	R/W	**DOF**	**Data Output Format** **DOF** / **0** / **1** / **2** / **3** **RGB** / **4:4:4** / **5:6:5** / **6:6:6** / **8:8:8** **MRGB** / **5:5:5** / **5:6:5** / **888a** / **888b** **YCbCr** / **CCIR656** / **CCIR601** / **3x8 Mode** / **3x 10Mode**	00b
[0]	R/W	**ENB**	LCDC Enable	0b
FPI Control Register(DPC_FPICNTL)				

Bit	R/W	Symbol	Description	Reset Value
***Address* : C000 2802h**				
[15:13]	R/W	**CHPHASE**	Select the phase for CLKH	000b
[12]	R/W	**CHMSKBNK**	Mask pixel clock during blank area	0b
[11:3]	R	**Reserved**	-	-
[2]	R/W	**PADSYNC**	Sync Enable for ALL PAD Output 0 : bypass , 1 : 1 clock delay	0
[1]	R/W	**HSMSKBNK**	Mask HSYNC during the vertical blank	0b
[0]	R/W	**PADHZ**	Disable all PADs for LCDC(VD, CLKH,CLKV, DE, FHSYNC,FVSYNC)	0b
FPI Polarity Control Register(DPC_FPIPOL1) ***Address* : C000 2804h**				
[15:10]	R	**Reserved.**	-	-
[9]	R/W	**FLDPOL**	Polarity control for field signal	0
[8]	R/W	**POLPOL**	Polarity control for POL/o_Y[0]	0b
[7]	R/W	**XDOFFPOL**	Polarity control for XDOFF_BLANK/o_Y[1]	0b
[6]	R/W	**PSPOL**	Polarity control for PS /o_Cb[0]	0b
[5]	R/W	**CVPOL**	Polarity control for CLKV/o_Cb[1]	0b
[4]	R/W	**CHPOL**	Polarity control for CLKH	0b
[3]	R/W	**FGPOL**	Polarity control for FG_SYNCT/o_Cr[0]	0b
[2]	R/W	**DEPOL**	Polarity control for DE/o_Cr[1]	0b
[1]	R/W	**HSPOL**	Polarity control for HSYNC	0b
[0]	R/W	**VSPOL**	Polarity control for VSYNC	0b
FPI Polarity Control Register 2(DPC_FPIPOL2) ***Address* : C000 2806h**				
[15:8]	R/W	**GREENPOL**	Polarity control for Green/Y [7:0]	0b
[7:0]	R/W	**BLUEPOL**	Polarity control for Blue/Cb[7:0]	**0b**
FPI Polarity Control Register 3(DPC_FPIPOL3) ***Address* : C000 2808h**				
[15:8]	R	**Reserved.**	-	0b
[7:0]	R/W	**REDPOL**	Polarity control for Red/Pr[7:0]	0b
FPI Enable Control Register 1(DPC_FPIATV1) ***Address* : C000 280Ah**				

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved.**	-	-
[9]	R	**FLDATV**	Enable control for field	0
[8]	R/W	**POLATV**	Enable control for POL/o_Y[0]	0b
[7]	R/W	**XDOFFATV**	Enable control for XDOFF_BLANK/o_Y[1]	0b
[6]	R/W	**PSATV**	Enable control for PS /o_Cb[0]	0b
[5]	R/W	**CVATV**	Enable control for CLKV/o_Cb[1]	0b
[4]	R/W	**CHATV**	Enable control for CLKH	0b
[3]	R/W	**FGATV**	Enable control for FG_SYNCT/o_Cr[0]	0b
[2]	R/W	**DEATV**	Enable control for DE/o_Cr[1]	0b
[1]	R/W	**HSATV**	Enable control for HSYNC	0b
[0]	R/W	**VSATV**	Enable control for VSYNC	0b
FPI Enable Control Register 2(DPC_FPIATV2) ***Address* : C000 280Ch**				
[15:0]	R/W	**VD1ATV**	Enable control for VD[15:0]	0
FPI Enable Control Register 3(DPC_FPIATV3) ***Address* : C000 280Eh**				
[15:8]	R		Reserved	0
[7:0]	R/W	**VD2ATV**	Enable control for VD[23:16]	0
Active Width Register (DPC_X_MAX) ***Address* : C000 2816h**				
[11:0]	R/W	**T12(XMAX)**	X width	719
Active Height Register (DPC_Y_MAX) ***Address* : C000 2818h**				
[11:0]	R/W	**T13(YMAX)**	Y width	479
HSYNC Width Register(DPC_HS_WIDTH) ***Address* : C000 281Ah**				
[10]	R/W	**SFTDIR**	Shift direction control for pixel data (0 : Right, 1 : Left)	1
[9:8]	R/W	**HSPADCFG**	HSYNC PAD Configuration. 2'b00 : HSYNC pin outputs horizontal sync signal(HSYNC). 2'b01 : HSYNC pin outputs the latch pulse(LP). 2'b10 : HSYNC pin outputs the Data Enable(DE) 2'b11 : HSYNC pin outputs the Composite Sync(CSYNC)	2'b00

Bit	R/W	Symbol	Description	Reset Value
[7:0]]	R/W	**T2(HSWID)**	HSYNC Width	0
HSYNC Start Register(DPC_HS_STR) ***Address* : C000 281Ch**				
[7:0]	R/W	**T8(HSSTR)**	HSYNC Start Position.	0
HSYNC End Register(DPC_HS_END) ***Address* : C000 281Eh**				
[7:0]	R/W	**T7(HSEND)**	HSYNC End position	0
VSYNC Control Register(DPC_V_SYNC) ***Address* : C000 2820h**				
[15:8]	R/W	**T10(VSSTR)**	VSYNC Start Position	0
[7]	R/W	**VSFLDEN**	Vertival Sync Field Enable.	0
[6]	R/W	**VSFLDPOL**	Vertival Sync Field polarity	0
[5:4]	R/W	**VSPADCFG**	VSYNC PAD Configuration. 2'b00 : FVSYNC pin outputs vertical sync signal(VSYNC). 2'b01 : FVSYNC pin outputs the start of First line(STV). 2'b1x : FVSYNC pin outputs the field.	2'b00
[3:0]	R/W	**T11(VSWID)**	VSYNC Width	0
VSYNC End Register(DPC_V_END) ***Address* : C000 2822h**				
[15]	R/W	**NOSYMBNKFLD**	Select field has T9-1 Bank lines.	0
[14]	R/W	**NOSYMBNKLINE**	Each field has not same lines for blank lines.	0
[13]	R/W	**NOSYMATVLINE**	Select field has yMax – 1 active lines.	0
[12]	R/W	**NOSYMATVLINE**	Each field has not same lines for active lines.	0
[11]	R/W	**SCANDIR**	Scan direction control for line data (0 : Down, 1 : Up)	1(UP)
[10]	R/W	**POLSTRLVL**	Toggle start level of POL per frame.	0
[9]	R/W		SMPTE 274M Interface Flag. (If its value is '1" in Interface Mode, the periods needed for the first field and the second field vertical syncs are different. The second field period is 1H longer than the first period.)	0
[8:0]	R/W	**T9(VSEND)**	VSYNC End position.	0
TV Blank End Register(DPC_TV-BNK) ***Address* : C000 2824h**				
[13:7]	R/W	**TVBNKSTR**	Blank Start position (Valid when TV mode is enabled.)	0

Bit	R/W	Symbol	Description	Reset Value
[6:0]	R/W	**TVBNKEND**	Blank End position (Valid when TV mode is enabled.)	0
DE Control Register (DPC_DE) ***Address* : C000 2826h**				
[15:14]	R/W	**DEPADCFG]**	DE PAD Configuration. Caution: When DOF is 3x10 mode(DOF==3),DE outputs Cr[1] **DOF[1:0] / DESel[1:0] / SIGNAL** **3 / xx / Cr[1]** **xx / 0 / DE** **xx / 1 / STH** **xx / 2 / CSYNC**	0
[13]	R/W		Enable DE during blank area	0
[12]	R/W	**DEMOD**	DE mode 0 : Enable Mode 1: Pulse Mode	0
[11:4]	R/W	**T3(DESTR)**	DE Start position.	0
[3:0]	R/W	**T14(DEWID)**	STH Pulse Width (when DEMode = 1 and DESel = 0) (T14). DE Delay (when DEMode = 0 and DESel = 0). 4'bxx00 0 delay 4'b0x01 +1 delay 4'b0x10 +2 delay 4'b0x11 +3 delay 4'b1x01 -1 delay 4'b1x10 -2 delay 4'b1x11 -3 delay	0
PS Control Register (DPC_PS) ***Address* : C000 2828h**				
[15:12]	R/W	**T31(PSSTR)**	PS End position	0
[11:0]	R/W	**T30(PSEND)**	PS Start position	0
FG Control Register (DPC_FG) ***Address* : C000 282Ah**				
[15]	R/W	**PSEN**	Power Saving Enable	0
[14:9]	R		Reserved	0
[11:8]	R/W	**XDFPLSWID**	XDOFF pulse width	0
[7:4]	R		Reserved	0

Bit	R/W	Symbol	Description	Reset Value
[3:0]	R/W	**FGWID**	FG Width	0
LP Control Register (DPC_LP) ***Address* : C000 282Ch**				
[15:14]	R	**Reserved**	-	**-**
[13]	R/W	**LPEN**	LP Enable	0
[12]	R/W	**LPActive**	Disable the LP during blank area	0
[11:8]	R/W	**T5(LPSTR)**	LP start position	0
[7:0]	R/W	**T4(LPWID)**	LP Width	0
CLKV Control Register 1(DPC_CLKVH) ***Address* : C000 282Eh**				
[15:13]	R/W	**CVDLY**	CLKV Delay	0
[12]	R/W	**CVATVAREA**	CLKV Active area	0
[11:0]	R/W	**T22(CVRISPOS)**	CLKV rising edge position	0
CLKV Control Register 2(DPC_CLKVL) ***Address* : C000 2830h**				
[15]	R/W	**POLTGLEN**	Vertical Toggling of POL	0
[14]	R	**Reserved**	-	-
[13]	R/W	**CVEN**	CLKV Enable	0
[12]	R/W	**CVMSKBNK**	Disable CLKV during vertical blank time	0b
[11:0]	R/W	**T21**	CLKV falling edge position	0
POL Control Register(DPC_POL) ***Address* : C000 2832h**				
[15]	R/W	**POLEN**	POL Enable	
[14:13]	R/W	**POLPERIOD**	POL alternating period. (1 ~ 4 HD)	00
[12]	R/W	**POLTGLAREA**	POL transition zone	0
[11:0]	R/W	**T20(POLTGLPOS)**	POL toggle position	0
CIS Sync Control Register(DPC_CISSYNC) ***Address* : C000 2834h**				
[9:0]	R/W	**T30(CISDLY)**	CIS Sync Delay (1~1024 clocks)	00
CSYNC Control Register DPC_MID_SYNC) ***Address* : C000 2836h**				

Bit	R/W	Symbol	Description	Reset Value
[11:0]	R/W	**MIDSYNCPOS**	MID Sync Start position	00
CSYNC Control Register DPC_C_SYNC) ***Address* : C000 2838h**				
[11:0]	R/W	**CSYNCPOS**	C Sync Start position	00
Blank Level for Luminance(DPC_Y_BLANK) ***Address* : C000 283Ah**				
[9:0]	R/W	**L1(YBNKLVL)**	blank for Y.	252
Blank Level for Chrominance(DPC_C_BLANK) ***Address* : C000 283Ch**				
[9:0]	R/W	**L2(CBNKLVL)**	blank for Cb or Cr.	512
Positive Sync Level for Luminance(DPC_YP_CSYNC) ***Address* : C000 283Eh**				
[9:0]	R/W	**L3(YPOSSYNCLVL)**	Positive Sync level for the luminance	748
Negative Sync Level for Luminance(DPC_YN_CSYNC) ***Address* : C000 2840h**				
[9:0]	R/W	**L4(YNEGSYNCLVL)**	Negative Sync level for the luminance	16
Positive Sync Level for Luminance(DPC_CP_CSYNC) ***Address* : C000 2842h**				
[9:0]	R/W	**L5(CPOSSYNCLVL)**	Positive Sync level for the chrominance	748
Negative Sync Level for Lumainance(DPC_CN_CSYNC) ***Address* : C000 2844h**				
[9:0]	R/W	**L6(CNEGSYNCLVL)**	Negative Sync level for the chrominance	276
Interrupt Controller Register (DPC_INTR) ***Address* : C000 2846h**				
[9]	R/W	**VSPLSSEL**	Output selection for ver_sync	
[8]	R	**Reserved**	-	-
[7]	R	**Reserved**	-	-
6	R	**Reserved**	-	-
5	R/W	**VSINTEN**	VSYNC Interrupt Enable	0
4	R/W	**HSINTEN**	HSYNC Interrupt Enable	0
3	R/W	**VSINTEDGE**	Interrupt position for VSYNC (0 : first edge, 1: second edge)	0
2	R/W	**HSINTEDGE**	Interrupt position for HSYNC (0 : first edge, 1: second edge)	0

Bit	R/W	Symbol	Description	Reset Value
1	R	**VSINTFLAG**	VSYNC Interrupt Status	0
0	R	**HSINTFLAG**	HSYNC Interrupt Status	0
Clock Controller Register (DPC_CLKCNTL) ***Address* : C000 2848h**				
[6]	R/W	**_656DATOUTEN**	656 Data Out Enable	0
[5]	R/W	**_656CLKOUTEN**	656 CLK Output Enable	0
[4:3]	R/W	**CLKSRC**	Display Source Clock 0 : ISP 1 : External Video Clock Input(VCLKIN). 2 : PLL	0
[2]	R/W	**CLK2SEL**	DClk2 Selection (0: 1DCLK, 1:1/2DCLK)	0
[1]	R/W	**CLK1SEL**	DClk1 Selection(0: 1DCLK, 1:1/2DCLK)	0
[0]	R/W	**CLK1POL**	DClk1 polarity control. (0: Normal, 1: Inversion)	0

TABLE 14-32. DISPLAY COTROLLER REGISTERS LIST

CHAPTER 15

2D GRAPHIC ACCELERATOR

15. 2D GRAPHIC ACCELERATOR

15.1 OVERVIEW

MP2520F has a 2D Graphic Controller to accelerate the GUI performance and is optimized in the O/S with various Graphic bases such as Windows CE or Linux.

- 32-deep source image FIFO
- Dual-bank Command Register Set provides efficient interface between CPU and graphics controller
- Hardware support for font color expansion, font caching, and image caching
- Graphic acceleration support for 16 bits per pixel mode
- Graphic acceleration functions include:
  - Rectangular source-copy block transfer (BitBLTs)
  - Transparent source-copy BitBLTs
  - Masked source-copy BitBLTs
  - Monochrome-to-color expansion on source and pattern data
  - Pattern and Rectangle Fills
  - 256 Raster Operations (ROPs)

When the direction of the screen is changed, RGB ROTATION rotates the detailed components on the screen. The ROTATION rotates selected shapes by 0, 90, 180 or 270 degrees and its BIT PER PIXEL (BPP) is 8, 16 or 24 bits.

15.2 OPERATIONS

15.2.1. Raster-Ops

A Raster operation (Raster-Op or ROP) is a graphic operation that is performed on a rectangular array of pixels. The 2D Graphic Controller supports 3-operand (source, pattern, destination). And Its operand is capable of supporting all most raster operations as defined for operating system based on GUI.

Below are basically provided ROPs.

- Bit Block-Level Transfer (BitBLT) : move Rectangular region to other area.
- Area Fill : Fill Rectangular area with certain color.
- Pattern Fill : Fill certain Rectangular area with stored image in internal 8x8 Pattern Register.
- Memory-to-Screen Transfer : Copy data from Source image storing memory to display memory.

3 input source needed for operate ROP.

- Source Data : Source Data is located in memory which stores CPU generated image or in frame buffer which is allocated for physical memory. Source data in memory can be transferred through DMA or CPU. If it is physical memory mapped data, 2D Graphics controller can access memory directly. Source Data

could be either monochrome or color data. Monochrome source data expands to foreground or background.

- Pattern Data : Pattern Data is stored pattern register in 2D Graphics controller. The pattern Size of pattern register is 8x8. Pattern data could be either monochrome or color data. Monochrome source data expands to foreground or background.
- Destination Data : Destination Data must be stored in Display memory.

15.2.2. Transparency

Data through ROPs is designated as transparent. If the color is same as transparency color of 2D Graphics controller, it is not stored in memory. Transparency color function can be Enable/Disable by CPU.

15.2.3. Monochrome to Color Expansion

2D Graphic Controller support 8bit or 16bit per pixel. If Source Image or Pattern Image is Monochrome(1BPP), Data is changed according to destination color format and ROP is performs. 2D Graphic Controller operates color expansion according to foreground and background color Register value in the Controller. If monochrome source image is font data, it can be used as font expansion in some O/S.

15.2.4. Fraction Control

2D Graphic controller performs 32bit pixel processing internally regardless color format of Source / Destination / Patter Image. Maximum performance can be maintained regardless color format through this function.

If image is not aligned as word(32bit), Fraction parameter should be set. Fraction parameter defines offset value of image by 32bit units.

Fraction parameter consists of 5bits and unit is bit.

For example,

When color format of Destination Image is 16bpp. Fraction parameter according to X coordinates of destination:

Fraction Parameter = (x%2)*16

When color format of Source Image is 1bpp. Fraction parameter according to X coordinates of Destination:

Fraction Parameter = (x%32)*1

15.2.5. FIFO Control

If source image data is stored in virtual address and/or cache of CPU, CPU should transfer source image data to source FIFO register of 2D graphics controller to operate ROPs.

Transferred data should be units of word(32bit). The number of transferred data is defined by source image color format, coordinates of X axis and length of X axis.

Below is source FIFO transfer routine.

```
GRP2D_UTIL_PushFIFO(
        GRP2D_COLORFMT    ColorFormat,          // [in] Color Format.
        S32               Stride,               // [in] number of byte per line of Source region
        U32               Width, U32   Height,  // [in] Width and Height
        U32*              pVirAddr32,           // [in] Virtual Address of Image
        U32               Frac,                 // [in] Define Fraction value. (unit:: bit, 0~31)
        GRP2D_DIR         XDir                  // [in] Direction of x coordinates
)
{
```

```
        U32         x, y, NumOfWord, BitNum;
        U32*        pEdgeAddr;
        U32         *pReadAddr;

        if (XDir==GRP2D_DIR_POSITIVE )          BitNum= (int)Frac & 0x1f;
        else {
                    switch(ColorFormat) {
                    case GRP2D_COLORFMT_1BPP:   BitNum= ((S32)Frac-(Width-1)) & 0x1f;break;
                    case GRP2D_COLORFMT_8BPP:   BitNum= ((S32)Frac-(Width-1)*8) & 0x1f;        break;
                    case GRP2D_COLORFMT_16BPP:  BitNum= ((S32)Frac-(Width-1)*16) & 0x1f;       break;
                    default:                            MES_NEVER_GET_HERE();                  break;
                    }
        }

        switch(ColorFormat) {
        case GRP2D_COLORFMT_1BPP:   NumOfWord= (Width+31+BitNum)/32; break;
        case GRP2D_COLORFMT_2BPP:   NumOfWord= (Width*2+31+BitNum)/32;      break;
        case GRP2D_COLORFMT_8BPP:   NumOfWord= (Width*8+31+BitNum)/32;      break;
        case GRP2D_COLORFMT_16BPP:  NumOfWord= (Width*16+31+BitNum)/32;     break;
        default:                            MES_NEVER_GET_HERE();           break;
        }

        pEdgeAddr  = pVirAddr32;

        // Dummy Writing
        NumOfWord++;

        for (y=0; y<Height; y++) {
                    pReadAddr = (U32*)((U32)pEdgeAddr & 0xfffffffc);
                    if (XDir==GRP2D_DIR_POSITIVE) {
                                for (x=0; x<NumOfWord; x++) {
                                            GRP2D.SRCFIFO= *pReadAddr;
                                            pReadAddr++;
                                }
                    } else {
                                for (x=0; x<NumOfWord; x++) {
                                            GRP2D.SRCFIFO= *pReadAddr;
                                            pReadAddr--;
                                }
                    }
                    pEdgeAddr += Stride;
        }
}
```

15.2.6. Dual Register Set

Controller register of 2D graphics controller consists of 2 banks. 1 bank contains current working command and the other is for receiving new command.

From this register, CPU can set new command to register when graphic controller is rendering. It will upgrade performance by avoiding wait stage of CPU even during graphics controller's working. New command in register will not affect graphics controller before input of run command.

15.3. 2D GRAPHIC CONTROLLER REGISTER

Destination Control Register (MESGDSTCTRL)

Address : E002 0000h

Bit	R/W	Symbol	Description	Reset Value
31 : 7	R	**Reserved**	-	-
6	R/W	**DSTNB**	Reads the contents of the destination area and executes the ROP operation 0 : Disable 1 : Read Operation	0
5	R/W	**DSTBPP**	Points out the color format of the destination area 0 : 8bpp 1 : 16bpp	0
4 : 0	R/W	**DSTFRAC**	Unit bit	0

TABLE 15-1. DISPLAY COTROLLER REGISTERS LIST

Destination Address Register (MESGDSTADDR)

Address: E002 0004h

Bit	R/W	Symbol	Description	Reset Value
31 : 0	R/W	**MESGDSTADDR**	Points out the Base Address of the Destination Area	0h

TABLE 15-2. DESTINATION ADDRESS REGISTER (MESGDSTADDR)

Destination Stride Register (MESGDSTSTRIDE)

Address: E002 0008h

Bit	R/W	Symbol	Description	Reset Value
31 : 0	R/W	**MESGDSTSRIDE**	Determines the address increment corresponding to the increase of the Y coordinate in the Destination Area	0h

TABLE 15-3. DESTINATION STRIDE REGISTER (MESGDSTSTRIDE)

Source Control Register (MESGSRCCTRL)

Address: E002 000Ch

Bit	R/W	Symbol	Description	Reset Value
31 : 8	R	**Reserved**	-	-
8	R/W	**INVIDEO**	Indicates whether the Source image exists at Frame buffers 0 : Controlled by CPU 1 : Frame Buffer	
7	R/W	**SRCENB**	Determines the execution of ROP operation after reading the contents of the Source Image area	

Bit	R/W	Symbol	Description	Reset Value
			0 : Disable 1 : Read Operation	
6 : 5	R/W	**SRCBPP**	Indicates the color format of the Source Image area 00 : 8bpp 01 : 16bpp 10 : 1bpp	0
4 : 0	R/W	**SRCFRAC**	Unit bit	0

TABLE 15-4. SOURCE CONTROL REGISTER (MESGSRCCTRL)

Source Address Register (MESGSRCADDR)

Address: E002 0010h

Bit	R/W	Symbol	Description	Reset Value
31 : 0	R/W	**MESGSRCADDR**	Points out the Base Address of the Source Area	0h

TABLE 15-5. SOURCE ADDRESS REGISTER (MESGSRCADDR)

Source Stride Register (MESGSRCSTRIDE)

Address: E002 0014h

Bit	R/W	Symbol	Description	Reset Value
31 : 0	R/W	**MESGSRCSTRIDE**	Determines the Address increment corresponding to the increase of the Y coordinate in the Source Area	0h

TABLE 15-6. SOURCE STRIDE REGISTER (MESGSRCSTRIDE)

Source Foreground Color Register (MESGSRCFORCOLOR)

Address: E002 0018h

Bit	R/W	Symbol	Description	Reset Value
31 : 16	R	**Reserved**	-	-
15 : 0	R/W	**MESGFORCOLOR**	RGB5:6:5 Format Valid when the Source Image Color Format is 1-BPP	0

TABLE 15-7. SOURCE FOREGROUND COLOR REGISTER (MESGSRCFORCOLOR)

Source Background Color Register (MESGSRCBACKCOLOR)

Address: E002 001Ch

Bit	R/W	Symbol	Description	Reset Value
31 : 16	R	**Reserved**	-	-
15 : 0	R/W	**MESGBACKCOLOR**	RGB5:6:5 Format Valid when the Source Image Color Format is 1-BPP	0

TABLE 15-8. SOURCE BACKGROUND COLOR REGISTER (MESGSRCBACKCOLOR)

Pattern Control Register (MESGPATCTRL)

Address: E002 0020h

Bit	R/W	Symbol	Description	Reset Value
31 : 7	R	**Reserved**	-	-
6	R/W	**PATMONO**	Determines whether the pattern is Color or Mono. 0 : Color 1 : Mono	0
5	R/W	**PATENB**	Determines the use of the Pattern Image 0 : Disable 1 : Enable	0
4 : 3	R/W	**PATBPP**	Indicates the Color Format of the Pattern Image area. 00 : 8bpp 01 : 16bpp 10 : 1bpp	0
2 : 0	R/W	**YOFFSET**	Points out the Y Offset of the Pattern. Unit : Pixel	0

TABLE 15-9. PATTERN CONTROL REGISTER (MESGPATCTRL)

Pattern Foreground Color Register (MESGFORCOLOR)

Address: E002 0024h

Bit	R/W	Symbol	Description	Reset Value
31 : 16	R	**Reserved**	-	-
15 : 0	R/W	**MESGFORCOLOR**	RGB5:6:5 Format Valid when the Pattern Image Color Format is 1-BPP	0

TABLE 15-10. PATTERN FOREGROUND COLOR REGISTER (MESGFORCOLOR)

Pattern Background Color Register (MESGBACKCOLOR)

Address: E002 0028h

Bit	R/W	Symbol	Description	Reset Value
31 : 16	R	**Reserved**	-	-
15 : 0	R/W	**MESGBACK COLOR**	RGB5:6:5 Format Valid when the Pattern Image Color Format is 1-BPP	0

TABLE 15-11. PATTERN BACKGROUND COLOR REGISTER (MESGBACKCOLOR)

Size Register (MESGSIZE)

Address: E002 002Ch

Bit	R/W	Symbol	Description	Reset Value
31 : 27	R	**Reserved**	-	-
26 : 16	R/W	**HEIGHT**	Indicate the height of the area. Unit : Pixel	0
10 : 0	R/W	**WIDTH**	Indicate the width of the area. Unit : Pixel	0

TABLE 15-12. SIZE REGISTER (MESGSIZE)

Control Register (MESGCTRL)

Address: E002 0030h

Bit	R/W	Symbol	Description	Reset Value
31 : 16	R/W	**TRANSPARANCY COLOR**	Points out transparent color	-
15 : 12	R	**Reserved**	-	-
11	R/W	**TRANPARENCYENB**	Determines whether to check transparency color 0 : Disable 1 : Enable	0
10	R/W	**FFCLR**	Clears the Source Input FIFO	0
9	R/W	**YDIR**	Determines the Fill direction on the Y axis 0 : Negative 1 : Positive	0
8	R/W	**XDIR**	Determines the Fill direction along the X axis 0 : Negative 1 : Positive	0
7 : 0	R/W		Defines the 8-bit raster operation(ROP). All 256 possible ROPs are supported.	0

TABLE 15-13. CONTROL REGISTER (MESGCTRL)

Status Register (MESGSTATUS)

Address: E002 0034h

Bit	R/W	Symbol	Description	Reset Value
31 : 1	R	**Reserved**	-	-
0	R	**BUSY**	Shows the operation status of the 2D Graphic Engine 0 : Idle 1 : Busy	0

TABLE 15-14. STATUS REGISTER (MESGSTATUS)

FIFO Status Register (MESGFIFOSTATUS)

Address: E002 0038h

Bit	R/W	Symbol	Description	Reset Value
31	R	**FULL**	Informs whether the Source FIFO is full or not 0 : non-Full 1: Full	0
30 : 5	R	**Reserved**	-	-
4 : 0	R/W	**REMAIN**	Remain word of Source FIFO	0

TABLE 15-15. FIFO STATUS REGISTER (MESGFIFOSTATUS)

Source FIFO Register (MESGFIFO)

Address: E002 003Ch

Bit	R/W	Symbol	Description	Reset Value
31 : 0	W	**MESGFIFO**	Source FIFO Data	-

TABLE 15-16. SOURCE FIFO REGISTER (MESGFIFO)

Pattern Register (MESGPAT)

Address: E002 0080h ~ E002 00FCh

Bit	R/W	Symbol	Description	Reset Value
31 : 0	W	**MESGPAT**	Pattern Value	-

TABLE 15-17. PATTERN REGISTER (MESGPAT)

CHAPTER 16

IMAGE SIGNAL PROCESSOR

16. IMAGE SIGNAL PROCESSOR

16.1 OVERVIEW

The Image Signal Processor (ISP) of the MP2520F receives 6 types of Input format. It Gamma corrects using a RAM. It enhances Luminance by adjusting Contrast, Brightness and Edge, and enhances Chrominance by adjusting Hue and Saturation. In addition, it has functions for Clipping, Suppress, Auto focus, Auto Exposure and Auto White balance. Finally, it provides Clocks or Syncs to external Image sensors or they are provided from the outside.

FEATURES

- Input data format :
  - YCbCr 4:2:2 16-bit format (601)
  - ITU-R BT 656(CCIR656)8-bit
  - ITU-R BT 656(CCIR656) Like 8-bit
  - 8/10 bits Bayer RGB
  - 8/10 bits Serial RGB
  - 8 bits parallel RGB format.
- Bi-directional and polarity-selectable Clock and Sync signal.
- Auto focus
- Auto exposure
- Auto white balance
- Gamma control,
- Hue control, Color suppression by level.
- Contrast, Brightness Control
- Horizontal Edge Enhancement

BLOCK DIAGRAM

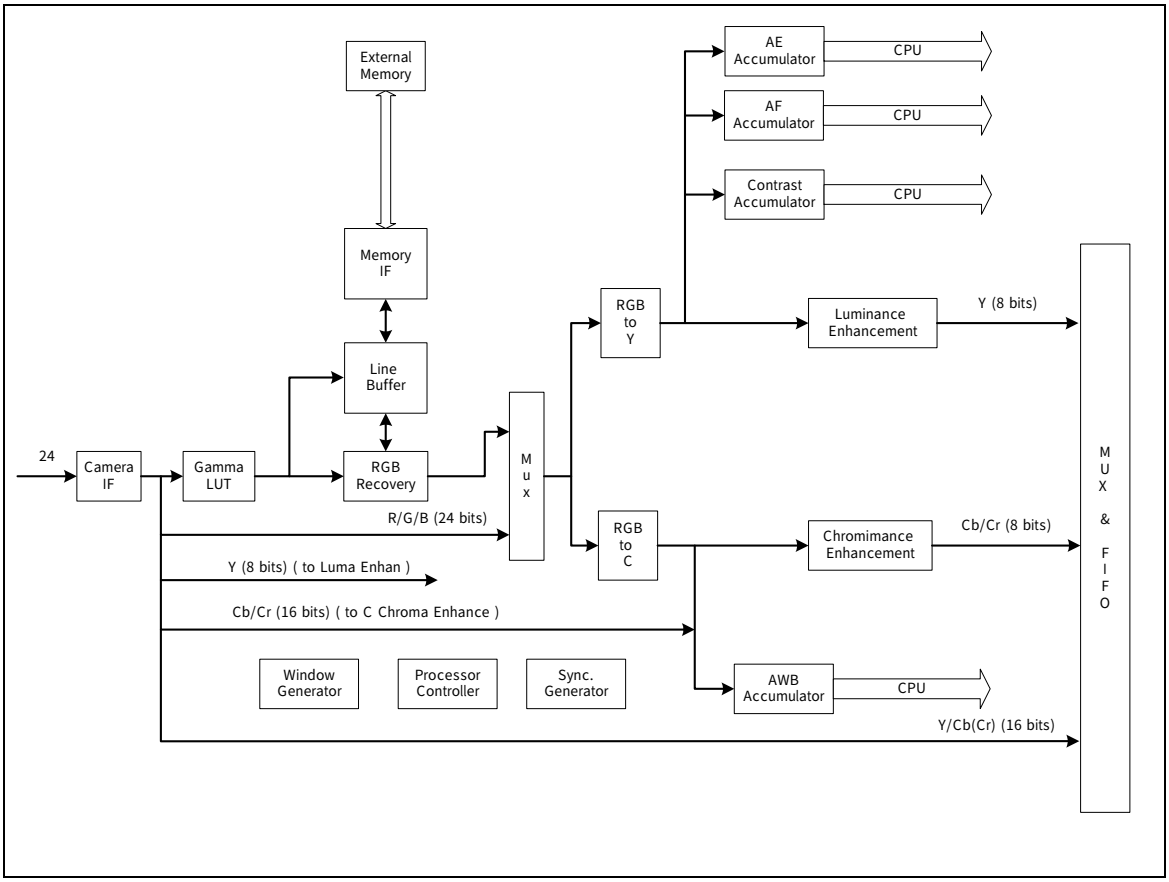


Figure 16-1. Image Signal Processor Block Diagram

16.2 OPERATION

16.2.1 Internal Signal Sync Generation

The ISP can receive Sync signals from the outside or provide them generated internally to the outside. In the data format of ITU_R BT656, the ISP receives Sync information from the outside and then creates Sync signals again. The ITU-R BT 656 data format does not have a Sync Pin, but its data have Sync information. The ISP writes values by the Falling Edge to the ISP_EAV2HSYNC register in Horizontal End Of Active Video (EAV). It generates Horizontal Sync by determining the time from the Falling Edge of Horizontal Period, Horizontal Sync, Pulse Width and Horizontal Sync to an Active signal and the Width of the Active Signal. In addition, it writes the values by the Falling Edge of Vertical Sync to the ISP_EAV2VSYNC register in Vertical EAV. On, It generates Vertical Sync by determining the time from the Falling Edge of Vertical Period, Vertical Sync,Pulse Width and Vertical Sync to an Active signal and the Width of the Active Signal. The unit of the Vertical Sync is Horizontal Line.

ISP Sync Control Register(ISP_VPERIOD)

Address : C000 3006h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_VPERIOD**	Vertical Sync Period. The unit is Horizontal sync. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x106

TABLE 16-1. SYNC CONTROL REGISTER(ISP_ VPERIOD)

ISP Sync Control Register(ISP_VPW)

Address : C000 3008h

Bit	R/W	Symbol	Description	Reset Value
[15:11]	R/W	**ISP_EAV2VSYNC**	Vertical EAV to Vertical Sync Starting point. The unit is Horizontal Sync. Effective when in CCIR655 mode.	0x00
[9:0]	R/W	**ISP_VPW**	Vertical Sync Pulse Width. The unit is Horizontal Sync. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x0A

TABLE 16-2. ISP SYNC CONTROL REGISTER(ISP_VPW)

ISP Sync Control Register(ISP_ HPERIOD)

Address : C000 300Ah

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**ISP_HPERIOD**	Horizontal Sync Period. The unit is ISP_CLK. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x187

TABLE 16-3. SYNC CONTROL REGISTER(ISP_ HPERIOD)

ISP Sync Control Register (ISP_ HPW)

Address : C000 300Ch

Bit	R/W	Symbol	Description	Reset Value
[15:9]	R/W	**ISP_EAV2HSYNC**	Horizontal EAV(End of Active Video) to Horizontal Sync Starting point. The unit is ISP_CLK. Effective when CCIR655 Mode.	0x10
[8:0]	R/W	**ISP_HPW**	Horizontal Sync Pulse Width. The unit is ISP_CLK. Effective when Sync output mode (ISP_SYNC_DIR = 1)	0x32

TABLE 16-4. SYNC CONTROL REGISTER(ISP_ HPW)

ISP Sync Control Register(ISP_HACT_ST)

Address : C000 300Eh

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_HACT_ST**	Horizontal Active Data Start Point from Falling Horizontal Sync.	0x0B

TABLE 16-5. SYNC CONTROL REGISTER(ISP_HACT_STW)

ISP Sync Control Register(ISP_H_WIDTH)

Address : C000 3010h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_H_WIDTH**	Horizontal active data end point from Horizontal Active Data Start Point	0x14B

TABLE 16-6. SYNC CONTROL REGISTER(ISP_H_WIDTH)

ISP Sync Control Register(ISP_VACT_ST)

Address : C000 3012h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	ISP_VACT_ST	Vertical Active Data Start Point from Falling Vertical Sync	0x0A

TABLE 16-7. SYNC CONTROL REGISTER(ISP_VACT_ST)

ISP Sync Control Register(ISP_V_HEIGHT)

Address : C000 3014h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	ISP_V_HEIGHT	Vertical Active Data End Point from Vertical Active Data Start Point	0x0FA

TABLE 16-8. SYNC CONTROL REGISTER(ISP_V_HEIGHT)

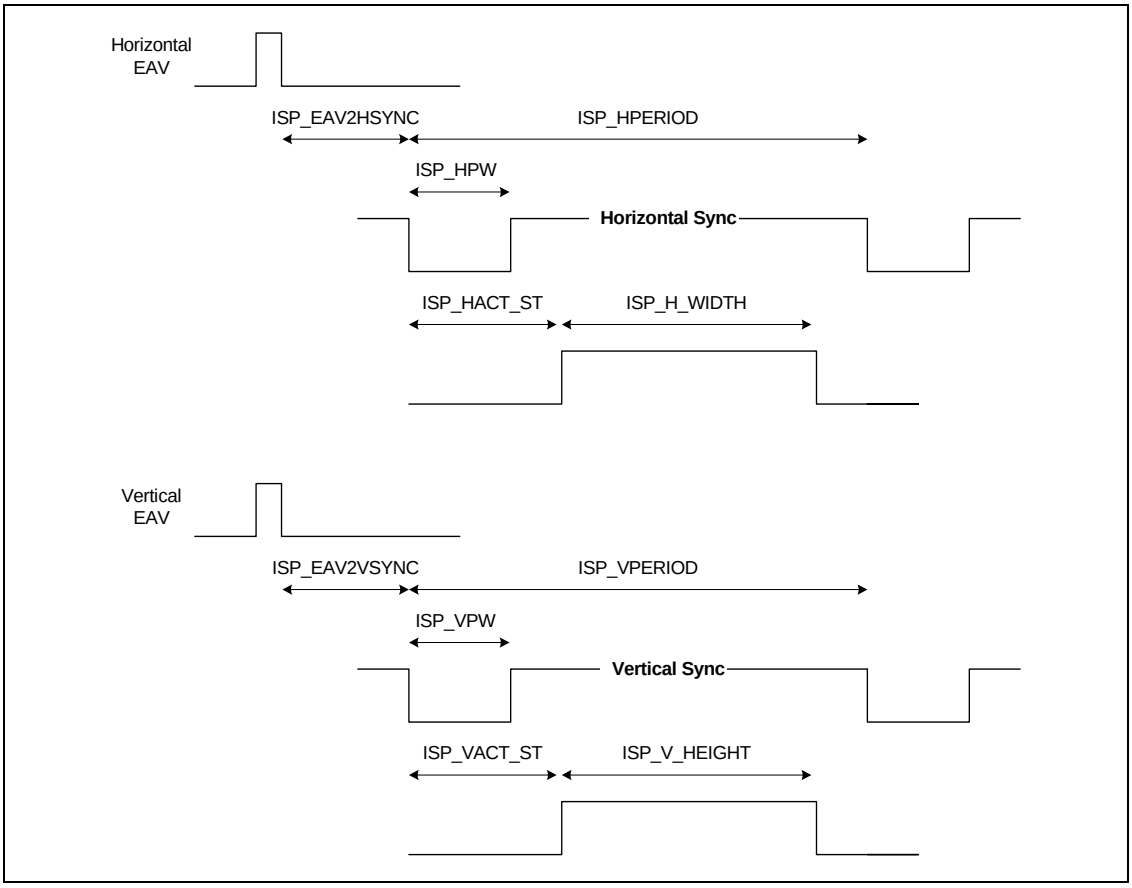


Figure 16-2. Image Signal Horizontal/Vertical Sync

16.2.2 Image Signal Window

The ISP allocates a region to every Sub-Block. Each Block operates at only its region. ISP_RGBSV, ISP_RGBEV, ISP_RGBSH and ISP_RGBEH determine the region to carry out Data entered from the outside. The region must be bigger than the actual Width and the actual Height. ISP_AESV, ISP_AEEV, ISP_AESH and ISP_AEEH are the regions for Auto Exposure. ISP_AFSV, ISP_AFEV, ISP_AFSH and ISP_AFEH are the regions for Auto Focus. ISP_VACT_ST, ISP_HEIGHT, ISP_HACT_ST and ISP_WIDTH are the regions for effective Data.

Processing Window Control Register(ISP_RGBSV)

Address : C000 3018h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_RGBSV**	Vertical Stating point of processing window from falling edge of Vertical Sync The unit is Horizontal Sync	0x05

TABLE 16-9. PROCESSING WINDOW CONTROL REGISTER(ISP_RGBSV)

Processing Window Control Register(ISP_RGBEV)

Address : C000 301Ah

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_RGBEV**	Vertical Ending point of processing window from falling edge of Vertical Sync The unit is Horizontal Sync	0xFF

TABLE 16-10. PROCESSING WINDOW CONTROL REGISTER(ISP_RGBEV)

Processing Window Control Register(ISP_RGBSH)

Address : C000 301Ch

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_RGBSH**	Horizontal Stating point of processing window from falling edge of Horizontal Sync The unit is ISP_CLK	0x05

TABLE 16-11. PROCESSING WINDOW CONTROL REGISTER(ISP_RGBSH)

Processing Window Control Register(ISP_RGBEH)

Address : C000 301Eh

Bit	R/W	Symbol	Description	Reset Value
[14:0]	R/W	**ISP_RGBEH**	Horizontal Ending point of processing window from falling edge of Horizontal Sync The unit is ISP_CLK	0x14F

TABLE 16-12. PROCESSING WINDOW CONTROL REGISTER(ISP_RGBEH)

Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESV)

Address : C000 3020h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AESV**	Vertical starting point for auto exposure/white balance accumulation from falling edge of Vertical Sync.	0x0A

TABLE 16-13. AUTO EXPOSURE/WHITE BALANCE ACCUMULATION WINDOW CONTROL REGISTER(ISP_AESV)

Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEV)

Address : C000 3022h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AEEV**	Vertical ending point for auto exposure/white balance accumulation from falling edge of Vertical Sync.	0x0FA

TABLE 16-14. AUTO EXPOSURE/WHITE BALANCE ACCUMULATION WINDOW CONTROL REGISTER(ISP_AEEV)

Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESH)

Address : C000 3024h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AESH**	Horizontal starting point for auto exposure/white balance accumulation from falling edge of Horizontal Sync.	0x0FA

TABLE 16-15. AUTO EXPOSURE/WHITE BALANCE ACCUMULATION WINDOW CONTROL REGISTER(ISP_AESH)

Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEH)

Address : C000 3026h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AEEH**	Horizontal ending point for auto exposure/white balance accumulation from falling edge of Horizontal Sync.	0x14A

TABLE 16-16. AUTO EXPOSURE/WHITE BALANCE ACCUMULATION WINDOW CONTROL REGISTER(ISP_AEEH)

Auto Focus Accumulation Window Control Register(ISP_ AFSV)

Address : C000 302Eh

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AFSV**	Vertical starting window point for auto focus accumulation from falling edge of Vertical Sync.	0x0A

TABLE 16-17. AUTO FOCUS ACCUMULATION WINDOW CONTROL REGISTER(ISP_ AFSV)

Auto Focus Accumulation Window Control Register(ISP_ AFEV)

Address : C000 3030h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AFEV**	Vertical ending window point for auto focus accumulation from falling edge of Vertical Sync.	0xFA

TABLE 16-18. AUTO FOCUS ACCUMULATION WINDOW CONTROL REGISTER(ISP_ AFEV)

Auto Focus Accumulation Window Control Register(ISP_ AFSH)

Address : C000 3032h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AFSH**	Horizontal starting window point for auto focus accumulation from falling edge of Horizontal Sync.	0xFA

TABLE 16-19. AUTO FOCUS ACCUMULATION WINDOW CONTROL REGISTER(ISP_ AFSH)

Auto Focus Accumulation Window Control Register(ISP_ AFEH)

Address : C000 3034h

Bit	R/W	Symbol	Description	Reset Value
[12:0]	R/W	**ISP_AFEH**	Horizontal ending window point for auto focus accumulation from falling edge of Horizontal Sync.	0x14A

TABLE 16-20. AUTO FOCUS ACCUMULATION WINDOW CONTROL REGISTER(ISP_ AFEH)

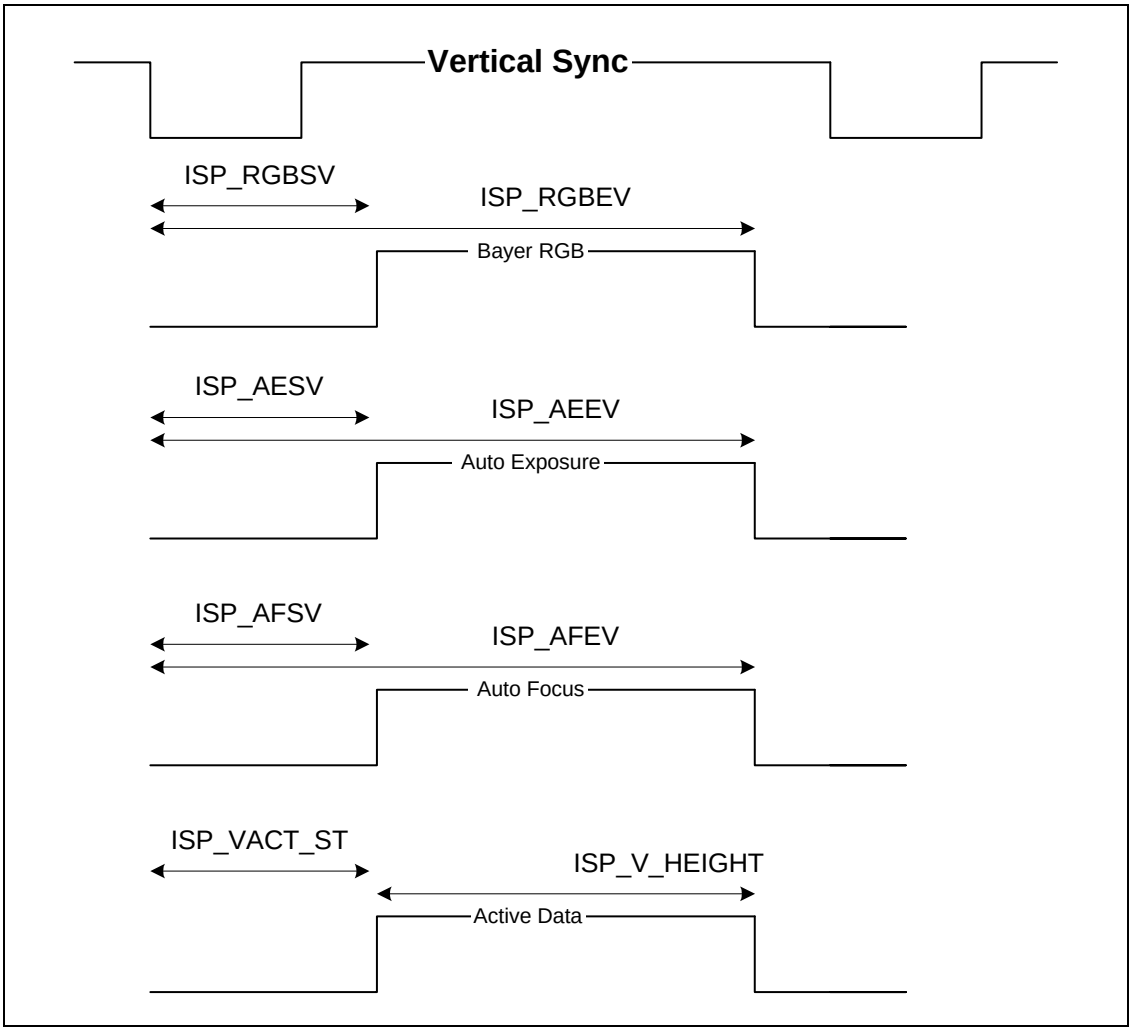


Figure 16-3. Image Signal Vertical Processing Window

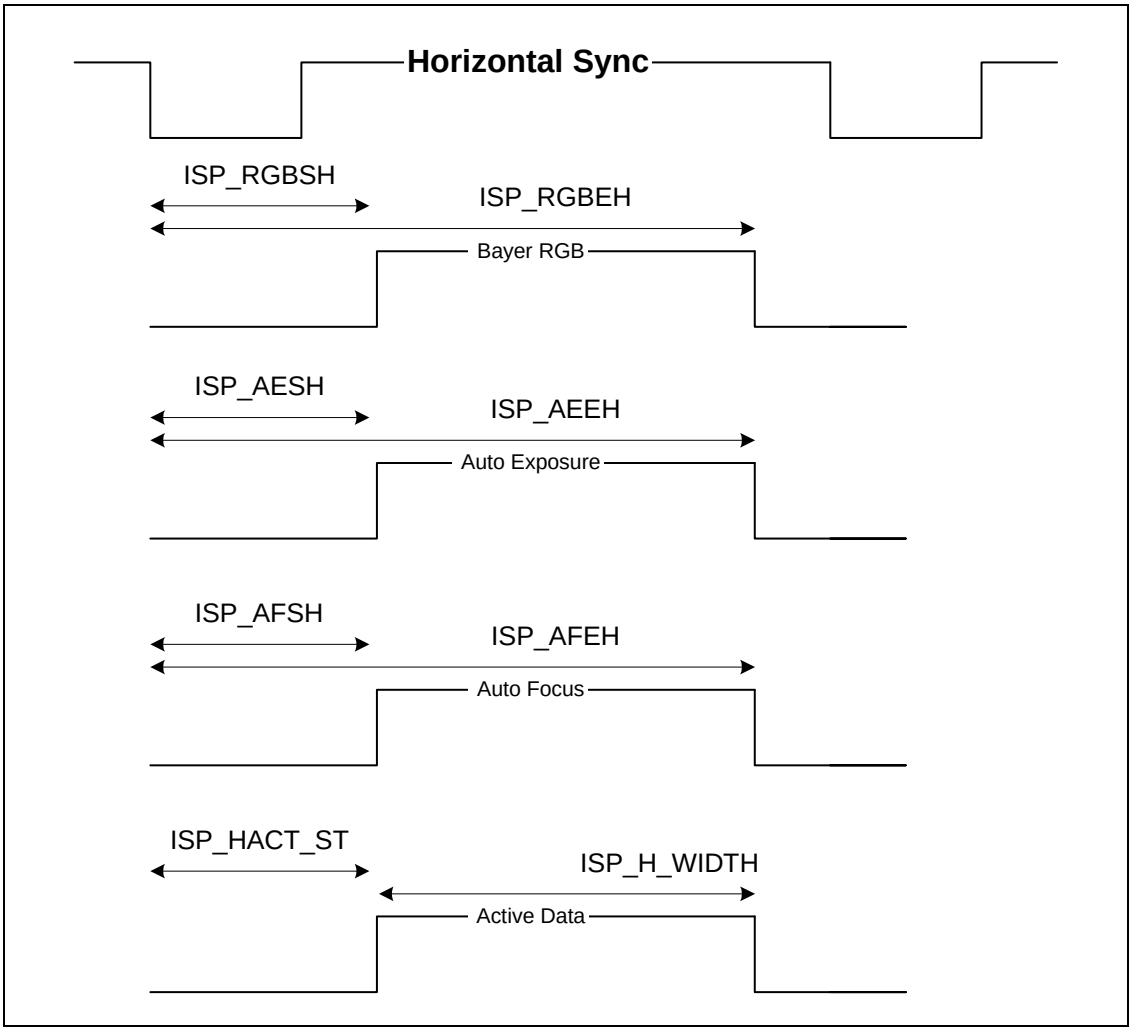


Figure 16-4. Image Signal Horizontal processing window

16.2.3 Gamma Control

The ISP uses a RAM with 1024 x 10 bits for the Gamma Control. This Gamma Ram is applied to only Bayer RGB. The ISP records a Table to Gamma RAM by means of ISP_GAMMA and ISP_GAMMD. ISP_GAMMA is the address of the Gamma RAM, and ISP_GAMMD is Gamma Data. If the Gamma Data are written, the Gamma Address, also, increases. Therefore, the ISP_GAMMA may be set only once.

Gamma Table Control(ISP_GAMMA)

Address : C000 309Ah

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ISP_GAMMA_A**	Address Interface of Gamma Table	0x00

TABLE 16-21. GAMMA TABLE CONTROL(ISP_GAMMA)

Gamma Table Control(ISP_GAMMD)

Address : C000 309Ch

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ISP_GAMMA_D**	Data Interface of Gamma Table The address will increase automatically after write the Data	0x00

TABLE 16-22. GAMMA TABLE CONTROL(ISP_GAMMD)

16.2.4 RGB Recovery

The ISP supports the Bayer RGB arranged as shown in Figure 16-5, and controls it using ISP_BAYER_ODR since the order of the Bayer is not determined. In order to convert the Bayer RGB into RGB, a Filter is used. The ISP creates Red, Green, and Blue using an Average Filter or a Median Filter. It filters using the Line Memory. If a Horizontal line is longer than 1024, Bayer Color is not changed into RGB in real time because the Line Memory capacity is 1024. In such case, the Bayer Color is written at one frame of an external memory. Then the Bayer Color of the External Memory is converted into RGB using Line Memory and written to the External Memory again.The RGB is converted into Y/Cb/Cr and sent to the Scale Processor. When the ISP reads the External Memory or writes the memory in the Bayer Color or the RGB format, Picture sizes and bit numbers by Data must be specified.

Procedure in the Horizontal Line of the Bayer Color with more than 1024	
1 : Bayer Color To External Memory	Determine ISP_MEM_WID (8bits or 16 bits). Determine ISP_DST_HWIDTH. Determine the Destination Address as ISP_MEMADDR1. Set ISP_PATH (=2) into "To Memory". Set ISP_DT_FMT (=6) into "**Bayer RGB Format from External Device (8/10 bits)".**
2:	Check if one Frame is terminated.
3 : Bayer Color To RGB	Determine ISP_SRC_HWIDTH. Determine ISP_DST_HWIDTH. Determine the Source Address as ISP_MEMADDR1. Determine the Destination Address as ISP_MEMADDR2. Set ISP_PATH (=2) into "To Memory". Set ISP_DT_FMT (=9) into "**Bayer RGB Format from External Device (8/10 bits)".**
4:	Check if one Frame is terminated.
5 : RGB to YCbCr	Determine ISP_SRC_HWIDTH. Determine the Source Address as ISP_MEMADDR1. Set ISP_PATH (=2) into "To Memory". Set ISP_DT_FMT (=9) into "**Bayer RGB Format from External Device (8/10 bits)".**

TABLE 16-23. RGB RECOVERY

Image Signal Processor Control Register(ISP_CON_1)

Address : C000 3000h

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**ISP_MEM_DON**	When Memory Write Mode is Setting and One Frame Writing is Completed, This bit is "1".	0
[14:13]	R/W	**ISP_DT_SEL**	ISP Data/Clock Selection 0 : Data = GPIOC[15:0] Clock = GPIOH[4] 1 : a. CCIR656 Format Data[7:0] = { GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], GPIOJ[15], GPIOJ[14], GPIOJ[13] } Clock = GPIOK[2]. b. Parallel RGB Data[23:0] = { GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], GPIOJ[15], GPIOJ[14], GPIOJ[13], GPIOC[15:0] } Clock = GPIOH[4] 2 : Only CCIR656 Format Data[7:0] = GPIOM[8:1] Clock = GPIOM[0] 3 : Reserved	0
[12]	R/W	**ISP_EDT_WID**	ISP Input Data Bit Width 0 : Not 8 bits Data 1: 8 bits Data	0
[11]	R/W	**ISP_ST**	Starting Signal Starting Signal should be pulse(0"→"1" → "0")	0
[10]	R/W	**ISP_ON**	ISP Enable	0
[9]	R/W	**ISP_ACT**	ISP Active Signal	0
[8]	R/W	**ISP_TB_BYPASS**	Gamma Table Bypass Signal 0 : Use Gamma Table 1: bypass Gamma Table	0
[7]	-	**Reserved**	-	-
[6]	R/W	**ISP_MEM_WID**	When reading and writing data(RGB) to External Memory, Bit Per Data 0 : 16 bits 1: 8 bits	0
[5:4]	R/W	**ISP_PATH**	ISP Data Path 0 : To Scale Processor With YC Enhancement 1: To Scale Processor With YC Enhancement Skip 2 : To Memory	0
[3:0]	R/W	**ISP_DT_FMT**	ISP Input Data Format 0 : 4:2:2 Format (16 bits) 1 : Reserved, 2 : Reserved, 3 : CCIR656 Interlaced Format (8 bits) 4 : CCIR656 Progressive Format (8 bits) 5 : CCIR656 Like Format (8 bits) 6 : Bayer RGB Format from External Device (8/10 bits) 7 : parallel RGB(8:8:8) Format(24 bits) 8 : Serial RGB Format(10bits)	0

Bit	R/W	Symbol	Description	Reset Value
			9 : Bayer RGB Format from Memory(8/16 bits) 10 : RGB Format from Memory (8/16 bits per Color)	

TABLE 16-24. IMAGE SIGNAL PROCESSOR CONTROL REGISTER(ISP_CON_1)

External Memory Address(ISP_MEMADDRL1, ISP_MEMADDRH1)

Address : C000 3096h
Address : C000 3098h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**ISP_MEMADDR1**	When External Device to Memory Mode, Destination Address. When Memory to Memory Mode, Source Address.	0x00

TABLE 16-25. EXTERNAL MEMORY ADDRESS(ISP_MEMADDRL1, ISP_MEMADDRH1)

External Memory Address(ISP_MEMADDRL2, ISP_MEMADDRH2)

Address : C000 30EEh
Address : C000 30F0h

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**ISP_MEMADDR2**	When Memory to Memory Mode, Destination Address.	0x00

TABLE 16-26. EXTERNAL MEMORY ADDRESS(ISP_MEMADDRL2, ISP_MEMADDRH2)

Image Signal Processor Source Pixel Width register(ISP_SRC_HWIDTH)

Address : C000 3016h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_ SRC_HWIDTH**	ISP Horizontal Memory Width of Source Pixel. The unit is Byte (pixel width) x 1, when 8bits BAYERRGB (pixel width) x 2, when 16bits BAYERRGB (pixel width) x 3, when 8bits RGB (pixel width) x 6, when 16bits RGB	0x00

TABLE 16-27. IMAGE SIGNAL PROCESSOR SOURCE PIXEL WIDTH REGISTER(ISP_SRC_HWIDTH)

Image Signal Processor Destination Pixel Width Register(ISP_DST_HWIDTH)

Address : C000 30F2h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_ DST_HWIDTH**	ISP Horizontal Memory Width of Destination Pixel. The unit is Byte (pixel width) x 1, when 8bits BAYERRGB (pixel width) x 2, when 16bits BAYERRGB (pixel width) x 3, when 8bits RGB (pixel width) x 6, when 16bits RGB	0x00

TABLE 16-28. IMAGE SIGNAL PROCESSOR SOURCE PIXEL WIDTH REGISTER(ISP_DST_HWIDTH)

Bayer RGB Recovery Method(ISP_RGBREC)

Address : C000 303Ah

Bit	R/W	Symbol	Description	Reset Value
[15:9]	-	**Reserved**	-	-
[8]	R/W	**ISP_R_REC_ TYPE**	R Pixel Recovery Type 0 : median filter 1 : Average	0
[7:5]	R/W	**ISP_G_REC_ TYPE**	G Pixel Recovery Type 000 : Average Left and Right 001 : Average UP and DOWN 010 : Median Filter 011 : Average Left , Right, Up and Down,	010
[4]	R/W	**ISP_B_REC_ TYPE**	B Pixel Recovery Type 0 : median filter 1 : Average	0
[3:2]	R/W	**ISP_BAYER_ ODR**	Bayer RGB Array Type 00 : FIRST_GB 01 : FIRST_BG 10 : FIRST_RG 11 : FIRST_GR	00
[1]	R/W	**ISP_CBRSWAP**	Cb/Cr Swap 0 : normal 1 : swap	0
[0]	R/W	**ISP_VID_RANGE**	Video Range 0 : Y = 219 / 256 x Y + 16 = (16 ~ 235) Cb = 224 / 256 x Cb + 16 = (16 ~ 240) Cr = 244 / 256 x Cr + 16 (16 ~ 240) 1 : Y = Y(0 ~ 255) Cb = Cb(0 ~ 255) Cr = Cr(0 ~ 255)	0

TABLE 16-29. BAYER RGB RECOVERY METHOD(ISP_RGBREC)

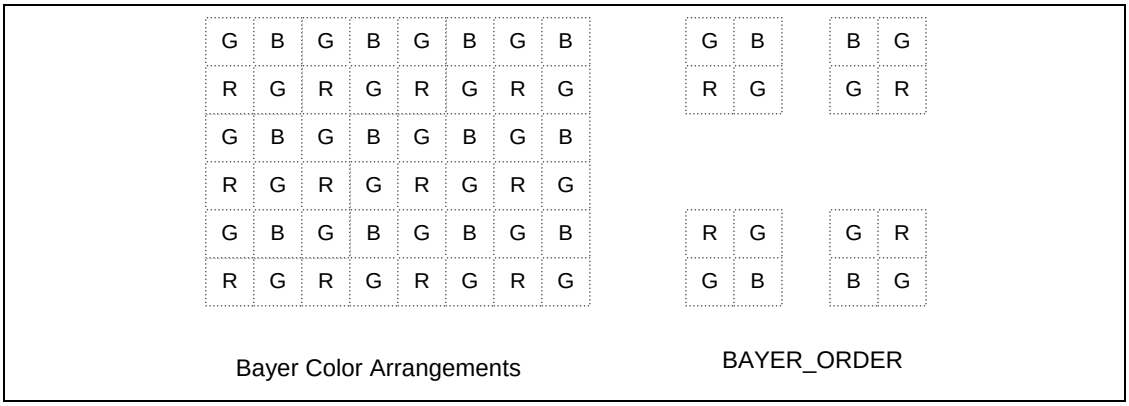


Figure 16-5. Bayer Color Arrangements

16.2.5 Color Space Converter (RGB to YcbCr)

The result of the ISP is Y/Cb/Cr Format. Therefore, RGB Data is converted into Y/Cb/Cr using the following formula.

Y = 0.299R + 0.587G + 0.114B

(B-Y) = -0.299R - 0.587G + 0.886B = 1.772 x Cb

(R-Y) = 0.701R - 0.587G - 0.114B = 1.402 x Cr

16.2.6 Luminance Enhancements

16.2.6.1 Edge Enhancement

The ISP enhances image quality by adding the Edge extracted. The Edge extracted by a High Pass Filter is added to Main Data to have the Edge section show up and makes clearer image quality.

Horizontal Edge Enhancement Gain(ISP_YGAIN)

Address : C000 3054

Bit	R/W	Symbol	Description	Reset Value
[6:4]	R/W	**ISP_YEDGEGAIN**	Horizontal Edge Gain 0 = 0.0, 1 = 1.0, 2 = 1.5, 3 = 2.0, 4 = 2.5, 5 = 3.0, 6 = 3.5, 7 = 4.0,	0x01
[3]		**Reserved**	-	-
[2:0]	R/W	**ISP_YMAINGAIN**	Horizontal Main path 0 = 0.0, 1 = 0.5, 2 = 0.75 3 = 1.0, 4 = 1.25, 5 = 1.5, 6 = 1.75 7 = 2.0,	0x03

TABLE 16-30. HORIZONTAL LUMINANCE ENHANCEMENT GAIN(ISP_YGAIN)

Horizontal Edge Enhancement Slice Limit (ISP_SLICELMT)

Address : C000 3060

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**ISP_SLICELMT**	The signal in the area Slice Limit will be zero This is used for reducing noise Range = 0 ~ 255	0x08

TABLE 16-31. HORIZONTAL LUMINANCE ENHANCEMENT GAIN(ISP_YGAIN)

16.2.6.2 Contrast

The contrast of Luminance is controlled by Image Data Information or a fixed value. The Contrast control using Image Data determines the region to get image information using ISP_RGBSV, ISP_RGBEV, ISP_RGBSH and ISP_ RGBEH. In addition, the desired level information is extracted by setting the Low/High Level value in ISP_CNTRSTLIM. The information extracted is a Count value and an Accumulated value. Using these values, the proper Contrast value is determined and set in ISP_CNTRSTGAIN.

Contrast Control Register(ISP_CNTRSTAIN)

Address : C000 3036h

Bit	R/W	Symbol	Description	Reset Value
[3]	R/W	**ISP_ CNTRSTACCEN**	Accumulation Enable Signal for auto Contrast Control.	0x0
[2:0]	R/W	**ISP_ CNTRSTGAIN**	Contrast Gain Control 0 : 0.25, 1 : 0.5, 2 : 0.75, 3 : 1.0, 4 : 1.25, 5 : 1.5, 6 : 1.75, 7 : 2.0	0x3

TABLE 16-32. CONTRAST CONTROL REGISTER(ISP_CNTRSTAIN)

Contrast Control Register(ISP_CNTRSTLIM)

Address : C000 3038h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_CNTRUL**	Upper limit for auto contrast accumulation.	0xFF
[7:0]	R/W	**ISP_CNTRLL**	Lower limit for auto contrast accumulation.	0x00

TABLE 16-33. CONTRAST CONTROL REGISTER(ISP_CNTRSTLIM)

16.2.6.3 Brightness

The Brightness is determined by adding the value between -128 and 127 to the Data of Luminance. A Negative Number means the degree of darkness, and a positive Number means the degree of brightness.

Brightness Control Register(ISP_BRIGHT)

Address : C000 3058h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**ISP_BRIGHT**	Range = -128 ~ 127	0x00

TABLE 16-34. BRIGHTNESS REGISTER(ISP_BRIGHT)

16.2.7 Chrominance Enhancement

16.2.7.1 Decimation

The result of the ISP is 4:2:2 Format. The data converted into Y/Cb/Cr from RGB has 4:4:4 Format. The ISP converts 4:4:4 Data Format into 4:2:2 Format using a decimation filter. Without the decimation filter, the ISP can, also, convert a Format.

Clip Point & Color suppress Register(ISP_CSUPSLANT)

Address : C000 305Eh

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**ISP_CSLANT_EN**	Color Suppress enable bit. 0 : Disable 1 : Enable	0
[14]	R/W	**ISP_DECI_OFF**	Chrominance Decimation Filter Off 0 : Filter On 1 : Filter Off	0
[13:3]		**Reserved**	-	-
[2:0]	R/W	**ISP_ CSLANT_PNT**	Suppress Gain Control	0x4

TABLE 16-35. CLIP POINT& COLOR SUPPRESS REGISTER(ISP_CSUPSLANT)

The property of the High pass Filter is as follows:

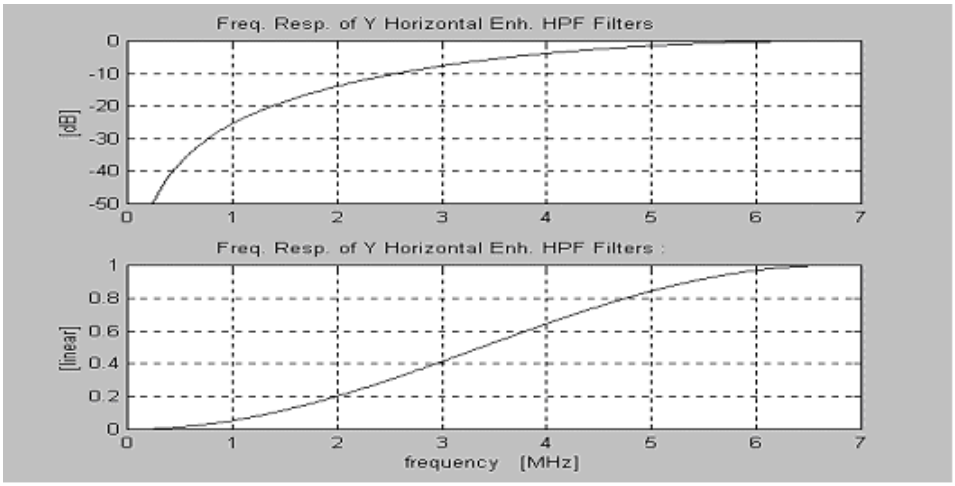


Figure 16-6. Frequency Response of Luminance Enhancement

The property of the Decimation Filter is as follows:

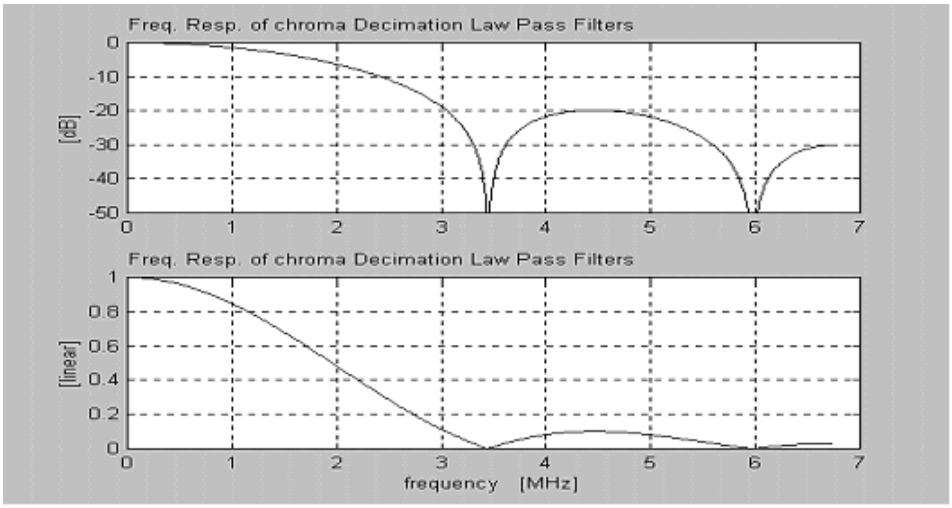


Figure 16-7. Frequency Response of Chrominance Decimation Filter

16.2.7.2 Hue Control & Gain Control

The Hue controls a Phase on the Cb/Cr Coordinate system. The Phase controls whole quadrants (First Quadrant to Fourth Quadrant) using the same value or each quadrant respectively. For the Phase control, the following formulas are used.

(B-Y)' = (B-Y) * Cos(θ) - (R-Y) * Sin(θ)
(R-Y)' = (B-Y) * Sin(θ) + (R-Y) * Cos(θ)

These formulas are applied to each quadrant as follows:

1) 1st quadrant ((B-Y) = 0 & (R-Y) = 0)
   (B-Y)' = (B-Y) x HUECB1_A + (R-Y) x HUECB1_B
   (R-Y)' = (B-Y) x HUECR1_A + (R-Y) x HUECR1_B
2) 2nd quadrant ((B-Y) < 0 & (R-Y) = 0)
   (B-Y)' = (B-Y) x HUECB2_A + (R-Y) x HUECB2_B
   (R-Y)' = (B-Y) x HUECR2_A + (R-Y) x HUECR2 _B
3) 3rd quadrant ((B-Y) < 0 & (R-Y) < 0)
   (B-Y)' = (B-Y) x HUECB3_A + (R-Y) x HUECB3_B
   (R-Y)' = (B-Y) x HUECR3_A + (R-Y) x HUECR3_B
4) 4th quadrant ((B-Y) = 0 & (R-Y) < 0)
   (B-Y)' = (B-Y) x HUECB4_A + (R-Y) x HUECB4_B
   (R-Y)' = (B-Y) x HUECR4_A + (R-Y) x HUECR4_B

HUECBn and HUECRn are the Gain of Cb/Cr. The gain is placed in between -2 and 2 and multiplied by 64.

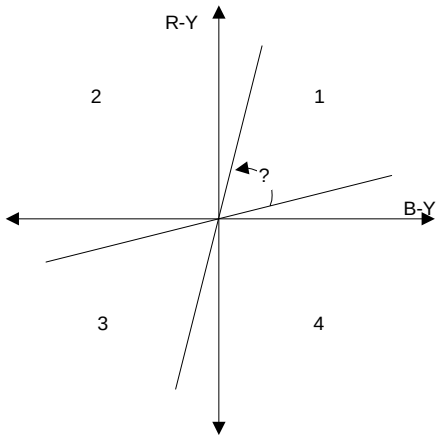


Figure 16-8. The Basic Concept of Hue Control

Hue Control for Each of 4 Coordinates Register

Register	Address	Width	Description	Reset Value
ISP_HUECB1AB	0xc0003040	HW	Hue Control of First Coordinate	0x4000
ISP_HUECR1AB	0xc0003042	HW	Hue Control of First Coordinate	0x0040
ISP_HUECB2AB	0xc0003044	HW	Hue Control of Second Coordinate	0x4000
ISP_HUECR2AB	0xc0003046	HW	Hue Control of Second Coordinate	0x0040
ISP_HUECB3AB	0xc0003048	HW	Hue Control of Third Coordinate	0x4000
ISP_HUECR3AB	0xc000304a	HW	Hue Control of Third Coordinate	0x0040
ISP_HUECB4AB	0xc000304c	HW	Hue Control of Fourth Coordinate	0x4000
ISP_HUECR4AB	0xc000304e	HW	Hue Control of Fourth Coordinate	0x0040

TABLE 16-36. HUE CONTROL FOR EACH OF 4 COORDINATER REGISTER

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_HUECBnA**	Gain is -2 to +2 Decimal Point = [6.5] 2's complement	0x40
[7:0]	R/W	**ISP_HUECBnB**	Gain is –2 to +2 Decimal Point = [6.5](1) 2's complement	0x00
			At each Coordinate, input the result of following equations. (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B	

TABLE 16-37. HUE CONTROL FOR EACH OF 4 COORDINATES REGISTER

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_HUECRnA**	Gain is -2 to +2 Decimal Point = [6.5] 2's complement	0x40
[7:0]	R/W	**ISP_HUECRnB**	Gain is –2 to +2 Decimal Point = [6.5](1) 2's complement	0x00
			At each Coordinate, input the result of following equations. (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B	

TABLE 16-38. HUE CONTROL FOR EACH OF 4 COORDINATES REGISTER

16.2.8 Clip & Color Suppress

Clip is applied to Luminance, and Color Suppress is applied to Chrominance. In Clip, the Luminance input below ISP_CLIP1 comes out unchanged. The slant of ISP_CLIPSLANT is applied to the Luminance input (Yin) between ISP_CLIP1 and ISP_CLIP2. In addition, Yin above ISP_CLIP2 is formed with the ISP_CLIP2 level.

In Color Suppress, the Clip information of the Luminance is used. In case of not exceeding ISP_CLIP1, the Chrominance input comes out unchanged. In a case of exceeding ISP_Clip2, the Zero value is applied. The slant of the Chrominance is applied between ISP_CLIP1 and ISP_CLIP2 using ISP_CSLANT_PNT. For the ISP_CSLANT_PNT and the slant of the Chrominance, refer to Table 16-35.

ISP_CSLANT_PNT	Slant of Starting point	Slant of Ending point
0	ISP_CLIP1	(Yin – ISP_CLIP1) = 1
1	ISP_CLIP1	(Yin – ISP_CLIP1) = 3
2	ISP_CLIP1	(Yin – ISP`_CLIP1) = 7
3	ISP_CLIP1	(Yin – ISP_CLIP1) = 15

4	ISP_CLIP1	(Yin – ISP_CLIP1) = 31
5	ISP_CLIP1	(Yin – ISP_CLIP1) = 63
6	ISP_CLIP1	(Yin – ISP_CLIP1) = 127
7	ISP_CLIP1	(Yin – ISP_CLIP1) = 255

TABLE 16-39. CLIP & COLOR SUPPRESS

Clip Point & Color Suppress Register(ISP_YCLIP)

Address : C000 305Ah

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_CLIP2**	ISP_Clip2 = High Clip, Range = 0 ~ 255	0xFF
[7:0]	R/W	**ISP_CLIP1**	ISP_Clip1 = Clip knee, Range = 0 ~ 255 If ISP_Clip1 = ISP_Clip2 = 255, then CLIP OFF.	0xFF

TABLE 16-40. CLIP POINT & COLOR SUPPRESS REGISTER(ISP_YCLIP)

Clip Point & Color Suppress Register(ISP_YCLIPSLANT)

Address : C000 305Ch

Bit	R/W	Symbol	Description	Reset Value
[2:0]	R/W	**ISP_CLIPSLANT**	Slant between ISP_CLIP1 and ISP_CLIP2 0 = 0.0 1 = 0.125, 2 = 0.250 3 = 0.375 4 = 0.5 5 = 0.625, 6 = 0.75 7 = 0.875	0x4

TABLE 16-41. CLIP PONT & COLOR SUPPRESS REGISTER(ISP_YCLIPSLANT)

Clip Point & Color Suppress Register(ISP_CSUPSLANT)

Address : C000 305Eh

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**ISP_CSLANT_EN**	Color Suppress enable bit 0 : Disable 1 : Enable	0
[14]	R/W	**ISP_DECI_OFF**	Chrominance Decimation Filter Off 0 : Filter On 1 : Filter Off	0
[13:3]		**Reserved**	-	-
[2:0]	R/W	**ISP_CSLANT_PNT**	Suppress Gain Control	0x4

TABLE 16-42. CLIP POINT & COLOR SUPPRESS REGISTER(ISP_CSUPSLANT)

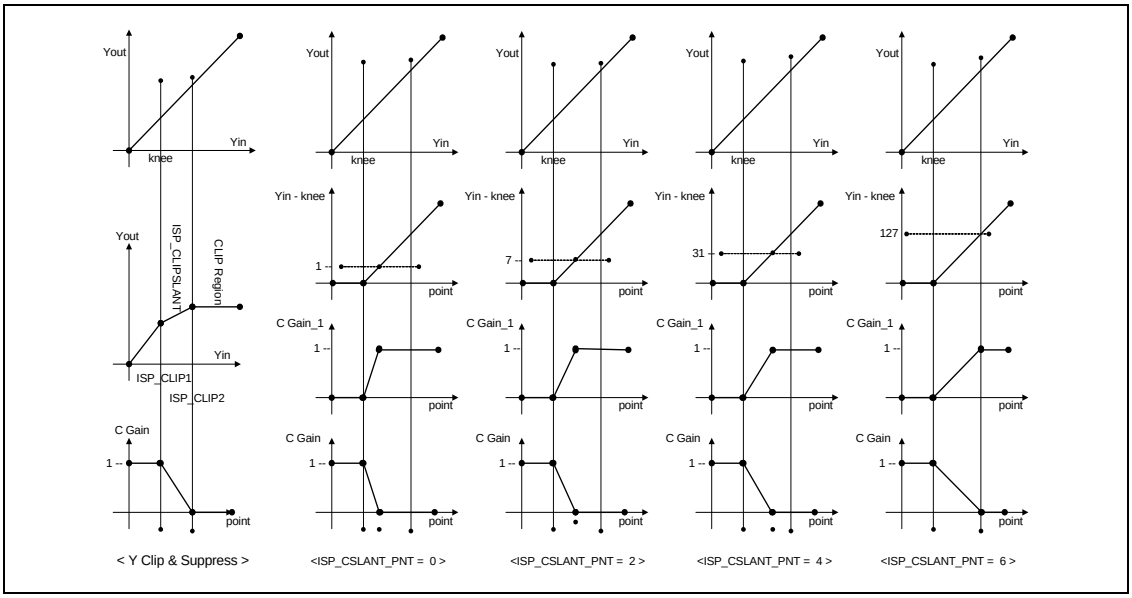


Figure 16-9. Luminance Clip & Color Suppress by Level

16.2.9 Auto Exposure

The ISP provides ARM9 with the accumulated value of Luminance to be used for Auto Exposure. The ISP makes 16 regions and the accumulated value of each area. The ISP determines the Limit of Luminance by means of ISP_AELIM and accumulates only the values within the Limit. Each area use ISP_AESV, ISP_AEEV, ISP_AESH, ISP_AEEH, ISP_AEVSTEP and ISP_AEHSTEP. The accumulated values are updated when Vertical Sync. The ARM gets the accumulated values through the ISP_AEACC Register.

Auto Exposure Accumulation Control Register(ISP_AELIM)

Address : C000 3028h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_AEULIM**	Upper limit for auto exposure accumulation.	0xFF
[7:0]	R/W	**ISP_AELLIM**	Lower limit for auto exposure accumulation.	0x00

TABLE 16-43. AUTO EXPOSURE ACCUMULATION CONTROL REGISTER(ISP_AELIM)

Auto Exposure Accumulation Control Register(ISP_ AEVSTEP)

Address : C000 302Ah

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ISP_AEVSTEP**	Vertical step for exposure accumulation is fixed with 4. ISP_AEVSTEP = (ISP_AEEV - ISP_AESV) / 4	0x3C

TABLE 16-44. AUTO EXPOSURE ACCUMULATION CONTROL REGISTER(ISP_ AEVSTEP)

Auto Exposure Accumulation Control Register(ISP_ AEHSTEP)

Address : C000 302Ch

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ISP_AEHSTEP**	Horizontal step for exposure accumulation is fixed with 4. ISP_AEHSTEP = (ISP_AEEH - ISP_AESH) / 4	0x50

TABLE 16-45. AUTO EXPOSURE ACCUMULATION CONTROL REGISTER(ISP_ AEHSTEP)

Auto Exposure Result Register(ISP_AEACCH)

Address : C000 309Eh

Bit	R/W	Symbol	Description	Reset Value
[15:13]	-	**Reserved**	-	-
[12:0]	R	**ISP_AEACCH**	High 13 bits (Map Address[1:0] = 10)	0x00

TABLE 16-46. AUTO EXPOSURE RESULT REGISTER(ISP_AEACCH)

Auto Exposure Result Register(ISP_AEACCL)

Address : C000 30DCh

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_AEACCL**	Low 16 bits (Map Address[1:0] = 00)	0x00
			Total Block Number is 16 words. Bits per block are total 29 bits.	

TABLE 16-47. AUTO EXPOSURE RESULT REGISTER(ISP_AEACCL)

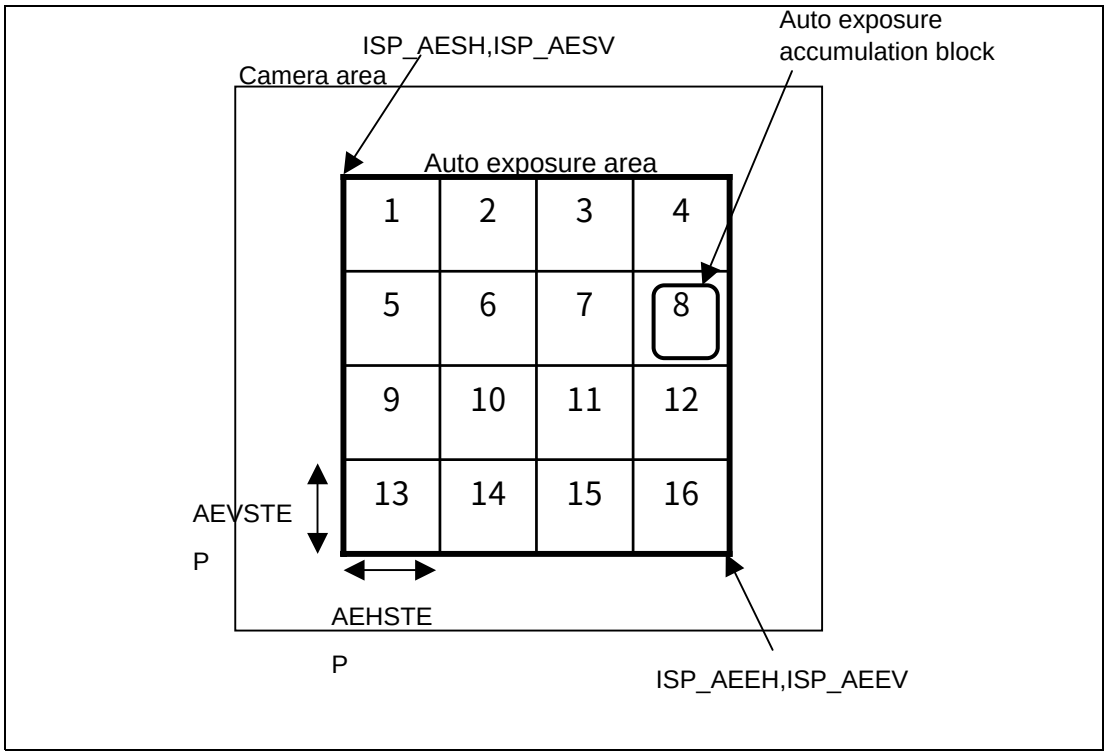


Figure 16-10. Auto Exposure Coordinates

16.2.10 Auto Focus

The ISP provides ARM9 with the accumulated value of Luminance passed through the Band Pass Filter. The ISP makes one region. The ISP accumulates the values by Band Pass Filtering the Luminance within the region. The region uses ISP_AFSV, ISP_AFEV, ISP_AFSH and ISP_AFEH. The accumulated values are updated when Vertical Sync. The ARM gets the accumulated values through the ISP_AFACC Register

Auto Focus Accumulation Register(ISP_AFACCH, ISP_AFACCL)

Address : C000 3070h / C000 3072h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_AFACCH**	Auto Focus Accumulation	0x00
[15:0]	R	**ISP_AFACCL**	Auto Focus Accumulation	0x00
			The number of Edge(Output of band pass filter) in auto focus area	

TABLE 16-48. AUTO FOCUS ACCUMULATION REGISTER(ISP_AFACCL, ISP_AFACCH)

16.2.11 Auto White Balance

The ISP provides the ARM9 with the accumulated frequency and the accumulated value of the Cb/Cr to be used for Auto White Balance. It determines a region in time domain. This region uses ISP_AESV, ISP_AEEV, ISP_AESH and ISP_AEEH. It determines the accumulation of the Auto White Balance Data by comparing Luminance Data in this region to ISP_WB_ULMT and ISP_WB_LLMT, and makes 256 regions on the (B-Y)/(R-Y) coordinate system.

These regions are made using ISP_WBCOORD0 to ISP_WBCOORD15 and indicate the position of the region that the Cb/Cr Data exist. If Luminance condition is satisfied, the accumulated frequency and the Data of the Cb/Cr are accumulated only when the Cb/Cr Data are present in the domain to be accumulated on the (B-Y)/(R-Y) coordinate system. The Accumulated value is updated whenever Vertical Sync. The ARM gets the accumulated value through the WBACCCNT, ISP_WBCBACC and ISP_WBCRACC Registers.

Upper/ Lower Limit for White Balance Accumulation Register(ISP_WBLMT)

Address : C000 3062h

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_WB_ULMT**	Upper Limit value of Luminance Level for White Balance Accumulation	0xFF
[7:0]	R/W	**ISP_WB_LLMT**	Lower Limit value of Luminance Level for White Balance Accumulation	0x00

TABLE 16-49. UPPER/ LOWER LIMIT FOR WHITE BALANCE ACCUMULATION REGISTER(ISP_WBLMT)

Upper/ Lower Limit for White Balance Accumulation Register(ISP_WBACCCNTH, ISP_WBACCCNTL)

Address : C000 3064h / C000 3066h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	**ISP_WBACCCNTH**	Upper 8 bits	0x00
[15:0]	R	**ISP_WBACCCNTL**	Lower 16 bits	0x00
			The total number of pixels which are in the white balance area.	

TABLE 16-50. UPPER/ LOWER LIMIT FOR WHITE BALANCE ACCUMULATION REGISTER(ISP_WBACCCNTH, ISP_WBACCCNTL)

Upper/ Lower Limit for White Balance Accumulation Register(ISP_WBCBACCH, ISP_WBCBACCL)

Address : C000 3068h
Address : C000 306Ah

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_WBCBACCH**	Upper 16 bits	0x00
[15:0]	R	**ISP_WBCBACCL**	Lower 16 bits	0x00
			The number of Cb pixels which are in the white balance area	

TABLE 16-51. UPPER/ LOWER LIMIT FOR WHITE BALANCE ACCUMULATION REGISTER(ISP_WBCBACCH, ISP_WBCBACCL)

Upper/ Lower Limit for White Balance Accumulation Register(ISP_WBCRACCH, ISP_WBCRACCL)

Address : C000 306Ch
Address : C000 306Eh

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_WBCRACCH**	Upper 16 bits	0x00
[15:0]	R	**ISP_WBCRACCL**	Lower 16 bits	0x00
			The number of Cr pixel which is in the white balance area	

TABLE 16-52. UPPER/ LOWER LIMIT FOR WHITE BALANCE ACCUMULATION REGISTER(ISP_WBCRACCH, ISP_WBCRACCL)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD0)

Address : C000 3076h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD0**	Set white balance pattern (1), 0 block setting ,	0x00

TABLE 16-53. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD0)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD1)

Address : C000 3078h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD1**	Set white balance pattern (1), 16~31 block setting	0x00

TABLE 16-54. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD1)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD2)

Address : C000 307Ah

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD2**	Set white balance pattern (1), 32~47 block setting	0x00

TABLE 16-55. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD2)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD3)

Address : C000 307Ch

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD3**	Set white balance pattern (1), 48~63 block setting	0x00

TABLE 16-56. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD3)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD4)

Address : C000 307Eh

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD4**	Set white balance pattern (1), 64~79 block setting	0x00

TABLE 16-57. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD4)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD5)

Address : C000 3080h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD5**	Set white balance pattern (1), 80~95 block setting	0x00

TABLE 16-58. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD5)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD6)

Address : C000 3082h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD6**	Set white balance pattern (1), 96~111 block setting	0x00

TABLE 16-59. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD6)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD7)

Address : C000 3084h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD7**	Set white balance pattern (1), 112~127 block setting	0x00

TABLE 16-60. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD7)

Color Coordinate Selection for White Balance Register (ISP_WBCOORD8)

Address : C000 3086h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD8**	Set white balance pattern (1), 128~143 block setting	0x00

TABLE 16-61. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER (ISP_WBCOORD8)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD9)

Address : C000 3088h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD9**	Set white balance pattern (1), 144~159 block setting	0x00

TABLE 16-62. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD9)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD10)

Address : C000 308Ah

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD10**	Set white balance pattern (1), 160~175 block setting	0x00

TABLE 16-63. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD10)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD11)

Address : C000 308Ch

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD11**	Set white balance pattern (1) 176~191 block setting	0x00

TABLE 16-64. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD11)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD12)

Address : C000 308Eh

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD12**	Set white balance pattern (1), 192~207 block setting	0x00

TABLE 16-65. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD12)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD13)

Address : C000 3090h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD13**	Set white balance pattern (1), 208~223 block setting	0x00

TABLE 16-66. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD13)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD14)

Address : C000 3092h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD14**	Set white balance pattern (1), 224~239 block setting	0x00

TABLE 16-67. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD14)

Color Coordinate Selection for White Balance Register(ISP_WBCOORD15)

Address : C000 3094h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**ISP_WBCOORD15**	Set white balance pattern (1), 240~255 block setting	0x00

TABLE 16-68. COLOR COORDINATE SELECTION FOR WHITE BALANCE REGISTER(ISP_WBCOORD15)

R-Y

+127

LSB MSB

WBCOORD0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WBCOORD1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WBCOORD2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
WBCOORD3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
WBCOORD4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
WBCOORD5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
WBCOORD6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
WBCOORD7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
WBCOORD8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
WBCOORD9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
WBCOORD10	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
WBCOORD11	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
WBCOORD12	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
WBCOORD13	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
WBCOORD14	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
WBCOORD15	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

-127 +127 B-Y

-127

Figure 16-11. Auto White Balance Coordinates

16.2.12 Possible Image Input Data Format and Related Port

Format	Condition	Data	Clock
YCbCr(4:2:2)	ISP_DT_SEL = 0	Y[7:0] = GPIOC[7:0] C[7:0] = GPIOC[15:8]	Clock = GPIOH[4]
CCIR656	ISP_DT_SEL = 1	YcbCr[7:0]={GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], PIOJ[15], GPIOJ[14], PIOJ[13] }	Clock = GPIOK[2].
	ISP_DT_SEL = 2	YcbCr[7:0] = GPIOM[8:1]	Clock = GPIOM[0]
Bayer RGB	ISP_DT_SEL = 0	Data[9:0] = GPIOC[9:0]	Clock = GPIOH[4]
Serial RGB	ISP_DT_SEL = 0	Data[9:0] = GPIOC[9:0]	Clock = GPIOH[4]
Parallel RGB	ISP_DT_SEL = 0	R[7:0]={GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], GPIOJ[15], GPIOJ[14], GPIOJ[13]} G[7:0] = GPIOC[15:8] B[7:0] = GPIOC[7:0]	Clock = GPIOH[4]

TABLE 16-69. POSSIBLE IMAGE INPUT DATA FORMAT AND RELATED PORT

16.3 IMAGE SIGNAL PROCESS REGISTER

Bit	R/W	Symbol	Description	Reset Value
Image Signal Processor Control Register(ISP_CON_1) ***Address : C000 3000h***				
[15]	R/W	**ISP_MEM_DON**	When Memory Write Mode is Setting and One Frame Writing is Completed, This bit is "1".	0
[14:13]	R/W	**ISP_DT_SEL**	ISP Data/Clock Selection 0 : Data = GPIOC[15:0] Clock = GPIOH[4] 1 : a. CCIR656 Format Data[7:0] = { GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], GPIOJ[15], GPIOJ[14], GPIOJ[13] } Clock = GPIOK[2]. b. Parallel RGB Data[23:0] = { GPIOI[15], GPIOI[14], GPIOI[3], GPIOI[2], GPIOI[1], GPIOJ[15], GPIOJ[14], GPIOJ[13], GPIOC[15:0] } Clock = GPIOH[4] 2 : Only CCIR656 Format Data[7:0] = GPIOM[8:1] Clock = GPIOM[0] 3 : Reserved	0
[12]	R/W	**ISP_EDT_WID**	ISP Input Data Bit Width 0 : Not 8 bits Data 1: 8 bits Data	0
[11]	R/W	**ISP_ST**	Starting Signal Starting Signal should be pulse(0"→"1" → "0")	0
[10]	R/W	**ISP_ON**	ISP Enable	0
[9]	R/W	**ISP_ACT**	ISP Active Signal	0
[8]	R/W	**ISP_TB_BYPASS**	Gamma Table Bypass Signal 0 : Use Gamma Table 1: Bypass Gamma Table	0
[7]		**Reserved**	-	-
[6]	R/W	**ISP_MEM_WID**	When reading and writing data(RGB) to External Memory, Bit Per Data 0 : 16 bits 1: 8 bits	0
[5:4]	R/W	**ISP_PATH**	ISP Data Path 0 : To Scale Processor With YC Enhancement 1: To Scale Processor With YC Enhancement Skip 2 : To Memory	0
[3:0]	R/W	**ISP_DT_FMT**	ISP Input Data Format 0 : 4:2:2 Format (16 bits) 1 : Reserved, 2 : Reserved,	0

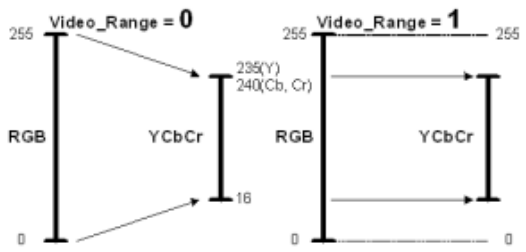
Bit	R/W	Symbol	Description	Reset Value
			3 : CCIR656 Interlaced Format (8 bits) 4 : CCIR656 Progressive Format (8 bits) 5 : CCIR656 Like Format (8 bits) 6 : Bayer RGB Format from External Device (8/10 bits) 7 : parallel RGB(8:8:8) Format(24 bits) 8 : Serial RGB Format(10bits) 9 : Bayer RGB Format from Memory(8/16 bits) 10 : RGB Format from Memory (8/16 bits per Color)	
Image Signal Processor Control Register(ISP_CON_2) ***Address : C000 3002h***				
[13]	R/W	**ISP_LOCK_OFF**	Lock Disable Signal when Memory Interface 0 : Lock On 1: Lock Disable	0
[12]	R/W	**ISP_BST_OFF**	Burst Disable Signal when Memory Interface 0 : Burst On 1: Burst Disable	0
[11]	R/W	**ISP_VSYNC_ST_POL**	Select Vertical Starting Point 0 : Rising Edge of Vertical Sync. 1: Falling Edge of Vertical Sync	0
[10:9]	R/W	**ISP_RGB_ORD**	Select RGB Order 0 : R,G,B 1 : : B,R,G 2 : G,B,R 3 : B,G,R	0
[8]	R/W	**ISP_FLD_GEN**	Generate Field Signal 0 : From Field Information(CCIR656) 1 : Generate Field Signal from External H/V Sync	0
[7:6]	R/W	**ISP_CLK_SRC**	Select Clock Source 0 : GPIOH[4] 1 : Clock = GPIOK[2]./ GPIOM[0] 2 : Divided Clock from Internal PLL Clock	0
[5]	R/W	**ISP_SYNC_DIR**	Select Sync(H/V) Direction 0 : Input from external Sync 1 : Output Internal Sync HSYNC = GPIOH[3], VSYNC = GPIOH[2]	0
[4]	R/W	**ISP_CLK2_SYS**	Select ISP OUT Clock Source 0 : ISP Divider Clock 1 : System Clock (Memory Clock)	0
[3]	R/W	**ISP_CLK1_SYS**	Select ISP IN Clock Source 0 : ISP Divider Clock 1 : System Clock (Memory Clock)	0
[2]	R/W	**ISP_CLK_POL**	Select Input Clock Polarity 0 : Normal	0

Bit	R/W	Symbol	Description	Reset Value
			1 : Inversion	
[1]	R/W	**ISP_VSYNC_POL**	VSYNC Signal Polarity, 0 : Normal 1 : Inversion	0
[0]	R/W	**ISP_HSYNC_POL**	HSYNC Signal Polarity, 0 : Normal 1 : Inversion	0
Image Signal Processor Interrupt Control Register(ISP_INT_CON) ***Address : C000 3004h***				
[14]	R	**ISP_VSYNC**	Status of Vertical Sync Signal Shows the IVSYNC pin status.	0
[13]	R	**ISP_HSYNC**	Status of Horizontal Sync Signal Shows the IHSYNC pin status.	0
[12:9]	R	**Reserved**	Reserved	0
[5]	R/W	**ISP_VINT_EN**	Vertical Sync Interrupt Enable 1 : Enable 0 : Disable	0
[4]	R/W	**ISP_VINT _TYPE**	Vertical Sync Interrupt Type 0 : Falling edge1 : Rising edge	0
[3]	R/W	**ISP_VINT _SC**	Vertical Sync Interrupt Status and Clear write “1” to Clear Interrupt Status	0
[2]	R/W	**ISP_HINT_EN**	Horizontal Sync Interrupt Enable 1 : Enable 0 : Disable	0
[1]	R/W	**ISP_HINT _TYPE**	Horizontal Sync Interrupt Type 0 : Falling edge1 : Rising edge	0
[0]	R/W	**ISP_HINT _SC**	Horizontal Sync Interrupt Status and Clear write “1” to Clear Interrupt Status	0
ISP Sync Control Register(ISP_VPERIOD) ***Address : C000 3006h***				
[12:0]	R/W	**ISP_VPERIOD**	Vertical Sync Period. The unit is Horizontal Sync. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x106
ISP Sync Control Register(ISP_VPW) ***Address : C000 3008h***				
[15:11]	R/W	**ISP_EAV2VSYNC**	Vertical EAV to Vertical Sync Starting point. The unit is Horizontal Sync. Effective when in CCIR655 mode.	0x00
[9:0]	R/W	**ISP_VPW**	Vertical Sync Pulse Width. The unit is Horizontal Sync. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x0A

Bit	R/W	Symbol	Description	Reset Value
ISP Sync Control Register(ISP_ HPERIOD) ***Address : C000 300Ah***				
[14:0]	R/W	**ISP_HPERIOD**	Horizontal Sync Period. The unit is ISP_CLK. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x187
ISP Sync Control Register(ISP_ HPW) ***Address : C000 300Ch***				
[15:9]	R/W	**ISP_EAV2HSYNC**	Horizontal EAV(End of Active Video) to Horizontal Sync Starting point. The unit is ISP_CLK. Effective when in CCIR655 Mode.	0x10
[8:0]	R/W	**ISP_HPW**	Horizontal Sync Pulse Width. The unit is ISP_CLK. Effective when in Sync output mode (ISP_SYNC_DIR = 1)	0x32
ISP Sync Control Register(ISP_HACT_ST) ***Address : C000 300Eh***				
[12:0]	R/W	**ISP_HACT_ST**	Horizontal Active Data Start Point from Falling Horizontal Sync.	0x0B
ISP Sync Control Register(ISP_H_WIDTH) ***Address : C000 3010h***				
[12:0]	R/W	**ISP_H_WIDTH**	Horizontal active data end point from falling horizontal sync	0x14B
ISP Sync Control Register(ISP_VACT_ST) ***Address : C000 3012h***				
[12:0]	R/W	**ISP_VACT_ST**	Vertical Active Data Start Point from Falling Vertical Sync	0x0A
ISP Sync Control Register(ISP_V_HEIGHT) ***Address : C000 3014h***				
[12:0]	R/W	**ISP_V_HEIGHT**	Vertical Active Data End Point from Falling Vertical Sync	0x0FA
Image Signal Processor Source Pixel Width Register (ISP_SRC_HWIDTH) ***Address : C000 3016h***				
[15:0]	R/W	**ISP_ SRC_HWIDTH**	ISP Horizontal Memory Width of Source Pixel. The unit is Byte (pixel width) x 1, when 8bits BAYERRGB (pixel width) x 2, when 16bits BAYERRGB (pixel width) x 3, when 8bits RGB (pixel width) x 6, when 16bits RGB	0x00
Processing Window Control Register(ISP_RGBSV) ***Address : C000 3018h***				
[12:0]	R/W	**ISP_RGBSV**	Vertical Stating point of processing window from falling edge of Vertical Sync. The unit is Horizontal Sync	0x05
Processing Window Control Register(ISP_RGBEV) ***Address : C000 301Ah***				
[12:0]	R/W	**ISP_RGBEV**	Vertical Ending point of processing window from falling edge of Vertical Sync. The unit is Horizontal Sync	0xFF

Bit	R/W	Symbol	Description	Reset Value
Processing Window Control Register(ISP_RGBSH) ***Address : C000 301Ch***				
[12:0]	R/W	**ISP_RGBSH**	Horizontal Stating point of processing window from falling edge of Horizontal Sync The unit is ISP_CLK	0x05
Processing Window Control Register(ISP_RGBEH) ***Address : C000 301Eh***				
[14:0]	R/W	**ISP_RGBEH**	Horizontal Ending point of processing window from falling edge of Horizontal Sync The unit is ISP_CLK	0x14F
Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESV) ***Address : C000 3020h***				
[12:0]	R/W	**ISP_AESV**	Vertical starting point for auto exposure/white balance accumulation from falling edge of Vertical Sync.	0x0A
Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEV) ***Address : C000 3022h***				
[12:0]	R/W	**ISP_AEEV**	Vertical ending point for auto exposure/white balance accumulation from falling edge of Vertical Sync.	0x0FA
Auto Exposure/White Balance Accumulation Window Control Register(ISP_AESH) ***Address : C000 3024h***				
[12:0]	R/W	**ISP_AESH**	Horizontal starting point for auto exposure/white balance accumulation from falling edge of Horizontal Sync	0x0FA
Auto Exposure/White Balance Accumulation Window Control Register(ISP_AEEH) ***Address : C000 3026h***				
[12:0]	R/W	**ISP_AEEH**	Horizontal ending point for auto exposure/white balance accumulation from falling edge of Horizontal Sync	0x14A
Auto Exposure Accumulation Control Register(ISP_AELIM) ***Address : C000 3028h***				
[15:8]	R/W	**ISP_AEULIM**	Upper limit for auto exposure accumulation.	0xFF
[7:0]	R/W	**ISP_AELLIM**	Lower limit for auto exposure accumulation.	0x00
Auto Exposure Accumulation Control Register(ISP_ AEVSTEP) ***Address : C000 302Ah***				
[9:0]	R/W	**ISP_AEVSTEP**	Vertical step for exposure accumulation is fixed with 4. ISP_AEVSTEP = (ISP_AEEV – ISP_AESV) / 4	0x3C
Auto Exposure Accumulation Control Register(ISP_ AEHSTEP) ***Address : C000 302Ch***				
[9:0]	R/W	**ISP_AEHSTEP**	Horizontal step for exposure accumulation is fixed with 4. ISP_AEHSTEP = (ISP_AEEH – ISP_AESH) / 4	0x50

Bit	R/W	Symbol	Description	Reset Value
Auto Focus Accumulation Window Control Register(ISP_ AFSV) ***Address : C000 302Eh***				
[12:0]	R/W	**ISP_AFSV**	Vertical starting window point for auto focus accumulation from falling edge of Vertical Sync.	0x0A
Auto Focus Accumulation Window Control Register(ISP_ AFEV) ***Address : C000 3030h***				
[12:0]	R/W	**ISP_AFEV**	Vertical ending window point for auto focus accumulation from falling edge of Vertical Sync.	0xFA
Auto Focus Accumulation Window Control Register(ISP_ AFSH) ***Address : C000 3032h***				
[12:0]	R/W	**ISP_AFSH**	Horizontal starting window point for auto focus accumulation from falling edge of Horizontal Sync.	0xFA
Auto Focus Accumulation Window Control Register(ISP_ AFEH) ***Address : C000 3034h***				
[12:0]	R/W	**ISP_AFEH**	Horizontal ending window point for auto focus accumulation from falling edge of IHSYNC.	0x14A
Contrast Control Register(ISP_CNTRSTGAIN) ***Address : C000 3036h***				
[3]	R/W	**ISP_ CNTRSTACCEN**	Accumulation Enable Signal for auto Contrast Control.	0x0
[2:0]	R/W	**ISP_CNTRSTGAIN**	Contrast Gain Control 0 : 0.25, 1 : 0.5, 2 : 0.75, 3 : 1.0, 4 : 1.25, 5 : 1.5, 6 : 1.75, 7 : 2.0	0x3
Contrast Control Register(ISP_CNTRSTLIM) ***Address : C000 3038h***				
[15:8]	R/W	**ISP_CNTRUL**	Upper limit for auto contrast accumulation.	0xFF
[7:0]	R/W	**ISP_CNTRLL**	Lower limit for auto contrast accumulation.	0x00
Bayer RGB Recovery Method (ISP_RGBREC) ***Address : C000 303Ah***				
[15:9]	-	**Reserved**	Reserved with 0	
[8]	R/W	**ISP_R_REC_TYPE**	R Pixel Recovery Type 0 : median filter 1 : Average	0
[7:5]	R/W	**ISP_G_REC_TYPE**	G Pixel Recovery Type 000 : Average Left and Right 001 : Average UP and DOWN 010 : Median Filter 011 : Average Left , Right, Up and Down,	010
[4]	R/W	**ISP_B_REC_TYPE**	B Pixel Recovery Type	0

Bit	R/W	Symbol	Description	Reset Value
			0 : median filter 1 : Average	
[3:2]	R/W	**ISP_BAYER_ODR**	Bayer RGB Array Type 00 : FIRST_GB 01 : FIRST_BG 10 : FIRST_RG 11 : FIRST_GR	00
[1]	R/W	**ISP_CBRSWAP**	Cb/Cr Swap 0 : normal 1 : swap	0
[0]	R/W	**ISP_VID_RANGE**	Video Range 0 : Y = 219 /256 x Y (0 ~ 255) + 16 Cb = 224/256 x Cb (0 ~ 255) Cr = 224/256 x Cr (0 ~ 255) 1 : Y = Y(0 ~ 255) Cb = Cb(0 ~ 255) Cr = Cr(0 ~ 255) 	0
Hue Control of Each 4 Coordinate (ISP_HUECBnAB) ***Address : C000 3040h / C000 3044h / C000 3048h / C000 304Ch***				
[15:8]	R/W	**ISP_HUECBnA**	Gain is -2 to +2 Decimal Point = [6.5][1] 2's complement	0x40
[7:0]	R/W	**ISP_HUECBnB**	Gain is –2 to +2 Decimal Point = [6.5][1] 2's complement	0x00
			At each Coordinate, input the result of following equations. (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer the Figure 16-8. The basic concept of Hue control	
Hue Control of Each of 4 Coordinates (ISP_HUECRnAB) ***Address : C000 3042h / C000 3046h / C000 304Ah / C000 304Eh***				

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**ISP_HUECRnA**	Gain is -2 to +2, Decimal Point = [6.5] (1) 2's complement	0x00
[7:0]	R/W	**ISP_HUECRnB**	Gain is -2 to +2, Decimal Point = [6.5] (1) 2's complement	0x40
			At each Coordinate, input the result of following equations. (B-Y)' = (B-Y) x HUECBn_A + (R-Y) x HUECBn_B (R-Y)' = (B-Y) x HUECRn_A + (R-Y) x HUECRn_B Refer the Figure 16-8. The basic Concept of Hue Control	
Note 1: Decimal Point = [6.5]: 8 bits = [2^1 2^0 1/2 1/4 1/8 1/16 1/32 1/64] for example. "0100_0000"=64/64=1, "0010_0000"=32/64=0.5, "1000_0000"=(-128)/64=(-2), "1100_0000"=(-64)/64=(-1)				
Horizontal Luminance Enhancement Gain (ISP_YGAIN) ***Address : C000 3054***				
[6:4]	R/W	**ISP_YEDGEGAIN**	Horizontal Edge Gain 0 = 0.0, 1 = 1.0, 2 = 1.5, 3 = 2.0, 4 = 2.5, 5 = 3.0, 6 = 3.5, 7 = 4.0,	0x01
[3]		**Reserved**	-	-
[2:0]	R/W	**ISP_YMAINGAIN**	Horizontal Main path 0 = 0.0, 1 = 0.5, 2 = 0.75 3 = 1.0, 4 = 1.25, 5 = 1.5, 6 = 1.75 7 = 2.0,	0x03
Horizontal Chrominance Delay Control (ISP_CDLY) ***Address : C000 3056h***				
[15:3]		**Reserved**	-	-
[2:0]	R/W	**ISP_CDLY**	Horizontal Chrominance Delay The unit is ISP_CLK. 0 ~ 4 5 ~ 7 : Reserved	0x00
Brightness Control (ISP_BRIGHT) ***Address : C000 3058h***				
[7:0]	R/W	**ISP_BRIGHT**	Range = -128 ~ 127	0x00
Clip Point & Color suppress (ISP_YCLIP) ***Adress : C000 305Ah***				
[15:8]	R/W	**ISP_CLIP2**	ISP_Clip2 = High Clip, Range = 0 ~ 255	0xFF
[7:0]	R/W	**ISP_CLIP1**	ISP_Clip1 = Clip knee, Range = 0 ~ 255 If ISP_Clip1 = ISP_Clip2 = 255, then CLIP OFF.	0xFF

Bit	R/W	Symbol	Description	Reset Value
Clip Point & Color suppress (ISP_YCLIPSLANT) ***Address : C000 305Ch***				
[2:0]	R/W	**ISP_CLIPSLANT**	Slant between ISP_CLIP1 and ISP_CLIP2 0 = 0.0 1 = 0.125, 2 = 0.250 3 = 0.375 4 = 0.5 5 = 0.625, 6 = 0.75 7 = 0.875	0x4
Clip Point & Color suppress (ISP_CSUPSLANT) ***Address : C000 305Eh***				
[15]	R/W	**ISP_CSLANT_EN**	Color Suppress enable bit. 0 : Disable 1 : Enable	0
[14]	R/W	**ISP_DECI_OFF**	Chrominance Decimation Filter Off 0 : Filter On 1 : Filter Off	0
[13:3]	R/W	**Reserved**	-	-
[2:0]		**ISP_CSLANT_PNT**	Suppress Gain Control	0x4
Horizontal Edge Enhancement (ISP_Limet) ***Address : C000 3060h***				
[7:0]	R/W	**ISP_SLICELMT**	The signal in the area of Slice Limit will be zero, This is used for reducing noise. Range = 0 ~ 255	0x08
Upper/ Lower Limit for White Balance Accumulation (ISP_WBLMT) ***Address : C000 3062h***				
[15:8]	R/W	**ISP_WB_ULMT**	Upper Limit value of Luminance Level for White Balance Accumulation	0xFF
[7:0]	R/W	**ISP_WB_LLMT**	Lower Limit value of Luminance Level for White Balance Accumulation	0x00
Upper/ Lower Limit for White Balance Accumulation (ISP_WBACCCNTH, ISP_WBACCCNTL) ***Address : C000 3064h / C000 3066h***				
[7:0]	R	**ISP_WBACCCNTH**	Upper 8 bits	0x00
[15:0]	R	**ISP_WBACCCNTL**	Lower 16 bits	0x00
			The total number of pixels which are in the white balance area.	
Upper/ Lower Limit for White Balance Accumulation (ISP_WBCBACCH, ISP_WBCBACCL) ***Address : C000 3068h / C000 306Ah***				
[15:0]	R	**ISP_WBCBACCH**	Upper 16 bits	0x00
[15:0]	R	**ISP_WBCBACCL**	Lower 16 bits	0x00
			The number of Cb pixels which are in the white balance area	
Upper/ Lower Limit for White Balance Accumulation (ISP_WBCRACCH, ISP_WBCRACCL) ***Address : C000 306Ch / C000 306Eh***				
[15:0]	R	**ISP_WBCRACCH**	Upper 16 bits	0x00

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_WBCRACCL**	Lower 16 bits	0x00
			The number of Cr pixels which are in the white balance area	
Auto Focus Accumulation (ISP_AFACCL, ISP_AFACCH) ***Address : C000 3070h / C000 3072h***				
[15:0]	R	**ISP_AFACCH**	Auto Focus Accumulation	0x00
[15:0]	R	**ISP_AFACCL**	Auto Focus Accumulation	0x00
			The number of Edge(Output of band pass filter) in auto focus area	
Color Coordinate Selection for White Balance (ISP_WBCOORD0) ***Address : C000 3076h***				
[15:0]	R/W	**ISP_WBCOORD0**	Set white balance pattern (1), 0 block setting ,	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD1) ***Address : C000 3078h***				
[15:0]	R/W	**ISP_WBCOORD1**	Set white balance pattern (1), 16~31 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD2) ***Address : C000 307Ah***				
[15:0]	R/W	**ISP_WBCOORD2**	Set white balance pattern (1), 32~47 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD3) ***Address : C000 307Ch***				
[15:0]	R/W	**ISP_WBCOORD3**	Set white balance pattern (1), 48~63 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD4) ***Address : C000 307Eh***				
[15:0]	R/W	**ISP_WBCOORD4**	Set white balance pattern (1), 64~79 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD5) ***Address : C000 3080h***				
[15:0]	R/W	**ISP_WBCOORD5**	Set white balance pattern (1), 80~95 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD6) ***Address : C000 3082h***				
[15:0]	R/W	**ISP_WBCOORD6**	Set white balance pattern (1), 96~111 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD7) ***Address : C000 3084h***				
[15:0]	R/W	**ISP_WBCOORD7**	Set white balance pattern (1), 112~127 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD8) ***Address : C000 3086h***				
[15:0]	R/W	**ISP_WBCOORD8**	Set white balance pattern (1), 128~143 block setting	0x00

Bit	R/W	Symbol	Description	Reset Value
Color Coordinate Selection for White Balance (ISP_WBCOORD9) ***Address : C000 3088h***				
[15:0]	R/W	**ISP_WBCOORD9**	Set white balance pattern (1), 144~159 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD10) ***Address : C000 308Ah***				
[15:0]	R/W	**ISP_WBCOORD10**	Set white balance pattern (1), 160~175 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD11) ***Address : C000 308Ch***				
[15:0]	R/W	**ISP_WBCOORD11**	Set white balance pattern (1), 176~191 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD12) ***Address : C000 308Eh***				
[15:0]	R/W	**ISP_WBCOORD12**	Set white balance pattern (1), 192~207 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD13) ***Address : C000 3090h***				
[15:0]	R/W	**ISP_WBCOORD13**	Set white balance pattern (1), 208~223 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD14) ***Address : C000 3092h***				
[15:0]	R/W	**ISP_WBCOORD14**	Set white balance pattern (1), 224~239 block setting	0x00
Color Coordinate Selection for White Balance (ISP_WBCOORD15) ***Address : C000 3094h***				
[15:0]	R/W	**ISP_WBCOORD15**	Set white balance pattern (1), 240~255 block setting	0x00
Note 1: For example, If you want to enable block 0, 3, 8, 9 in ISP_WBCOORDn, Use ISP_WBCOORDn = (1 << 0) + (1 << 3) + (1 << 8) + (1<<9).				
External Memory Address (ISP_MEMADDRL1, ISP_MEMADDRH1) ***Address : C000 3096h / C000 3098h***				
[31:0]	R/W	**ISP_MEMADDR1**	When External Device to Memory Mode, Destination Address. When Memory to Memory Mode, Source Address.	0x00
External Memory Address (ISP_MEMADDRL2, ISP_MEMADDRH2) ***Address : C000 30Eeh / C000 30F0h***				
[31:0]	R/W	**ISP_MEMADDR2**	When Memory to Memory Mode, Destination Address.	0x00
Gamma Table Control (ISP_GAMMA) ***Address : C000 309Ah***				
[9:0]	R/W	**ISP_GAMMA_A**	Address Interface of Gamma Table	0x00
Gamma Table Control (ISP_GAMMD) ***Address : C000 309Ch***				

Bit	R/W	Symbol	Description	Reset Value
[9:0]	R/W	**ISP_GAMMA_D**	Data Interface of Gamma Table The address will increase automatically after write the Data	0x00
Auto Exposure Result (ISP_AEACCH) ***Adress : C000 309Eh***				
[15:13]	-	**Reserved**	-	-
[12:0]	R	**ISP_AEACCH**	High 13 bits (Map Address[1:0] = 10)	0x00
Auto Exposure Result (ISP_AEACCL) ***Adress : C000 30DCh***				
[15:0]	R	**ISP_AEACCL**	Low 16 bits (Map Address[1:0] = 00)	0x00
			Total Block Number is 16 words. Bits per block are total 29 bits.	
Luminance Contrast Information (ISP_CNTST_LLCNTL, ISP_CNTST_LLCNTH) ***Address : C000 30DEh ~ C000 30E0h***				
[15:0]	R	**ISP_CNTST_ LLCNTL**	The total number of pixels which are in the Low Limit value of Luminance Level. low bits [15:0]	0x00
[7:0]	R	**ISP_CNTST_ LLCNTH**	The total number of pixels which are in the Low Limit value of Luminance Level. High bits [23:16]	0x00
Luminance Contrast Information (ISP_CNTST_HLCNTL, ISP_CNTST_HLCNTH) ***Address : C000 30E2h ~ C000 30E4h***				
[15:0]	R	**ISP_CNTST_ HLCNT_L**	The total number of pixels which are in the High Limit value of Luminance Level low bits [15:0]	0x00
[7:0]	R	**ISP_CNTST_ HLCNT_H**	The total number of pixels which are in the High Limit value of Luminance Level High bits [23:16]	0x00
Luminance Contrast Information (ISP_CNTST_LLACCL, ISP_CNTST_LLACCH) ***Address : C000 30E6h ~ C000 30E8h***				
[15:0]	R	**ISP_CNTST_ LLACC_L**	The accumulated data which is in the low Limit value of Luminance Level low bits [15:0]	0x00
[15:0]	R	**ISP_CNTST_ LLACC_H**	The accumulated data which is in the low Limit value of Luminance Level High bits [31:16]	0x00
Luminance Contrast Information (ISP_CNTST_HLACCL, ISP_CNTST_HLACCH) ***Address : C000 30EAh ~ C000 30ECh***				

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R	**ISP_CNTST_ HLACC_L**	The accumulated data which is in the high Limit value of Luminance Level low bits [15:0]	0x00
[15:0]	R	**ISP_CNTST_ HLACC_H**	he accumulated data which is in the high Limit value of Luminance Level High bits [31:16]	0x00
External Memory Address for BayerRGB to RGB (ISP_MEMRGBADDRL, ISP_MEMRGBADDRH) ***Address : C000 30EEh ~ C000 30F0h***				
[15:0]	R/W	**ISP_MEMRGBADD RH**	When Memory to Memory Mode, Destination Address	0x00
[15:0]	R/W	**ISP_MEMRGBADD RL**	When Memory to Memory Mode, Destination Address	0x00
Image Signal Processor Destination Pixel Width Register (ISP_DST_HWIDTH) ***Address : C000 30F2H***				
[15:0]	R/W	**ISP_DST_HWIDTH**	ISP Horizontal Memory Width of Destination Pixel. The unit is Byte (pixel width) X 1, when 8bits BAYERRGB (pixel width) X 2, when 16bits BAYERRGB (pixel width) X 3, when 8bits RGB (pixel width) X 6, when 16bits RGB	0x00

TABLE 16-70. IMAGE SIGNAL PROCESSOR REGISTERS LIST

CHAPTER 17

PULSE WITH MODULATOR

17. PULSE WITH MODULATOR

17.1 OVERVIEW

The MP2520F has four Pulse Width Modulators (PWM). Each PWM operates respectively and is controlled by its own register set. Each channel outputs the pulse width modulated signal via an external pin. Four PWMs have the same circuit architectures and, hereinafter, will be described as PWMn (n = 0, 1, 2, 3)

Each PWM Channel has a 7-bit Prescaler. The Prescaler receives the Clock provided by the Power Management and divides the Clock with the value specified by the PWMnPERIOD, and then produces the Clock for carrying out the PWM operation.

In addition, each PWM Channel has a Counter composed of 10 bits. The CPU can produce the desired signal by specifying the period and the duty of a PWM Waveform in the PWMnPERIOD and PWMnDUTY registers.

When the specified value in the PWMnPERIOD corresponds to the DUTY Counter value, the PWM resets the Counter and sets the PWM Signal to '0'.

When the specified value in the PWMnDUTY corresponds to the DUTY Counter value, the PWM sets the PWM Signal to '1'.

The PWMnPOL determines whether to Invert or Bypass the value before the PWM Signal produced in the pertinent Channel goes out through the external PAD.

FEATURES

- 4 Pulse Width Modulator channels
- 7-Bit Clock Divider & 10-Bit Period Counter
- 10-Bit Duty Counter

BLOCK DIAGRAM

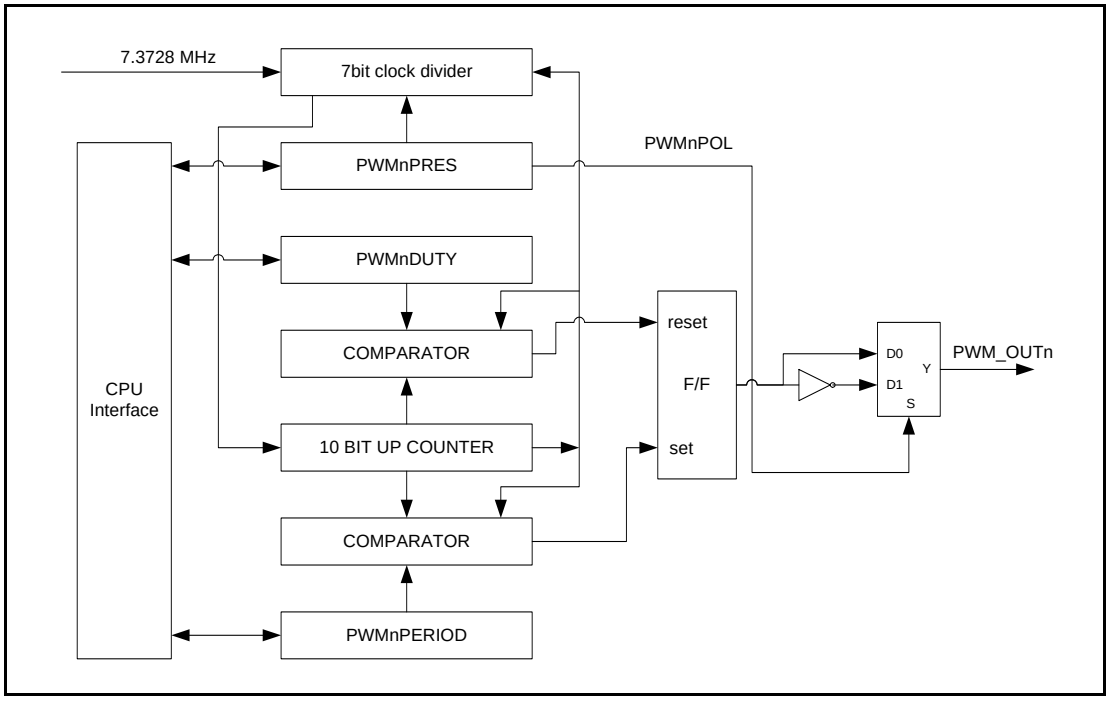


Figure 17-1. PWM Block Diagram

17.2 PWM SIGNAL

As shown below, the 10-bit DUTY Counter is reset by the PWMnPERIOD, and the PWM Signal is changed to '0'. When the PWMnDUTY register value corresponds to the DUTY Counter value, the PWM Signal is set to '1'.

If the value specified by the PWMNDUTY is bigger than the PWMnPERIOD value, the PWM Signal is always "0".

If the PWMnDUTY is set to "0", the PWM Signal is always "1".

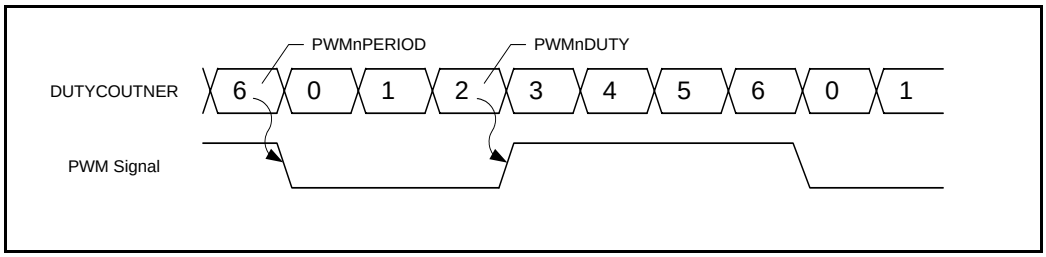


Figure 17-2. PWM Signal Timing Diagram

17.3 PWM CONTROLLER REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
PWM Prescale0/1 Register (PWM_PRES01) ***Address : C000 0B00h***				
15	RW	**PWM1POL**	This bit determines the polarity of PWM signal 0: Inverted 1: Bypass	0
14:8	RW	**PWM1PRESCALE**	These 7 bits determine the prescaler value for PWM1	0
7	RW	**PWM0POL**	This bit determine the polarity of PWM signal 0: Inverted 1: Bypass	0
6:0	RW	**PWM0PRESCALE**	These 7 bits determine the prescaler value for PWM0	0
PWM0 Duty Cycle (PWM_DUTY0) ***Address : C000 0B02h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM0DUTY**	Set the length of PWM Signal Low area Set 0, PWM Output is 1 Set bigger then PWMnPERIOD, PWM Output is 0	0
PWM1 Duty Cycle (PWM_DUTY1) ***Address : C000 0B04h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM1DUTY**	Set the length of the PWM Signal Low area If set to 0, PWM Output is 1 If set bigger than PWMnPERIOD, PWM Output is 0	0
PWM0 Period Cycle (PWM_PERIOD0) ***Address : C000 0B06h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM0PERID**	Set the Period of the PWM Signal	0
PWM1 Period Cycle (PWM_PERIOD1) ***Address : C000 0B08h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM1PERID**	Set the Period of the PWM Signal	0
PWM Prescale2/3 Register (PWM_PRES23) ***Address : C000 0B10h***				
15	RW	**PWM3POL**	This bit determines the polarity of the PWM Signal 0: Inverted 1: Bypass	0

Bit	R/W	Symbol	Description	Reset Value
14:8	RW	**PWM3PRESCALE**	These 7 bits determine the prescaler value for PWM1	0
7	RW	**PWM2POL**	This bit determines the polarity of the PWM Signal 0: Inverted 1: Bypass	0
6:0	RW	**PWM2PRESCALE**	These 7 bits determine the prescaler value for PWM0	0
PWM2 Duty Cycle (PWM_DUTY2) ***Address : C000 0B02h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM2DUTY**	Set the length of PWM Signal Low Area If set to 0, the PWM Output is 1 If set bigger than PWMnPERIOD , the PWM Output is 0	0
PWM3 Duty Cycle (PWM_DUTY3) ***Address : C000 0B14h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM3DUTY**	Set the length of PWM Signal Low Area If set to 0, the PWM Output is 1 If set bigger than PWMnPERIOD , the PWM Output is 0	0
PWM2 Period Cycle (PWM_PERIOD2) ***Address : C000 0B16h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM2PERID**	Set the Period of PWM Signal	0
PWM3 Period Cycle (PWM_PERIOD3) ***Address : C000 0B18h***				
15:10	R	**Reserved**	-	-
9:0	RW	**PWM3PERID**	Set the Period of PWM Signal	0

TABLE 17-1. PULSE WITH MODULATOR REGISTERS LIST

CHAPTER 18

PULSE PERIOD MEASUREMENT (PPM)

18. PULSE PERIOD MEASUREMENT (PPM)

18.1 OVERVIEW

The Pulse Period Measurement (PPM) measures the period of the high level and the low level of a 1-bit Signal entered from the outside.

The PPM can produce each interrupt at the Rising edge and the Falling edge in the signal entered. If the high or low period is too long to be measured by the counter in the PPM, Overflow interrupt can occur.
The PPM block uses the Clock signal from XTI input pin (7.3728 MHz)

FEATURES

- 16-bit Pulse Period Measurement Counter
- Overflow Check
- Control Input Polarity

BLOCK DIAGRAM

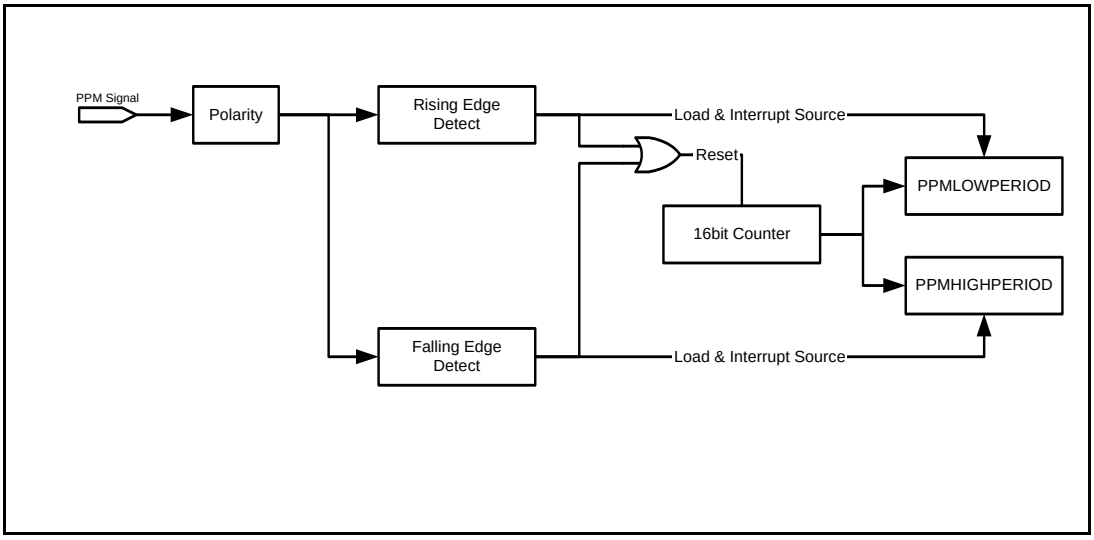


Figure 18-1. PPM Block Diagram

18.2 OPERATION

The Polarity block in PPM is for adjusting the input signal polarity by PPMINPOL bit.
When Rising edge is detected, the counter value.

If a Rising Edge is detected, ine 16-bit Counter is stored in the PPMLOWPERIOD so that the CPU can read the time for the Low level just before the rising edge.

When Falling Edge is detected, the counter value in 16-bit Counter is stored in the PPMHIGHPERIOD so that CPU can read the time for the High level just before the falling edge. If the Low period or the High period is so long that the 16-bit Counter cannot measure the entered signal, the 16-bit Counter is overflowed and the status of the overflow is stored. Then the production of the Overflow interrupt in the Low period or the High Period is transferred to the CPU.

The PPMINT interrupt can be selected either on the Falling Edge, on the Rising Edge, or when Overflow occurs.

18.3 PPM CONTROLLER REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
PPM Control Register (PPMCTRL) ***Address : 0xC000 3E00***				
15	R/W	**PPMENB**	PPM Module Enable 0 : Disable 1 : Enable	-
14	R/W	**PPMINPOL**	Control Polarity of PPM Input Signal 0 : Invert 1 : Bypass	
13 : 3	R	**Reserved**		
2	R/W	**PPMIRQO**	Overflow Interrupt Enable 0 : Disable 1 : Enable	-
1	R/W	**PPMIRQF**	Falling Edge Detect Interrupt Enable 0 : Disable 1 : Enable	-
0	R/W	**PPMIRQR**	Rising Edge Detect Interrupt Enable 0 : Disable 1 : Enable	0
PPM Status Register (PPMSTATUS) ***Address : 0xC000 3E04***				
15 : 5	R/W	**Reserved**		-
4	R/W	**PPMOVERLOW**	Indicate Overflow in Low 0 : Normal 1 : Overflow	0
3	R/W	**PPMOVERHIGH**	Indicate Overflow in High 0 : Normal 1 : Overflow	
2	R/W	**PPMPENDO**	Overflow Interrupt Pending Bit, Set to 1 to clear this bit 0 : None 1 : Detected	
1	R/W	**PPMPENDF**	Falling Edge Detect Interrupt Pending Bit 0 : None 1 : Detected	
0	R/W	**PPMPENDR**	Rising Edge Detect Interrupt Pending Bit 0 : None 1 : Detected	
PPM Low Period Register (PPMLOWPERIOD) ***Address : 0xC000 3E06***				
15 :0	R	**PPMLOWPERIOD**	Read Counter Value of Low	-
PPM High Period Register (PPMHIGHPERIOD) ***Address : 0xC000 3E08***				
15 : 0	R	**PPMHIGHPERIOD**	Read Counter Value of High	-

TABLE 18-1. PPM CONTROLLER REGISTERS LIST

MAGIC EYES

CHAPTER 19

USB HOST / DEVICE

19. USB HOST / DEVICE

19.1 USB HOST

19.1.1 Overview

A 3-port USB host interface is supported by the MP2520F as follows:

- Open Rev.1.0 compatible.
- USB Rev. 1.1 compatible.
- 3 downstream ports.
- Support for both LowSpeed and HighSpeed USB devices.

BLOCK DIAGRAM

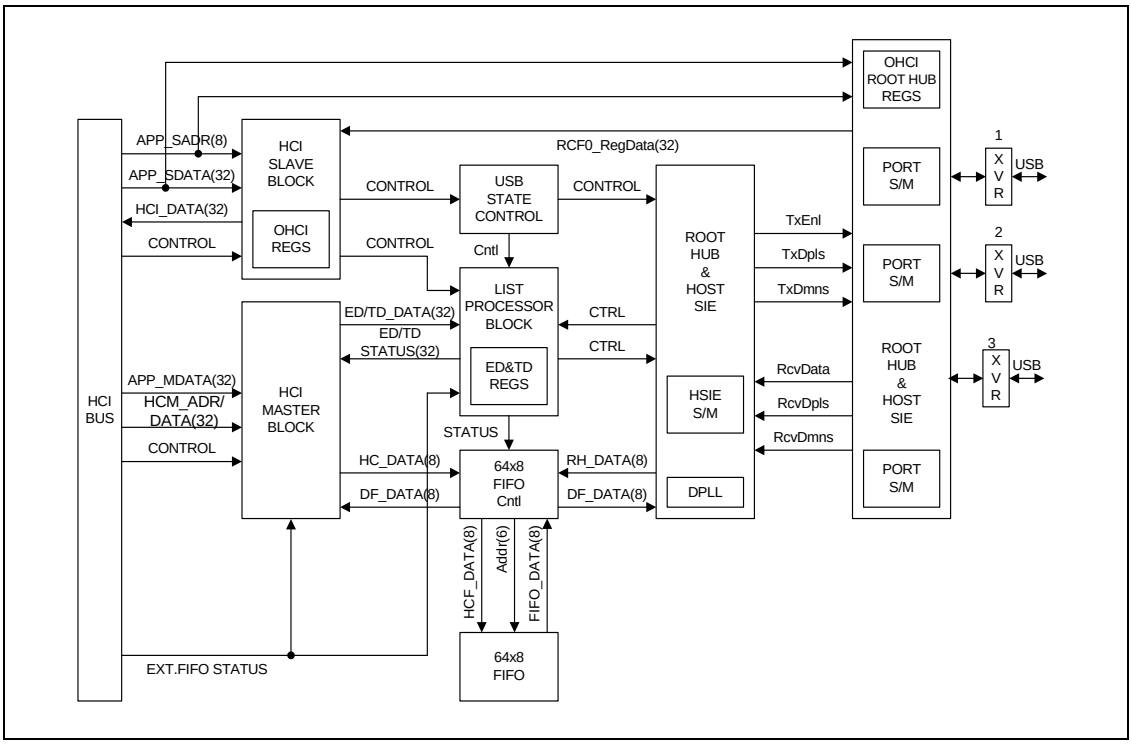


Figure 19-1. USB Host Controller Block Diagram

19.1.2 USB HOST CONTROL REGISTER

The MP2520F USB Host controller meets OPEN HCI, Rev. 1.0. For detail information, refer to the Open Host Controller Interface, Rev. 1.0.

OHCI REGISTERs for USB Host Controller

Register	Address	Description
HcRevision	0xC0004300	Control and status group
HcControl	0xC0004304	
HcCommonStatus	0xC0004308	
HcInterruptStatus	0xC000430C	
HcInterruptEnable	0xC0004310	
HcInterruptDisable	0xC0004314	
HcHCCA	0xC0004318	Memory pointer group
HcPeriodCurrentED	0xC000431C	
HcControlHeadED	0xC0004320	
HcControlCurrentED	0xC0004324	
HcBulkHeadED	0xC0004328	
HcBulkCurrentED	0xC000432C	
HcDoneHead	0xC0004330	
HcRmInterval	0xC0004334	Frame counter group
HcFmRemaining	0xC0004338	
HcFmNumber	0xC000433C	
HcPeriodicStart	0xC0004340	
HcLSThreshold	0xC0004344	
HcRhDescriptorA	0xC0004348	Root hub group
HcRhDescriptorB	0xC000434C	
HcRhStatus	0xC0004350	
HcRhPortStatus1	0xC0004354	
HcRhPortStatus2	0xC0004358	

TABLE 19-1. OHCI REGISTERS FOR USB HOST CONTROLLER

19.2 USB DEVICE

19.2.1 OVERVIEW

- A high-performance, full-speed function controller solution is supported by the USB function controller via a DMA interface. The bulk transfer, interrupt transfer and control transfer that uses DMA are supported by the USB function controller. The following are the specifications of the USB function controller: Full Speed USB Function Controller compatible with the USB Specification Version 1.1.
- DMA Interface for Bulk Transfer.
- 5 Endpoints with FIFO
  EP0: 16byte (Register)
  EP1: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP2: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP3: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP4: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  Integrated USB Transceiver.

FEATURES

- Fully compliant with USB Specification, Version 1.1.
- Full Speed (12Mbps) Device.
- Integrated USB Transceiver.
- Supports control, interrupt, and bulk transfer.
- 5 Endpoints with FIFO:
  One bi-directional control endpoint with 16 byte FIFO (EP0)
  Four bi-directional bulk endpoints with 64byte FIFO (EP1, EP2, EP3, EP4).
- Supports DMA interface for receiving and transmitting bulk endpoints (EP1, EP2, EP3, EP4).
- Independent 64byte receiving and transmitting FIFO to maximize throughput.
- Supports suspend and remote wake-up function.
- USB device operating frequency: 48MHz.

BLOCK DIAGRAM

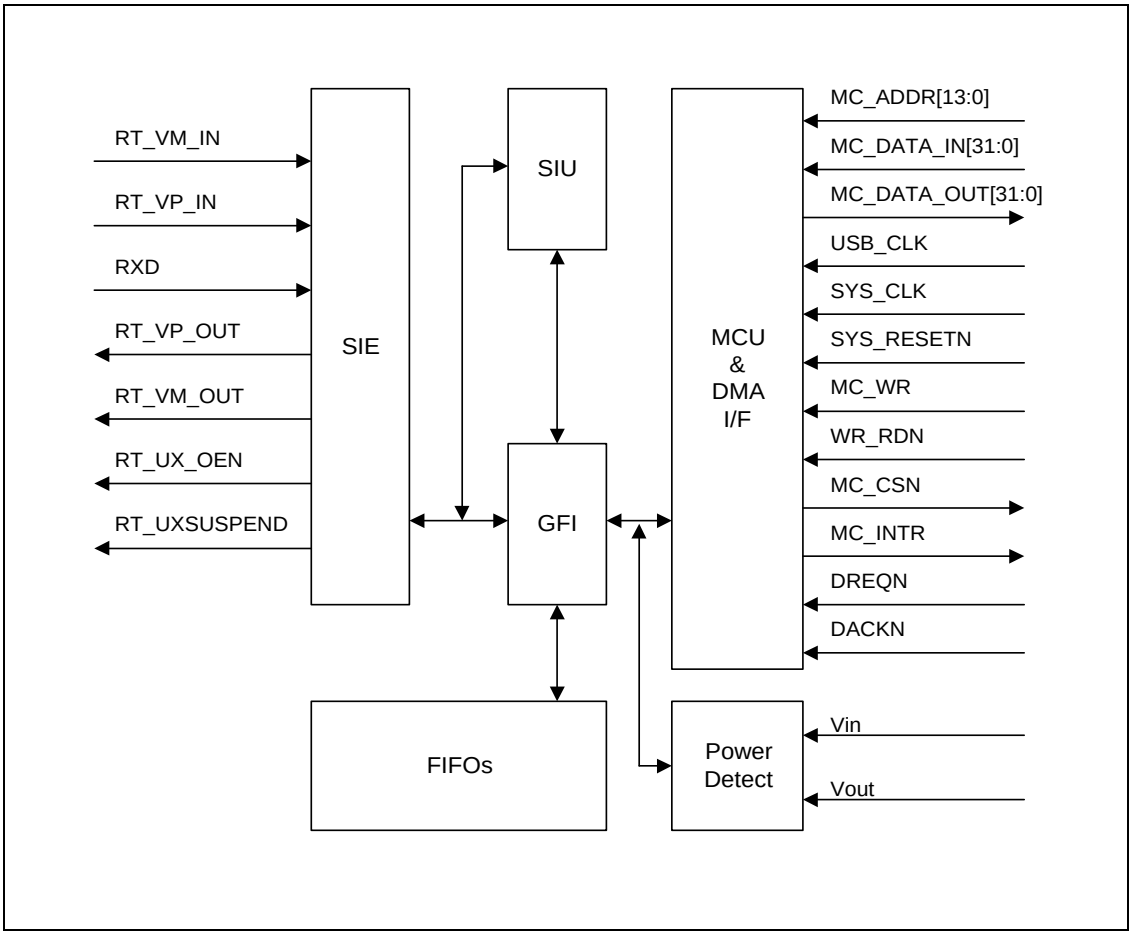


Figure 19-2. USB Device Block Diagram

19.2.2 OPERATION

It is recommended that you refer to Universal Serial Bus Specification. Rev. 11.1for further information.

19.2.2.1 USB DEVICE SPECIAL REGISTERS.

Detail functionality of the register set of the USB device controller is described in this section. All special function registers are byte-accessible or word accessible. All reserved bits are zero. Common indexed registers depend on the INDEX register (INDEX_REG) (offset address; 0X141c) value. EX: Before writing to the IN_CSR1 register, you must write '0x00' to the INDEX_REG if you want to write to the EPO CSR register.

NOTE: All registers should be reconfigured after Host Reset Signaling.

Register Name	Description	Offset Address
	NON INDEXED REGISTERS	
FUNC_ADDR_REG	Function address register	0x1400
PWR_REG	Power management register	0x1402
EP_INT_REG (EP0–EP4)	Endpoint interrupt register	0x1404
USB_INT_REG	USB interrupt register	0x140C
EP_INT_EN_REG (EP0–EP4)	Endpoint interrupt enable register	0x140e
USB_INT_EN_REG	USB interrupt enable register	0x1416
FRAME_NUM1_REG	Frame number 1 register	0x1418
FRAME_NUM2_REG	Frame number 2 register	0x141a
INDEX_REG	Index register	0x141c
EP0_FIFO_REG	Endpoint0 FIFO register	0x1440
EP1_FIFO_REG	Endpoint1 FIFO register	0x1442
EP2_FIFO_REG	Endpoint2 FIFO register	0x1444
EP3_FIFO_REG	Endpoint3 FIFO register	0x1446
EP4_FIFO_REG	Endpoint4 FIFO register	0x1448
EP1_DMA_CON	Endpoint1 DMA control register	0x1460
-	reserved	0x1462
EP1_DMA_FIFO	Endpoint1 DMA FIFO counter register	0x1464
EP1_DMA_TTC_L	Endpoint1 DMA transfer counter low-byte register	0x1466
EP1_DMA_TTC_M	Endpoint1 DMA transfer counter middle-byte register	0x1468
EP1_DMA_TTC_H	Endpoint1 DMA transfer counter high-byte register	0x146a
EP2_DMA_CON	Endpoint2 DMA control register	0x146c
-	reserved	0x146e
EP2_DMA_FIFO	Endpoint2 DMA FIFO counter register	0x1470
EP2_DMA_TTC_L	Endpoint2 DMA transfer counter low-byte register	0x1472
EP2_DMA_TTC_M	Endpoint2 DMA transfer counter middle-byte register	0x1474
EP2_DMA_TTC_H	Endpoint2 DMA transfer counter high-byte register	0x1476
EP3_DMA_CON	Endpoint3 DMA control register	0x1480
-	reserved	0x1482

Register Name	Description	Offset Address
EP3_DMA_FIFO	Endpoint3 DMA FIFO counter register	0x1484
EP3_DMA_TTC_L	Endpoint3 DMA transfer counter low-byte register	0x1486
EP3_DMA_TTC_M	Endpoint3 DMA transfer counter middle-byte register	0x1488
EP3_DMA_TTC_H	Endpoint3 DMA transfer counter high-byte register	0x148a
EP4_DMA_CON	Endpoint4 DMA control register	0x148c
-	reserved	0x148e
EP4_DMA_FIFO	Endpoint4 DMA FIFO counter register	0x1490
EP4_DMA_TTC_L	Endpoint4 DMA transfer counter low-byte register	0x1492
EP4_DMA_TTC_M	Endpoint4 DMA transfer counter middle-byte register	0x1494
EP4_DMA_TTC_H	Endpoint4 DMA transfer counter high-byte register	0x1496
COMMON INDEXED REGISTERS		
MAXP_REG	Endpoint MAX packet register	0x1420
OUT_MAXP_REG	OUT endpoint MAX packet register	0x1426
IN INDEXED REGISTERS		
IN_CSR1_REG	EP In control status register 1/EP0 control status register	0x1422
IN_CSR2_REG	EP In control status register 2	0x1424
OUT INDEXED REGISTERS		
OUT_CSR1_REG	EP Out control status register 1	0x1428
OUT_CSR2_REG	EP Out control status register 2	0x142a
OUT_FIFO_CNT1_REG	EP Out write count register 1	0x142c
OUT_FIFO_CNT2_REG	EP Out write count register 2	0x142e

TABLE 19-2. USB DEVICE SPECIAL REGISTERS

19.2.2.2 UHDP[0]/UHDN[0]/UHDP[2]/UHDN[0]/FUNCTION SELECTION

UHDP[0]/UHDN[0]/ UHDP[2]/UHDN[2] is multiplexed pin between the USB host and USB device. The function of UHDP[0]/UHDN[0]/UHDP[2]/UHDN[2] is determined by GPIOPADSEL[0]/ GPIOPADSEL[1] special register. To use the UHDP[0]/UHDN[0]/UHDP[2]/UHDN[2] as a USB device port GPIOPADSEL[0]/GPIOPADSEL[1] should be set to '1'

FUNCTION ADDRESS REGISTER(FUNC_ADDR_REG)

Address : C000 1400h

This register maintains the USB device controller address assigned by the host. The Micro Controller Unit (MCU) writes the value received through a SET_ADDRESS descriptor to this register. This address is used for the next token.

Bit	R/W	Symbol	Description	Reset Value
[7]	R/W	**ADDR_UD**	Set by the MCU whenever it updates the FUNCTION_ADDR field in this register. This bit will be cleared by the USB when the DATA_END bit is in the EP0_CSR register.	0
[6:0]	R/W	**FUN_ADDR**	The MCU writes the unique address, assigned by the host, to this field.	00

TABLE 19-3. FUNCTION ADDRESS REGISTER(FUNC_ADDR_REG)

POWER MANAGEMENT REGISTER(PWR_REG)

This is the power control register in the USB block.

Address : C000 1402h

Bit	R/W	Symbol	Description	Reset Value
[7]	R/W	**ISO_UD**	Used for ISO mode only. If set, the GFI waits for a SOF token to set IN_PKT_RDY, even though a packet to send is already loaded by the MCU. If an IN token is received before an SOF token, then a zero length data packet will be sent.	0
[6:4]	-	**Reserved**	-	-
[3]	R	**USB_RSET**	Set by the USB if reset signal is received from the host. This bit remains set as long as a reset sign a persists on the bus.	0
[2]	R/W	**MCU_RSUM**	Set by the MCU for MCU resume. The USB generates the resume signal.	
[1]	R	**SUS_MD**	Set by the USB automatically when the device enters into suspend mode. It is cleared under the following conditions: 1) The MCU clears the MCU_RESUME bit by writing '0' to end the remote resume signal. 2) The resume signal from host is received.	0
[0]	R/W	**SUS_EN**	Suspends the mode enable control bit. 0 = Disable (default). The device will not enter suspend mode. 1 = Enable suspend mode	0

TABLE 19-4. POWER MANAGEMENT REGISTER(PWR_REG)

INTERRUPT REGISTER(EP_INT_REG, USB_INT_REG)

There are two interrupt register in the USB core. When the MCU is interrupted, these registers act as status registers for it. Writing a '1' (not '0') to each bit that was set clears the bits. After interruption, the MCU should read the contents of the interrupt-related register and write back to clear the contents if it is necessary.

Address : C000 xxxx(L)h
Address : C000 xxxx(B)h

Bit	R/W	Symbol	Description	Reset Value
[4:1]	R/W	**EP1_4_INT**	For BULK/INTERRUPT IN endpoints: Set by the USB under the following conditions: 1. IN_PKT_RDY bit is cleared. 2. FIFO is flushed. 3. SENT_STALL is set. For BULK/INTERRUPT OUT endpoints: Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. SENT_STALL bit is set. For ISO IN endpoints: Set by the USB under the following conditions: 1. UNDER_RUN bit is set. 2. IN_PKT_RDY bit is cleared. 3. FIFO is flushed. **Note**: conditions 1 and 2 are mutually exclusive. For ISO OUT endpoints: Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. OVER RUN bit is set. **Note**: Conditions 1 and 2 are mutually exclusive.	0
[0]	R/W	**EP0_INT**	4	0

TABLE 19-5. INTERRUPT REGISTER(EP_INT_REG, USB_INT_REG)

Address : C000 140Ch

Bit	R/W	Symbol	Description	Reset Value
[2]	R/W	**RSET_INT**	Set by the USB when it receives the reset signal.	0
[1]	R/W	**RSUM_INT**	Set by the USB when it receives the resume signal while in suspend mode. If the resume occurs due to a USB reset, then the MCU is first interrupted with a RESUME interrupt. Once the clocks resume and the SE0 condition persists for 3ms, the USB RESET interrupt will be initiated.	0
[0]	R/W	**SUSP_INT**	Set by the USB when it receives the suspend signal. This bit is set whenever there is no activity for 3ms on the bus. Thus, if the MCU does not stop the clock after the first suspend interrupt, it will continue to be interrupted every 3ms as long as there is no activity on the USB bus. By default this interrupt is disabled.	0

TABLE 19-6. INTERRUPT REGISTER(EP_INT_REG, USB_INT_REG)

INTERRUPT ENABLE REGISTER(EP_INT_EN_REG, USB_INT_REG)

The USB device controller also has two interrupt enable registers (not resume interrupt enable) that correspond to each interrupt register. The default is USB reset interrupt enabled.

Address : C000 140Eh

Bit	R/W	Symbol	Description	Reset Value
[4]	R/W	**EP4_INT_EN**	EP4 Interrupt Enable bit 0 = Interrupt Disable 1 = Enable	1
[3]	R/W	**EP3_INT_EN**	EP3 Interrupt Enable bit 0 = Interrupt Disable 1 = Enable	1
[2]	R/W	**EP2_INT_EN**	EP2 Interrupt Enable bit 0 = Interrup t Disable 1 = Enable	1
[1]	R/W	**EP1_INT_EN**	EP1 Interrupt Enable bit 0 = Interrupt Disable 1 = Enable	1
[0]	R/W	**EP0_INT_EN**	EP0 Interrupt Enable bit 0 = Interrupt Disable 1 = Enable	1

TABLE 19-7. INTERRUPT ENABLE REGISTER(EP_INT_EN_REG, USB_INT_REG)

Address : C000 1416h

Bit	R/W	Symbol	Description	Reset Value
[2]	R/W	**RSET_INT_EN**	Reset interrupt enable bit. 0 = Interrupt Disable 1 = Enable	1
[1]	-	-	-	0
[0]	R/W	**SUSP_INT_EN**	Suspend interrupt enable bit. 0 = Interrupt Disable 1 = Enable	0

TABLE 19-8. INTERRUPT ENABLE REGISTER(EP_INT_EN_REG, USB_INT_REG)

FRAME NUMBER REGISTER(FRAME_NUM1_REG, FRAME_NUM2_REG)

A frame number is included in each Start Of Frame (SOF) if the host transfers a USB packet. The USB device controller catches this frame number and loads it into this register.

Address : C000 1418h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	**FRM_NUM1**	Frame number lower byte value	00

TABLE 19-9. FRAME NUMBER REGISTER(FRAME_NUM1_REG, FRAME_NUM2_REG)

Address : C000 141Ah

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	**FRM_NUM2**	Frame number higher byte value	00

TABLE 19-10. FRAME NUMBER REGISTER(FRAME_NUM1_REG, FRAME_NUM2_REG)

INDEX REGISTER (INDEX_REG)

To indicate certain endpoint registers effectively, use this INDEX register. For an endpoint inside the core using the INDEX register, the endpoint registers (MAXP_REG, IN_CSR1_REG, IN_CSR2_REG, OUT_CSR1_REG, OUT_CSR2_REG, OUT_FIFO_CNT1_REG and OUT_FIFO_CNT2_REG) can be accessed by the MCU.

Address : C000 141Ch

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**INDEX_REG**	Indicates a certain endpoint.	00

TABLE 19-11. INDEX REGISTER(INDEX_REG)

END POINT0 CONTROL STATUS REGISTER(EP0_CSR)

For Endpoint0, this register has the control and status bits. As a control transaction is involved with both IN and OUT tokens, only one CSR register is mapped to the IN CSR1 register. (Shares IN1_CSR and can be accessed by writing the index register"0" and read/write IN1_CSR)

Address : C000 1422h

Bit	R/W	Symbol	Description	Reset Value
[7]	W	**SETUP_END**	The MCU should write a "1" to this bit to clear SETUP_END.	0
[6]	W	**OUT_PKT_RDY**	The MCU should write a "1" to this bit to clear OUT_PKT_RDY.	0
[5]	R/W	**SEND_STALL**	The MCU should write a "1" to this bit at the same time it clears OUT_PKT_RDY, if it decodes an invalid token. 0 = Finish the STALL condition. 1 = The USB issues a STALL and shake to the current control transfer.	0
[4]	R	**SETUP_END**	Set by the USB when a control transfer ends before DATA_END is set. When the USB sets this bit, an interrupt is generated to the MCU. When such a condition occurs, the USB flushes the FIFO and invalidates MCU access to the FIFO.	0
[3]	SET	**DATA_END**	Set by the MCU on the following conditions: 1. After loading the last packet of data into the FIFO, but at the same time IN_PKT_RDY is set. 2. While it clears OUT_PKT_RDY after unloading the last packet of data. 3. For a zero length data phase.	0
[2]	CLEAR	**SENT_STALL**	Set by the USB if a control transaction is stopped due to a protocol violation. An interrupt is generated when this bit is set. The MCU should write "0" to clear this bit.	0
[1]	SET	**IN_PKT_RDY**	Set by the MCU after writing a packet of data into EP0 FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so the MCU can load the next packet. For a zero length data phase, the MCU sets DATA_END at the same time.	0
[0]	R	**OUT_PKT_RDY**	Set by the USB once a valid token is written to the FIFO. An interrupt is generated when the USB sets this bit. The MCU clears this bit by writing a "1" to the SERVICED_OUT_PKT_RDY bit.	0

TABLE 19-12. END POINT0 CONTROL STATUS REGISTER(EP0_CSR)

END POINT in CONTROL STATUS REGISTER(IN_CSR1_REG, IN_CSR2_REG)

Address : C000 1422h

Bit	R/W	Symbol	Description	Reset Value
[7]	-	**Reserved**	-	0
[6]	R/W	**CLR_DT_TOG**	Used in set-up procedure. 0 = There are alternation of DATA0 and DATA1. 1 = The data toggle bit is cleared and PID in packet will maintain DATA0.	0
[5]	R/ CLE AR	**SNT_STALL**	Set by the USB when an IN token issues a STALL handshake, and after the MCU sets SEND_STALL bit to start STALL handshaking. When the USB issues a STALL handshake, IN_PKT_RDY is cleared.	0
[4]	W/R	**SND_STALL**	0 = The MCU clears this bit to finish the STALL condition. 1 = The MCU issues a STALL handshake to the USB.	0
[3]	R/W	**FF_FLUSH**	Set by the MCU if it intends to flush the packet in Input-related FIFO. This bit is cleared by the USB when the FIFO is flushed. The MCU is interrupted when this happens. If a token is in process, the USB waits until the transmission is complete before FIFO flushing. If two packets are loaded into the FIFO, only the first packet (the packet that is intended to be sent to the host) is flushed, and the corresponding IN_PKT_RDY bit is cleared.	0
[2]	R/ CLE AR	**UND_RUN**	Valid only For ISO Mode Set by the USB when in ISO mode, an IN token is received, and the IN_PKT_RDY bit is not set. The USB sends a zero length data packet for such conditions, and the next packet that is loaded into the FIFO is flushed. This bit is cleared by writing 0.	0
[1]	-	**Reserved**	-	-
[0]	R/ SET	**IN_PKT_RDY**	Set by the MCU after writing a packet of data into the FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so the MCU can load the next packet. While this bit is set, the MCU will not be able to write to the FIFO. If the MCU sets the SND_STALL bit, this bit cannot be set.	0

TABLE 19-13. END POINT IN CONTROL STATUS REGISTER(IN_CSR1_REG)

Address : C000 1424h

Bit	R/W	USB	Symbol	Description	Reset Value
[7]	R/W	R	**AUTO_SET**	If set, whenever the MCU writes MAXP data, IN_PKT_RDY will automatically be set by the core without any intervention from the MCU. If the MCU writes less than MAXP data, then the IN_PKT_RDY bit has to be set by the MCU.	0
[6]	R/W	R	**ISO**	Used only for endpoints whose transfer type is programmable. 0 = Configures endpoint to Bulk mode 1 = Configures endpoint to ISO mode	0
[5]	R/W	R	**MODE_IN**	Used only for endpoints whose direction is programmable. 0 = Configures Endpoint Direction as OUT 1 = Configures Endpoint Direction as IN	1
[4]	R/W	R	**IN_DMA_ INT_EN**	Determines whether the interrupt should be issued or not when the EP1 IN_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt Enable 1 = Interrupt Disable	0
[3:0]	-	-	**Reserved**	Reserved	-

TABLE 19-14. END POINT IN CONTROL STATUS REGISTER(IN_CSR2_REG)

End Point out control status register(OUT_CSR1_REG)

Address : C000 1428h

Bit	MCU	USB	OUT_CSR1_ REG	Description	Reset Value
[7]	R/W	CLEAR	**CLR_DATA_ TOGGLE**	When the MCU writes a 1 to this bit, the data toggle sequence bit is reset to DATA0.	0
[6]	CLEAR/R	SET	**SENT_STALL**	Set by the USB when an OUT token is ended with a STALL handshake. The USB issues a STALL handshake to the host if it sends more than MAXP data for the OUT TOKEN.	0
[5]	R/W	R	**SEND_STALL**	0 = The MCU clears this bit to end the STALL condition handshake, and IN_PKY_RDY is cleared. 1 = The MCU issues a STALL handshake to the USB. The MCU clears this bit to end the STALL condition handshake, and IN_PKY_RDY is cleared.	0
[4]	R/W	CLEAR	**FIFO_FLUSH**	The MCU writes a 1 to flush the FIFO. This bit can be set only when OUT_PKT_RDY (D0) is set. The packet due to be unloaded by the MCU will be flushed.	0
[3]	R	R/W	**DATA_ERROR**	Valid only in ISO mode. This bit should be sampled with OUT_PKT_RDY . When set, it indicates the data packet due to be unloaded by the MCU has an error (either bit stuffing or CRC). If two packets are loaded into the FIFO, and the second packet has an error, then this bit gets set only after the first packet is unloaded. This bit is automatically cleared when OUT_PKT_RDY gets cleared.	0
[2]	R/Clear	R/W	**OVER_RUN**	Valid only in ISO mode. This bit is set if the core is not able to load an OUT ISO token into the FIFO. The MCU clears this bit by writing 0.	0
[1]	-	-	**Reserved**	-	-
[0]	R/ CLEAR	SET	**OUT_PKT_ RDY**	Set by the USB after it has loaded a packet of data into the FIFO. Once the MCU reads the packet from FIFO, this bit should be cleared by the MCU. (Write a "0")	0

TABLE 19-15. END POINT OUT CONTROL STATUS REGISTER(OUT_CSR1_REG)

End Point out control status register(OUT_CSR2_REG)

Address : C000 142Ah

Bit	MCU	USB	OUT_CSR2_ REG	Description	Reset Value
[7]	R/W	R	**AUTO_CLR**	If set, whenever the MCU reads data from the OUT FIFO, OUT_PKT_RDY will be cleared automatically by the logic, without any intervention from the MCU.	0
[6]	R/W	R	**ISO**	Determines the endpoint transfer type. 0 : Configures the endpoint to Bulk mode. 1 : Configures the endpoint to ISO mode.	0
[5]	R/W	R	**OUT_DMA_ INT_MASK**	Determines whether the interrupt should be issued or not. The OUT_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt Enable 1 = Interrupt Disable	0
[4:0]	-	-	**Reserved**	Reserved	-

TABLE 19-16. END POINT OUT CONTROL STATUS REGISTER(OUT_CSR2_REG)

END POINT FIFO REGISTER(EP0_FIFO_REG)

EP0_FIFO_REG should be accessed by MCU to access EP0 FIFO.

Address : C000 1440h

Bit	MCU	USB	EP0_FIFO	Description	Reset Value
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

TABLE 19-17. END POINT FIFO REGISTER(EP0_FIFO_REG)

END POINT FIFO REGISTER(EP1_FIFO_REG)

EP1_FIFO_REG should be accessed by the MCU to access EP1 FIFO.

Address : C000 1442h

Bit	MCU	USB	EP1_FIFO	Description	Reset Value
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

TABLE 19-18. END POINT FIFO REGISTER(EP1_FIFO_REG)

END POINT FIFO REGISTER(EP2_FIFO_REG)

EP2_FIFO_REG should be accessed by the MCU to access EP2 FIFO.

Address : C000 1444h

Bit	MCU	USB	EP2_FIFO	Description	Reset Value
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

TABLE 19-19. END POINT FIFO REGISTER(EP2_FIFO_REG)

END POINT FIFO REGISTER(EP3_FIFO_REG)

EP3_FIFO_REG should be accessed by the MCU to access EP3 FIFO.

Address : C000 1446h

Bit	MCU	USB	EP3_FIFO	Description	Reset Value
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

TABLE 19-20. END POINT FIFO REGISTER(EP3_FIFO_REG)

END POINT FIFO REGISTER(EP4_FIFO_REG)

EP4_FIFO_REG should be accessed by the MCU to access EP4 FIFO.

Address : C000 1448h

Bit	MCU	USB	EP4_FIFO	Description	Reset Value
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

TABLE 19-21. END POINT FIFO REGISTER(EP4_FIFO_REG)

IN MAX Packet Register(IN_MAXP_REG)

Address : C000 1420h

Bit	MCU	USB	MAXP_REG	Description	Reset Value
[3:0]	R/W	R	**MAXP**	0000 : Reserved 0001 : MAXP = 8 Byte 0010 : MAXP = 16 Byte 0100 : MAXP = 32 Byte 1000 : MAXP = 64 Byte For EP0, MAXP=8 is recommended. For EP1~4, MAXP=32 or MAXP=64 is recommended. And, if MAXP=32, the dual packet mode will be enabled automatically.	0001

TABLE 19-22. IN MAX PACKET REGISTER(IN_MAXP_REG)

OUT MAX Packet Register(OUT_MAXP_REG)

Address : C000 1426h

Bit	MCU	USB	MAXP_REG	Description	Reset Value
[3:0]	R/W	R	**MAXP**	0000 : Reserved 0001 : MAXP = 8 Byte 0010 : MAXP = 16 Byte 0100 : MAXP = 32 Byte 1000 : MAXP = 64 Byte For EP0, MAXP=8 is recommended. For EP1~4, MAXP=32 or MAXP=64 is recommended. And, if MAXP=32, the dual packet mode will be enabled automatically.	0001

TABLE 19-23. OUT MAX PACKET REGISTER(OUT_MAXP_REG)

END POINT Out Write Count REGISTER(OUT_FIFO_CNT1_REG)

The number of bytes in the packet due to be unloaded by the MCU is maintained by these registers.

Address : C000 142Ch

Bit	MCU	USB	OUT_FIFO_CNT1_REG	Description	Reset Value
[7:0]	R	W	**OUT_CNT_LOW**	Lower byte of write count.	0x00

TABLE 19-24. END POINT OUT WRITE COUNT REGISTER(OUT_FIFO_CNT1_REG)

END POINT Out Write Count REGISTER(OUT_FIFO_CNT2_REG)

Address : C000 142Eh

Bit	MCU	USB	OUT_FIFO_CNT2_REG	Description	Reset Value
[7:0]	R	W	**OUT_CNT_HIGH**	Higher byte of write count. The OUT_CNT_HIGH may be always 0 normally.	00

TABLE 19-25. END POINT OUT WRITE COUNT REGISTER(OUT_FIFO_CNT2_REG)

DMA INTERFACE CONTROL REGISTER(EP1_DMA_CON)

Address : C000 146Ch

Bit	MCU	USB	EP1_DMA_CON	Description	Reset Value
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation 0 = DMA is stopped 1= DMA is running Write) Ignorethe Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring.	0
[3]	-	-	**Reserved**		-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0

TABLE 19-26. DMA INTERFACE CONTROL REGISTER(EP1_DMA_CON)

DMA INTERFACE CONTROL REGISTER(EP2_DMA_CON)

Address : C000 1480h

Bit	MCU	USB	EP2_DMA_CON	Description	Reset Value
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation. 0 = DMA is stopped 1= DMA is running Write) Ignore the Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1=: DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring.	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run Read operation: OUT DMA Run Observation	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0

TABLE 19-27. DMA INTERFACE CONTROL REGISTER(EP2_DMA_CON)

DMA INTERFACE CONTROL REGISTER(EP3_DMA_CON)

Address : C000 148Ch

Bit	MCU	USB	EP3_DMA_CON	Description	Reset Value
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation. 0 = DMA is stopped 1= DMA is running Write) Ignore Epn_DMA_TTC_n register 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0

TABLE 19-28. DMA INTERFACE CONTROL REGISTER(EP3_DMA_CON)

DMA INTERFACE CONTROL REGISTER(EP4_DMA_CON)

Address : C000 1460h

Bit	MCU	USB	EP4_DMA_CON	Description	Reset Value
[7]	R/W	W	**IN_RUN_OB**	Read Mode: DMA Run Observation. 0 = DMA is stopped 1= DMA is running Write Mode: Ignore the Epn_DMA_TTC_n register 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring.	0
[3]	-	-	**-**	reserved	0
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0, and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0

TABLE 19-29. DMA INTERFACE CONTROL REGISTER(EP4_DMA_CON)

DMA FIFO COUNTER REGISTER(EP1_DMA_FIFO)

The byte size in FIFO to be transferred by DMA is in this register. When OUT_DMA is enabled, the value in the OUT FIFO Write Count Register 1 will be loaded into this register. For IN DMA Mode, the MCU should set the proper value by R/W.

Address : C000 1464h

Bit	MCU	USB	DMA_UNIT	Description	Reset Value
[7:0]	R/W	R	**EP1_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00

TABLE 19-30. DMA FIFO COUNTER REGISTER(EP1_DMA_FIFO)

DMA FIFO COUNTER REGISTER(EP2_DMA_FIFO)

Address : C000 1470h

Bit	MCU	USB	DMA_UNIT	Description	Reset Value
[7:0]	R/W	R	**EP2_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00

TABLE 19-31. DMA FIFO COUNTER REGISTER(EP2_DMA_FIFO)

DMA FIFO COUNTER REGISTER(EP3_DMA_FIFO)

Address : C000 1484h

Bit	MCU	USB	DMA_UNIT	Description	Reset Value
[7:0]	R/W	R	**EP3_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00

TABLE 19-32. DMA FIFO COUNTER REGISTER(EP3_DMA_FIFO)

DMA FIFO COUNTER REGISTER(EP4_DMA_FIFO)

Address : C000 1490h

Bit	MCU	USB	DMA_UNIT	Description	Reset Value
[7:0]	R/W	R	**EP4_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00

TABLE 19-33. DMA FIFO COUNTER REGISTER(EP4_DMA_FIFO)

DMA TOTAL Transfer Counter REGISTER(EP1_DMA_TTC_L, EP1_DMA_TTC_M, EP1_DMA_TTC_H)

The total number of bytes to be transferred using DMA is in this register. (Total 20 bit Counter)

Address : C000 1466h
Address : C000 1468h
Address : C000 146Ah

Bit	MCU	USB	DMA_TX	Description	Reset Value
[7:0]	R/W	R	**EP1_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP1_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP1_TTC_H**	DMA total transfer count value (higher byte)	0x00

TABLE 19-34. DMA TOTAL TRANSFER COUNTER REGISTER(EP1_DMA_TTC_L, EP1_DMA_TTC_M, EP1_DMA_TTC_H)

DMA TOTAL Transfer Counter REGISTER(EP2_DMA_TTC_L, EP2_DMA_TTC_M, EP2_DMA_TTC_H)

The total number of bytes to be transferred using DMA is in this register. (Total 20 bit Counter).

Address : C000 1472h
Address : C000 1474h
Address : C000 1476h

Bit	MCU	USB	DMA_TX	Description	Reset Value
[7:0]	R/W	R	**EP2_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP2_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP2_TTC_H**	DMA total transfer count value (higher byte)	0x00

TABLE 19-35. DMA TOTAL TRANSFER COUNTER REGISTER(EP2_DMA_TTC_L, EP2_DMA_TTC_M, EP2_DMA_TTC_H)

DMA TOTAL Transfer counter REGISTER(EP3_DMA_TTC_L, EP3_DMA_TTC_M, EP3_DMA_TTC_H)

The total number of bytes to be transferred using DMA is in this register. (Total 20 bit Counter).

Address : C000 1486h
Address : C000 1488h
Address : C000 148Ah

Bit	MCU	USB	DMA_TX	Description	Reset Value
[7:0]	R/W	R	**EP3_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP3_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP3_TTC_H**	DMA total transfer count value (higher byte)	0x00

TABLE 19-36. DMA TOTAL TRANSFER COUNTER REGISTER(EP3_DMA_TTC_L, EP3_DMA_TTC_M, EP3_DMA_TTC_H)

DMA TOTAL Transfer counter REGISTER(EP4_DMA_TTC_L, EP4_DMA_TTC_M, EP4_DMA_TTC_H)

The total number of bytes to be transferred using DMA is in this register. (Total 20 bit Counter).

Address : C000 1492h
Address : C000 1494h
Address : C000 1496h

Bit	MCU	USB	DMA_TX	Description	Reset Value
[7:0]	R/W	R	**EP4_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP4_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP4_TTC_H**	DMA total transfer count value (higher byte)	0x00

TABLE 19-37. DMA TOTAL TRANSFER COUNTER REGISTER(EP4_DMA_TTC_L, EP4_DMA_TTC_M, EP4_DMA_TTC_H)

19.2.3 USB DEVICE REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
FUNCTION ADDRESS REGISTER (FUNC_ADDR_REG) ***Address : C000 1400h***				
[7]	R/W	**ADDR_UD**	Set by the MCU whenever it updates the FUNCTION_ADDR field in this register. This bit will be cleared by the USB when the DATA_END bit is in the EP0_CSR register.	0
[6:0]	R/W	**FUN_ADDR**	The MCU writes the unique address, assigned by the host, to this field.	00
POWER MANAGEMENT REGISTER (PWR_REG) ***Address : C000 1402h***				
[7]	R/W	**ISO_UD**	Used for ISO mode only. If set, the GFI waits for an SOF token to set IN_PKT_RDY, even though a packet to send is already loaded by the MCU. If an IN token is received before an SOF token, then a zero length data packet will be sent.	0
[6:4]	-	**Reserved**	-	-
[3]	R	**USB_RSET**	Set by the USB if a reset signal is received from the host. This bit remains set as long as the reset signal persists on the bus.	0
[2]	R/W	**MCU_RSUM**	Set by the MCU for MCU resume. The USB generates the resume signal.	
[1]	R	**SUS_MD**	Set by the USB automatically when the device enters into suspend mode. It is cleared under the following conditions: 1) The MCU clears the MCU_RESUME bit by writing '0' to end remote resume signaling. 2) The resume signal from the host is received.	0
[0]	R/W	**SUS_EN**	Suspend mode enable control bit. 0 = Disable (default). The device will not enter suspend mode. 1 = Enable suspend mode.	0
INTERRUPT REGISTER (EP_INT_REG, USB_INT_REG) ***Address : C000 xxxx(L)h ~ C000 xxxx(B)h***				

Bit	R/W	Symbol	Description	Reset Value
[4:1]	R/W	**EP1_4_INT**	For BULK/INTERRUPT IN endpoints: Set by the USB under the following conditions: 1. IN_PKT_RDY bit is cleared. 2. FIFO is flushed. 3. SENT_STALL is set. For BULK/INTERRUPT OUT endpoints: Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. SENT_STALL bit is set. For ISO IN endpoints: Set by the USB under the following conditions: 1. UNDER_RUN bit is set. 2. IN_PKT_RDY bit is cleared. 3. FIFO is flushed. **Note**: conditions 1 and 2 are mutually exclusive. For ISO OUT endpoints: Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. OVER RUN bit is set. **Note**: Conditions 1 and 2 are mutually exclusive.	0
[0]	R/W	**EP0_INT**	Corresponds to endpoint 0 interrupt. Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. IN_PKT_RDY bit is cleared. 3. SENT_STALL bit is set. 4. SETUP_END bit is set. 5. DATA_END bit is cleared (Indicates end of control transfer).	0
Address : C000 140Ch				
[2]	R/W	**RSET_INT**	Set by the USB when it receives a reset signal.	0
[1]	R/W	**RSUM_INT**	Set by the USB when it receives a resume signal, while in suspend mode. If the resume occurs due to a USB reset, then the MCU is first interrupted with a RESUME interrupt. Once the clocks resume and the SE0 condition persists for 3ms, a USB RESET interrupt will be initiated.	0
[0]	R/W	**SUSP_INT**	Set by the USB when it receives a suspend signal. This bit is set whenever there is no activity for 3ms on the bus. Thus, if the MCU does not stop the clock after the first suspend interrupt, it will be continue to be interrupted every 3ms as long as there is no activity on the USB bus. By default, this interrupt is disabled.	0
INTERRUPT ENABLE REGISTER (EP_INT_EN_REG, USB_INT_REG) ***Address : C000 140Eh***				

Bit	R/W	Symbol	Description	Reset Value
[4]	R/W	**EP4_INT_EN**	EP4 Interrupt Enable bit. 0 = Interrupt Disable 1 = Enable	1
[3]	R/W	**EP3_INT_EN**	EP3 Interrupt Enable bit. 0 = Interrupt Disable 1 = Enable	1
[2]	R/W	**EP2_INT_EN**	EP2 Interrupt Enable bit. 0 = Interrupt Disable 1 = Enable	1
[1]	R/W	**EP1_INT_EN**	EP1 Interrupt Enable bit. 0 = Interrupt Disable 1 = Enable	1
[0]	R/W	**EP0_INT_EN**	EP0 Interrupt Enable bit. 0 = Interrupt Disable 1 = Enable	1
Address : C000 1416h				
[2]	R/W	**RSET_INT_EN**	Reset interrupt enable bit. 0 = InterruptDdisable 1 = Enable	1
[1]	-	**-**	-	0
[0]	R/W	**SUSP_INT_EN**	Suspend interrupt enable bit 0 = Interrupt Disable 1 = Enable	0
FRAME NUMBER REGISTER (FRAME_NUM1_REG, FRAME_NUM2_REG) ***Address : C000 1418h***				
[7:0]	R	**FRM_NUM1**	Frame number lower byte value.	00
Address : C000 141Ah				
[7:0]	R	**FRM_NUM2**	Frame number higher byte value.	00
INDEX REGISTER (INDEX_REG) ***Address : C000 141Ch***				
[7:0]	R/W	**INDEX_REG**	Indicates a certain endpoint.	00
END POINT0 CONTROL STATUS REGISTER (EP0_CSR) ***Address : C000 1422h***				
[7]	W	**SETUP_END**	The MCU should write a "1" to this bit to clear SETUP_END.	0
[6]	W	**OUT_PKT_RDY**	The MCU should write a "1" to this bit to clear OUT_PKT_RDY.	0
[5]	R/W	**SEND_STALL**	The MCU should write a "1" to this bit at the same time it clears OUT_PKT_RDY, if it decodes an invalid token. 0 = Finish the STALL condition. 1 = The USB issues a STALL and shake to the current control transfer.	0

Bit	R/W	Symbol	Description	Reset Value
[4]	R	**SETUP_END**	Set by the USB when a control transfer ends before DATA_END is set. When the USB sets this bit, an interrupt is generated to the MCU. When such a condition occurs, the USB flushes the FIFO and invalidates the MCU access to the FIFO.	0
[3]	SET	**DATA_END**	Set by the MCU on the following conditions: 1. After loading the last packet of data into the FIFO, and at the same time IN_PKT_RDY is set. 2. While it clears OUT_PKT_RDY after unloading the last packet of data. 3. For a zero length data phase.	0
[2]	CLEAR	**SENT_STALL**	Set by the USB if a control transaction is stopped due to a protocol violation. An interrupt is generated when this bit is set. The MCU should write "0" to clear this bit.	0
[1]	SET	**IN_PKT_RDY**	Set by the MCU after writing a packet of data into EP0 FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so the MCU can load the next packet. For a zero length data phase, the MCU sets DATA_END at the same time.	0
[0]	R	**OUT_PKT_RDY**	Set by the USB once a valid token is written to the FIFO. An interrupt is generated when the USB sets this bit. The MCU clears this bit by writing a "1" to the SERVICED_OUT_PKT_RDY bit.	0
END POINT in CONTROL STATUS REGISTER (IN_CSR1_REG, IN_CSR2_REG) ***Address : C000 1422h***				
[7]	-	**Reserved**	-	-
[6]	R/W	**CLR_DT_TOG**	Used in set-up procedure. 0 = There are alternations of DATA0 and DATA1. 1 = The data toggle bit is cleared and the PID in the packet will maintain DATA0.	0
[5]	R/CLEAR	**SNT_STALL**	Set by the USB when an IN token issues a STALL handshake, and after the MCU sets the SEND_STALL bit to start STALL handshaking. When the USB issues a STALL handshake, IN_PKT_RDY is cleared.	0
[4]	W/R	**SND_STALL**	0 = The MCU clears this bit to finish the STALL condition. 1 = The MCU issues a STALL handshake to the USB.	0
[3]	R/W	**FF_FLUSH**	Set by the MCU if it intends to flush the packet in Input-related FIFO. This bit is cleared by the USB when the FIFO is flushed. The MCU is interrupted when this happens. If a token is in process, the USB waits until the transmission is complete before FIFO flushing. If two packets are loaded into the FIFO, only the first packet (The packet that is intended to be sent to the host) is flushed, and the corresponding IN_PKT_RDY bit is cleared.	0
[2]	R/CLEAR	**UND_RUN**	Valid only For ISO Mode Set by the USB when in ISO mode, an IN token is received, and the IN_PKT_RDY bit is not set. The USB sends a zero length data packet for such conditions, and the next	0

Bit	R/W	Symbol	Description	Reset Value
			packet that is loaded into the FIFO is flushed. This bit is cleared by writing 0.	
[1]	-	**Reserved**	-	-
[0]	R/ SET	**IN_PKT_RDY**	Set by the MCU after writing a packet of data into the FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so the MCU can load the next packet. While this bit is set, the MCU will not be able to write to the FIFO. If the MCU sets the SND_STALL bit, this bit cannot be set.	0

TABLE 19-38. USB DEVICE REGISTERS LIST

Bit	MCU	USB	Symbol	Description	Reset Value
Address : C000 1424h					
[7]	R/W	R	**AUTO_SET**	If set, whenever the MCU writes MAXP data, IN_PKT_RDY will automatically be set by the core without any intervention from the MCU. If the MCU writes less than MAXP data, then the IN_PKT_RDY bit has to be set by the MCU.	0
[6]	R/W	R	**ISO**	Used only for endpoints whose transfer type is programmable. 0 = Configures endpoint to Bulk mode 1 = Configures endpoint to ISO mode	0
[5]	R/W	R	**MODE_IN**	Used only for endpoints whose direction is programmable. 0 = Configures Endpoint Direction as OUT 1 = Configures Endpoint Direction as IN	1
[4]	R/W	R	**IN_DMA_INT_EN**	Determines whether the interrupt should be issued or not when the EP1 IN_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt Enable 1 = Interrupt Disable	0
[3:0]	-	-	**Reserved**	-	-
End Point out control status register (OUT_CSR1_REG) ***Address : C000 1428h***					
[7]	R/W	CLEAR	**CLR_DATA_ TOGGLE**	When the MCU writes a 1 to this bit, the data toggle sequence bit is reset to DATA0.	0
[6]	CLEAR /R	SET	**SENT_STALL**	Set by the USB when an OUT token is ended with a STALL handshake. The USB issues a STALL handshake to the host if it sends more than MAXP data for the OUT TOKEN.	0
[5]	R/W	R	**SEND_STALL**	0 = The MCU clears this bit to end the STALL condition handshake, and IN_PKY_RDY is cleared. 1 = The MCU issues a STALL handshake to the USB. The MCU clears this bit to end the STALL condition handshake, and IN_PKY_RDY is cleared.	0
[4]	R/W	CLEAR	**FIFO_FLUSH**	The MCU writes a 1 to flush the FIFO. This bit can be set only when OUT_PKT_RDY (D0) is set. The packet due to be unloaded by the MCU will be flushed.	0

Bit	MCU	USB	Symbol	Description	Reset Value
[3]	R	R/W	**DATA_ERROR**	Valid only in ISO mode. This bit should be sampled with OUT_PKT_RDY . When set, it indicates the data packet due to be unloaded by the MCU has an error (either bit stuffing or CRC). If two packets are loaded into the FIFO, and the second packet has an error, then this bit gets set only after the first packet is unloaded. This bit is automatically cleared when OUT_PKT_RDY gets cleared.	0
[2]	R/Clear	R/W	**OVER_RUN**	Valid only in ISO mode. This bit is set if the core is not able to load an OUT ISO token into the FIFO. The MCU clears this bit by writing 0.	0
[1]	-	-	**Reserved**	-	-
[0]	R/ CLEAR	SET	**OUT_PKT_RDY**	Set by the USB after it has loaded a packet of data into the FIFO. Once the MCU reads the packet from FIFO, this bit should be cleared by the MCU. (Write a "0")	0
End Point out control status register (OUT_CSR2_REG) ***Address : C000 142Ah***					
[7]	R/W	R	**AUTO_CLR**	If set, whenever the MCU reads data from the OUT FIFO, OUT_PKT_RDY will be cleared automatically by the logic, without any intervention from the MCU.	0
[6]	R/W	R	**ISO**	Determines endpoint transfer type. 0 = Configures endpoint to Bulk mode. 1 = Configures endpoint to ISO mode.	0
[5]	R/W	R	**OUT_DMA_INT_ MASK**	Determines whether the interrupt should be issued or not. The OUT_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt Enable 1 = Interrupt Disable	0
[4:0]	-	-	**Reserved**	-	-
END POINT FIFO REGISTER (EP0_FIFO_REG) ***Address : C000 1440h***					
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX
END POINT FIFO REGISTER (EP1_FIFO_REG) ***Address : C000 1442h***					
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX
END POINT FIFO REGISTER (EP2_FIFO_REG) ***Address : C000 1444h***					
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX

Bit	MCU	USB	Symbol	Description	Reset Value
END POINT FIFO REGISTER (EP3_FIFO_REG) ***Address : C000 1446h***					
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX
END POINT FIFO REGISTER (EP4_FIFO_REG) ***Address : C000 1448h***					
[7:0]	R/W	R/W	**FIFO_DATA**	FIFO data value	0xXX
IN MAX packet register (IN_MAXP_REG) ***Address : C000 1420h***					
[3:0]	R/W	R	**MAXP**	0000 : Reserved 0001 : MAXP = 8 Byte 0010 : MAXP = 16 Byte 0100 : MAXP = 32 Byte 1000 : MAXP = 64 Byte For EP0, MAXP=8 is recommended. For EP1~4, MAXP=32 or MAXP=64 is recommended. And, if MAXP=32, the dual packet mode will be enabled automatically.	0001
OUT MAX packet register (OUT_MAXP_REG) ***Address : C000 1426h***					
[3:0]	R/W	R	**MAXP**	0000 : Reserved 0001 : MAXP = 8 Byte 0010 : MAXP = 16 Byte 0100 : MAXP = 32 Byte 1000 : MAXP = 64 Byte For EP0, MAXP=8 is recommended. For EP1~4, MAXP=32 or MAXP=64 is recommended. And, if MAXP=32, the dual packet mode will be enabled automatically.	0001
END POINT o ut write count REGISTER (OUT_FIFO_CNT1_REG) ***Address : C000 142Ch***					
[7:0]	R	W	**OUT_CNT_LOW**	Lower byte of write count.	0x00
END POINT out write count REGISTER (OUT_FIFO_CNT2_REG) ***Address : C000 142Eh***					
[7:0]	R	W	**OUT_CNT_HIGH**	Higher byte of write count. The OUT_CNT_HIGH may be always 0 normally.	00
DMA INTERFACE CONTROL REGISTER (EP1_DMA_CON) ***Address : C000 146Ch***					
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation. 0 = DMA is stopped 1 = DMA is running	0

Bit	MCU	USB	Symbol	Description	Reset Value
				Write) Ignore Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	
[6:4]	R	W	**STATE**	DMA State Monitoring	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB / OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0
DMA INTERFACE CONTROL REGISTER (EP2_DMA_CON) ***Address : C000 1480h***					
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation. 0 = DMA is stopped 1 = DMA is running Write) Ignore Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring.	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0
DMA INTERFACE CONTROL REGISTER (EP3_DMA_CON) ***Address : C000 148Ch***					

Bit	MCU	USB	Symbol	Description	Reset Value
[7]	R/W	W	**IN_RUN_OB**	Read) DMA Run Observation. 0 = DMA is stopped 1 = DMA is running Write) Ignore Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring.	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation. 0 = Stop 1 = Run	0
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0
DMA INTERFACE CONTROL REGISTER (EP4_DMA_CON) ***Address : C000 1460h***					
[7]	R/W	W	**IN_RUN_OB**	Read Mode: DMA Run Observation. 0 = DMA is stopped 1 = DMA is running Write Mode: Ignore Epn_DMA_TTC_n register. 0 = DMA requests will be stopped if Epn_DMA_TTC_n reaches 0. 1 = DMA requests will be continued although Epn_DMA_TTC_n reaches 0.	0
[6:4]	R	W	**STATE**	DMA State Monitoring	0
[3]	-	-	**Reserved**	-	-
[2]	R/W	R/W	**OUT_RUN_OB /OUT_DMA_RUN**	Functionally separated into write and read operations. Write operation: 0 = Stop 1 = Run. Read operation: OUT DMA Run Observation.	0
[1]	R/W	R	**IN_DMA_RUN**	Start DMA operation 0 = Stop 1 = Run	0

Bit	MCU	USB	Symbol	Description	Reset Value
[0]	R/W	R/Clear	**DMA_MODE_EN**	Set DMA mode. If the RUN_OB has been written as 0 and Epn_DMA_TTC_n reaches 0, the DMA_MODE_EN bit will be cleared by the USB. 0 = Interrupt Mode 1 = DMA Mode	0
DMA FIFO COUNTER REGISTER (EP1_DMA_FIFO) ***Address : C000 1464h***					
[7:0]	R/W	R	**EP1_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00
DMA FIFO COUNTER REGISTER (EP2_DMA_FIFO) ***Address : C000 1470h***					
[7:0]	R/W	R	**EP2_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00
DMA FIFO COUNTER REGISTER (EP3_DMA_FIFO) ***Address : C000 1484h***					
[7:0]	R/W	R	**EP3_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00
DMA FIFO COUNTER REGISTER (EP4_DMA_FIFO) ***Address : C000 1490h***					
[7:0]	R/W	R	**EP4_FIFO_CNT**	EP DMA transfer FIFO counter value	0x00
DMA TOTAL Transfer Counter REGISTER (EP1_DMA_TTC_L, EP1_DMA_TTC_M, EP1_DMA_TTC_H) ***Address : C000 1466h / C000 1468h /C000 146Ah***					
[7:0]	R/W	R	**EP1_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP1_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP1_TTC_H**	DMA total transfer count value (higher byte)	0x00
DMA TOTAL Transfer Counter REGISTER (EP2_DMA_TTC_L, EP2_DMA_TTC_M, EP2_DMA_TTC_H) ***Address : C000 1472h / C000 1474h / C000 1476h***					
[7:0]	R/W	R	EP2_TTC_L	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP2_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP2_TTC_H**	DMA total transfer count value (higher byte)	0x00
DMA TOTAL Transfer Counter REGISTER (EP3_DMA_TTC_L, EP3_DMA_TTC_M, EP3_DMA_TTC_H) ***Address : C000 1486h / C000 1488h / C000 148Ah***					
[7:0]	R/W	R	**EP3_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP3_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP3_TTC_H**	DMA total transfer count value (higher byte)	0x00
DMA TOTAL Transfer Counter REGISTER (EP4_DMA_TTC_L, EP4_DMA_TTC_M, EP4_DMA_TTC_H) ***Address : C000 1492h / C000 1494h / C000 1496h***					

Bit	MCU	USB	Symbol	Description	Reset Value
[7:0]	R/W	R	**EP4_TTC_L**	DMA total transfer count value (lower byte)	0x00
[7:0]	R/W	R	**EP4_TTC_M**	DMA total transfer count value (middle byte)	0x00
[7:0]	R/W	R	**EP4_TTC_H**	DMA total transfer count value (higher byte)	0x00

CHAPTER 20

I^2C

20. I²C

20.1 OVERVIEW

The MP2520F Microprocessor can support a multi-master I²C -bus serial interface. Information between bus masters and peripheral devices that are connected to the 12C-bus is carried by a dedicated serial data line (SDA) and a serial clock line (SCL). The SDA and SCL lines are bi-directional.

In multi-master I²C -bus mode Serial data to or from slave devices can be received or transmitted by multiple MP2520F Microprocessors. The master MP2520F, by which a data transfer can be initiated over the 12C-bus, is responsible for terminating the transfer. This I²C -bus in MP2520F uses the standard bus arbitration procedure.

Values must be written to the following registers to control multi-master 12C-bus operations:

- I²C CON, Multi-master I²C -bus Control Register
- I²C STAT,Multi-master I²C -bus Control/Status Register
- I²C DS, Multi-master I²C -bus TX/RX Data Shift Register
- I²C ADD,Multi-master I²C -bus Address Register

The SDA and SCL lines should both be at High level when the 12C-bus is free. A Start condition can be initiated by a High-to-Low transition of SDA. A Stop condition can be initiated by a Low-to-High transition of SDA while SCL remains steady at High Level.

Start and Stop conditions can always be generated by Master devices. The slave device that the bus master device has selected can be determined by a 7-bit address value in the first data byte, which is put onto the bus after the Start condition has been initiated. The direction of the transfer (read or write) is determined by the 8th bit.

Each SDA line data byte should total eight bits. The number of bytes that can be received or sent during the bus transfer operation is not limited. An acknowledge (ACK) bit should immediately follow every byte, and data is always sent from the most significant bit (MSB) first.

BLOCK DIAGRAM

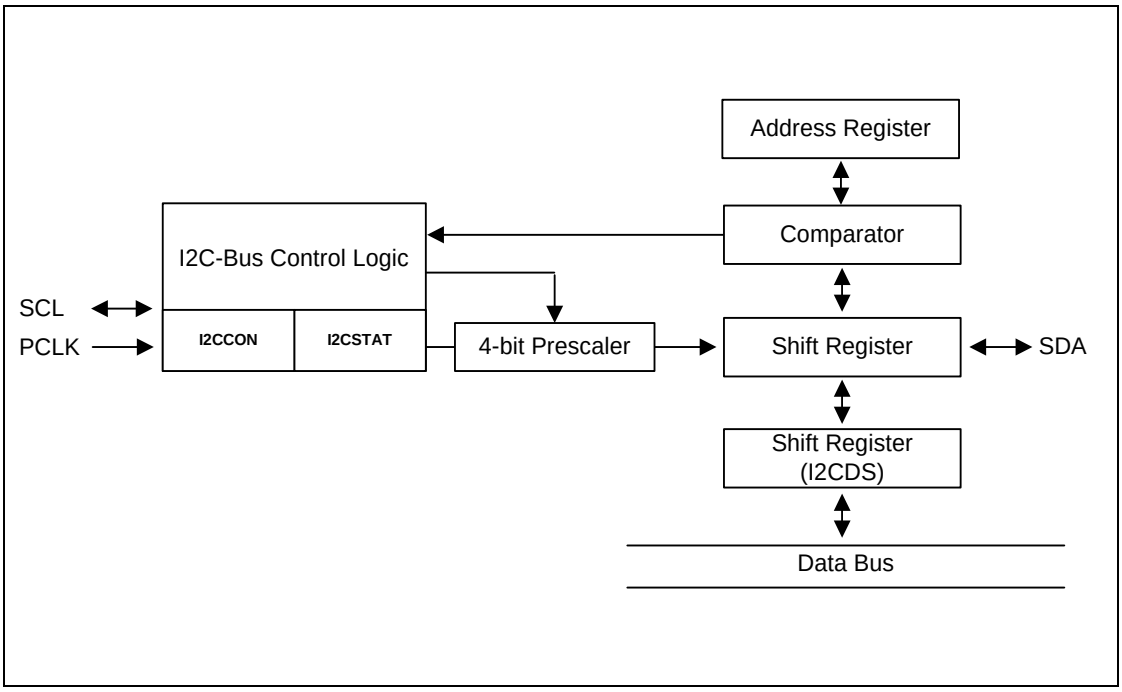


Figure 20-1. I²C Block Diagram

20.2 OPERATION

20.2.1 THE I²C-BUS INTERFACE

There are four operation modes in the MP2520F I²C -bus interface:

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode

The following describes functional relationships among these operating modes:

20.2.1.1 START AND STOP CONDITIONS

The I2-C bus is usually in slave mode when it is inactive. That is, the interface should be in slave mode before detecting a Start condition on the SDA line.(A High-to-Low transition of the SDA line can be initiated by a Start condition while the clock signal of SCL is High). A data transfer on the SDA line can be initiated and SCL signal generated when the interface state is changed to master mode.

A single byte serial data over the SDA line can be transferred after a Start condition, and the data transfer can be terminated by a Stop condition. A Stop condition is a Low-to-High transition of the SDA line while SCL is High. Stop and Start conditions are always generated by the master. When a Start condition is generated, the I^2C -bus is busy. The I^2C -bus will be free again within a few clocks after a Stop condition.

A slave address is sent to notify the slave device when a master initiates a Start condition. A 7-bit address and a 1-bit transfer direction indicator (write or read) are included in the single byte of the address field. A write operation (transmit operation) is indicated when bit 8 is 0; request for data read (receive operation) is indicated when bit 8 is 1.

The transfer operation will be completed by the master through transmitting a Stop condition. Another Start condition and a slave address should be generated when the master wants to continue data transmission to bus. So the read-write operation can be performed in various formats.

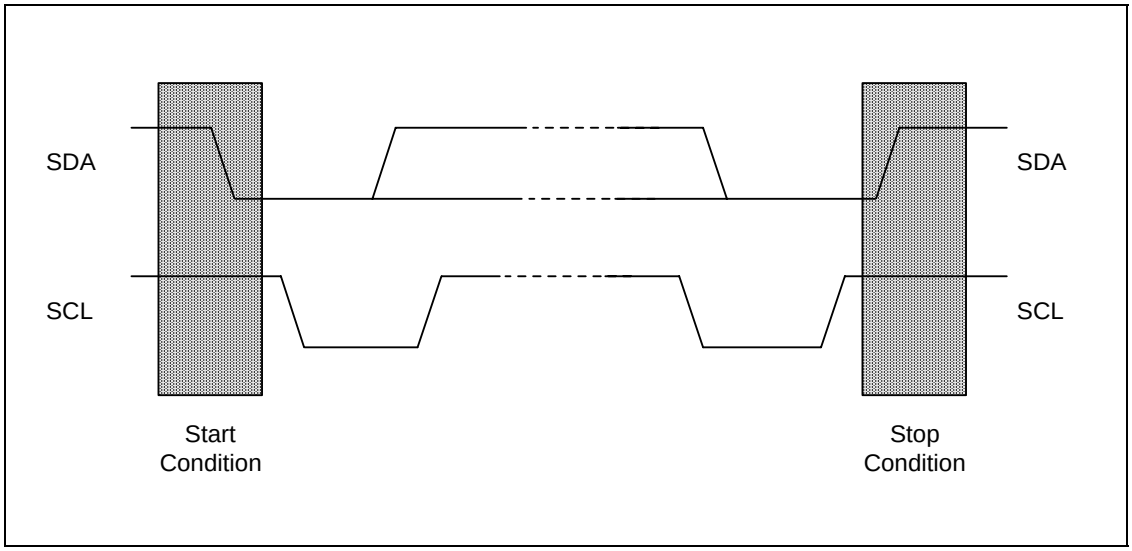


Figure 20-2. Start and Stop Condition

20.2.1.2 DATA TRANSFER FORMAT

Every Data will be transmitted on the SDA line byte should be 8 bits long. The number of bytes that can be transmitted per transfer is unlimited. The address filed should be contained in the first byte following a Start condition. When the I^2C -bus is operating in master mode, the master can transmit the address field. An acknowledge (ACK) bit should follow each byte. The MSB bit of the serial data and addresses are always sent first.

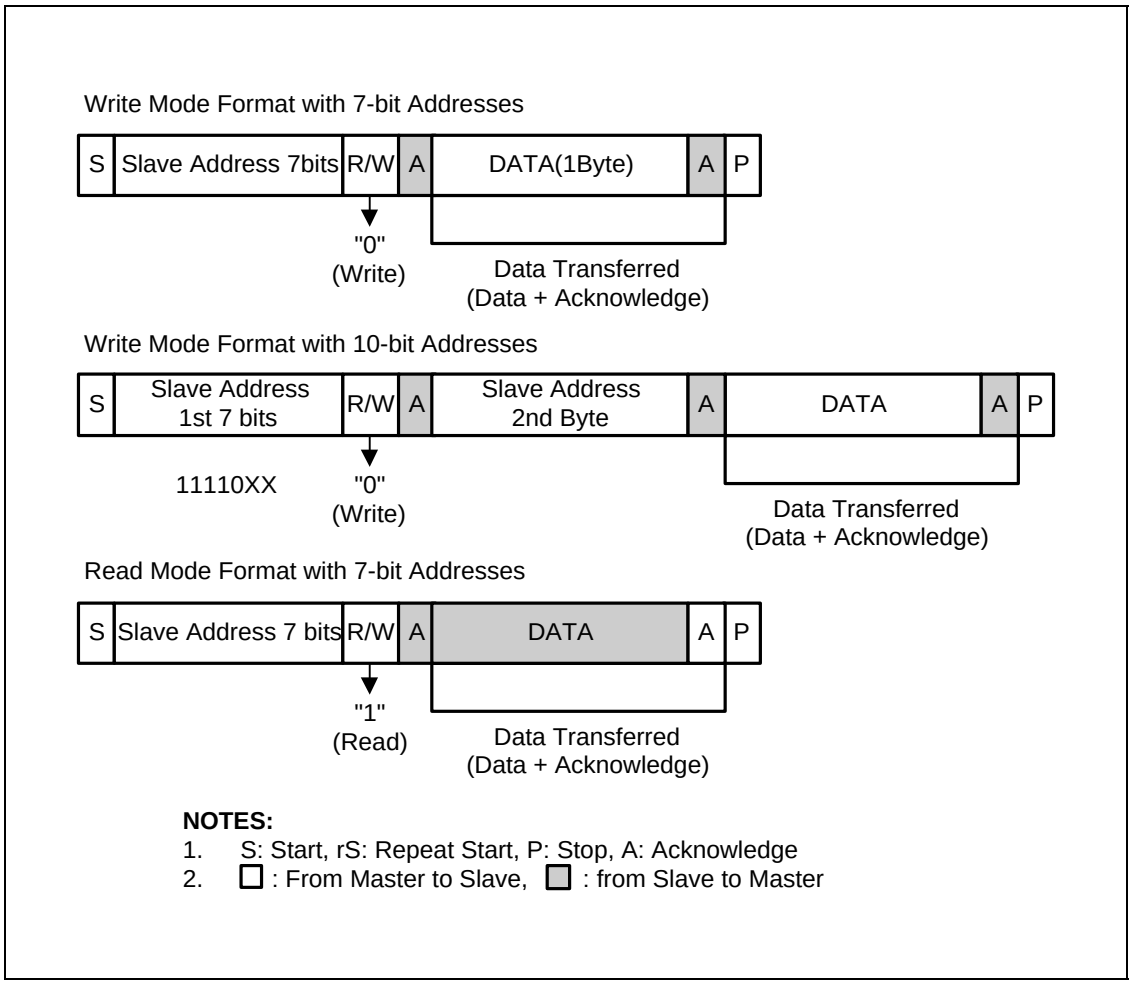


Figure 20-3. I^2C -Bus Interface Data Format

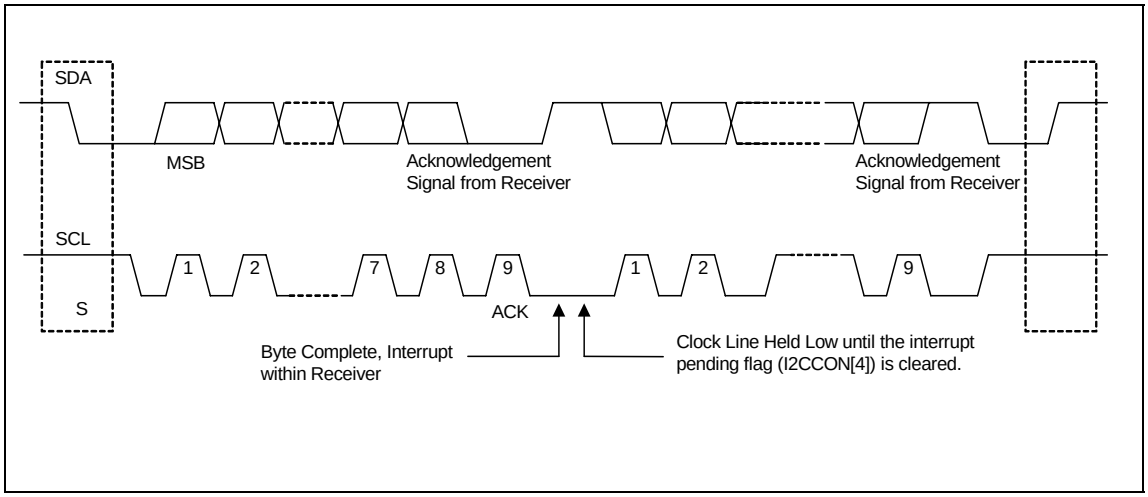


Figure 20-4. Data Transfer on the I^{2}C -Bus

20.2.1.3 ACK SIGNAL TRANSMISSION

An ACK should be sent by the receiver to the transmitter Master to finalize a single byte transfer operation. The ACK pulse should occur at the ninth clock of the SCL line. For the single byte data transfer eight clocks are required. The clock pulse required to transmit the ACK bit should be generated by the master.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received, should release the SDA line. The SDA line should also be driven Low by the receiver during the ACK clock pulse so that SDA is Low during the High period of ninth SCL pulse.

Software (I^{2}C STAT) can enable or disable the ACK bit transmit function. But completion of a single byte data transfer operation requires the ACK pulse on the ninth clock of SCL.

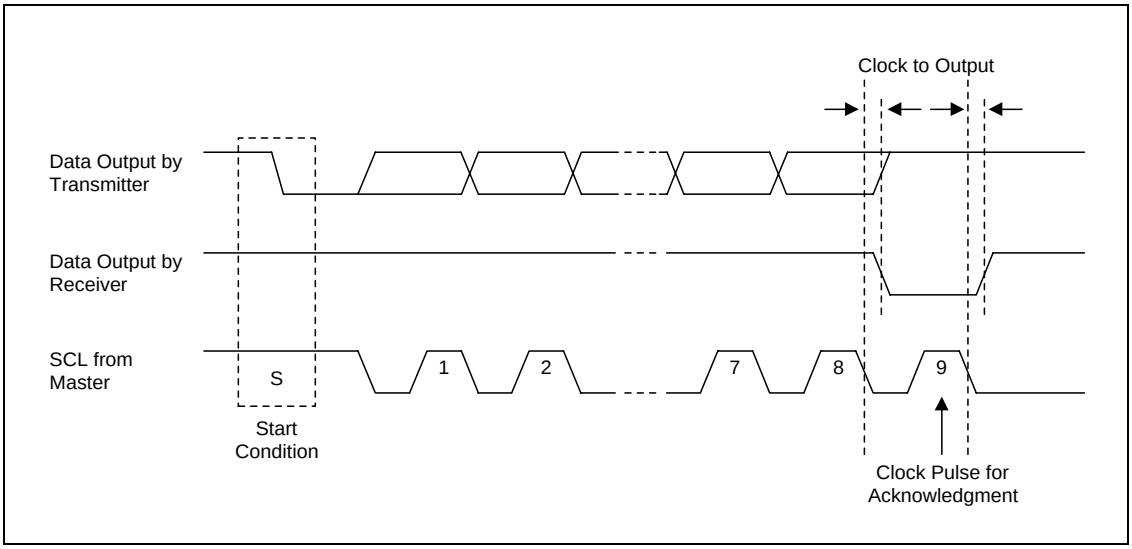


Figure 20-5. Acknowledge on the I²C -Bus

20.2.2 READ-WRITE OPERATION

Until new data is written to the I²C DS (I²C -bus Data Shift Register) the I²C -bus interface will wait after the transmission of the data in transmitter mode. The SCL line will be held Low until the new data is written. The SCL line will be released after the new data is written to the I²C DS Register. The interrupt should be held by the MP2520F to identify competition of the current data transfer. New data should be written to I²C DS again after the interrupt is received by the CPU.

Until the I²C DS Register is read, the I²C -bus interface will wait after data is received in receive mode. The SCL line will be held Low until the new data is read. The SCL line will be released after the new data is read from the I²C DS Register. The interrupt should be held by the MP2520F to identify the completion of the new data reception. The data should be read from I²C DS after the interrupt request is received by the CPU.

20.2.2.1 BUS ARBITRATION PROCEDURES

To prevent conflict between two masters on the bus, arbitration takes place on the SDA line. A data transfer by a master with an SDA High level will not be initiated if another master with an SDA active Low level is not detected because the current level on the bus does not correspond to its own level. Until the SDA line turns High, the arbitration procedure will be extended.

But each master should evaluate whether or not the mastership is allocated to itself when each master simultaneously lowers the SDA line. The address bits are detected by each master for the purpose of evaluation. The address bit is also detected on the SDA line while the save address is generated by each master because the lowering of the SDA line is stronger than maintaining High on the line. For instance, a Low is generated by one master as the first address bit, while the other master is maintaining High - in this case, both masters will detect Low on the bus because Low is stronger than High even if the first master is trying to maintain High on the line. When this happens, the Low (as the first bit of the address) generating master will get the mastership and the High (as the first bit of the address) generating master should withdraw from mastership. When Low is generated by both masters as the first bit of the address, there should be arbitration for the second address bit again. This arbitration will continue to the end of the last address bit.

20.2.2.2 ABORT CONDITIONS

The SDA line level should be maintained at High when a slave receiver cannot acknowledge the slave address confirmation. In this case, to abort the transfer, the master should generate a Stop condition.

The end of the slave transmit operation should be signaled when a master receiver is involved in the aborted transfer by canceling the generation of an ACK after the last data byte is received from the slave. To allow a master to generate a Stop condition, the slave transmitter should then release the SDA.

20.2.2.3 CONFIGURING THE I^2C -BUS

In the I^2C CON Register, the 4-bit prescaler value can be programmed to control the frequency of the serial clock (SCL). The I^2C -bus interface address is stored in the I^2C -bus address register, I^2C ADD. (By default, the value of I^2C -bus interface address is unknown.)

20.2.3 FLOWCHARTS OF THE OPERATIONS IN EACH MODE

Before any of the I^2C TX/RX operations, the following steps should take place:

1) Write own slave address on the I^2C ADD register if needed.
2) Set I^2C CON Register.
   a) Enable interrupt
   b) Define SCL period
3) Set I^2C STAT to enable Serial Output.

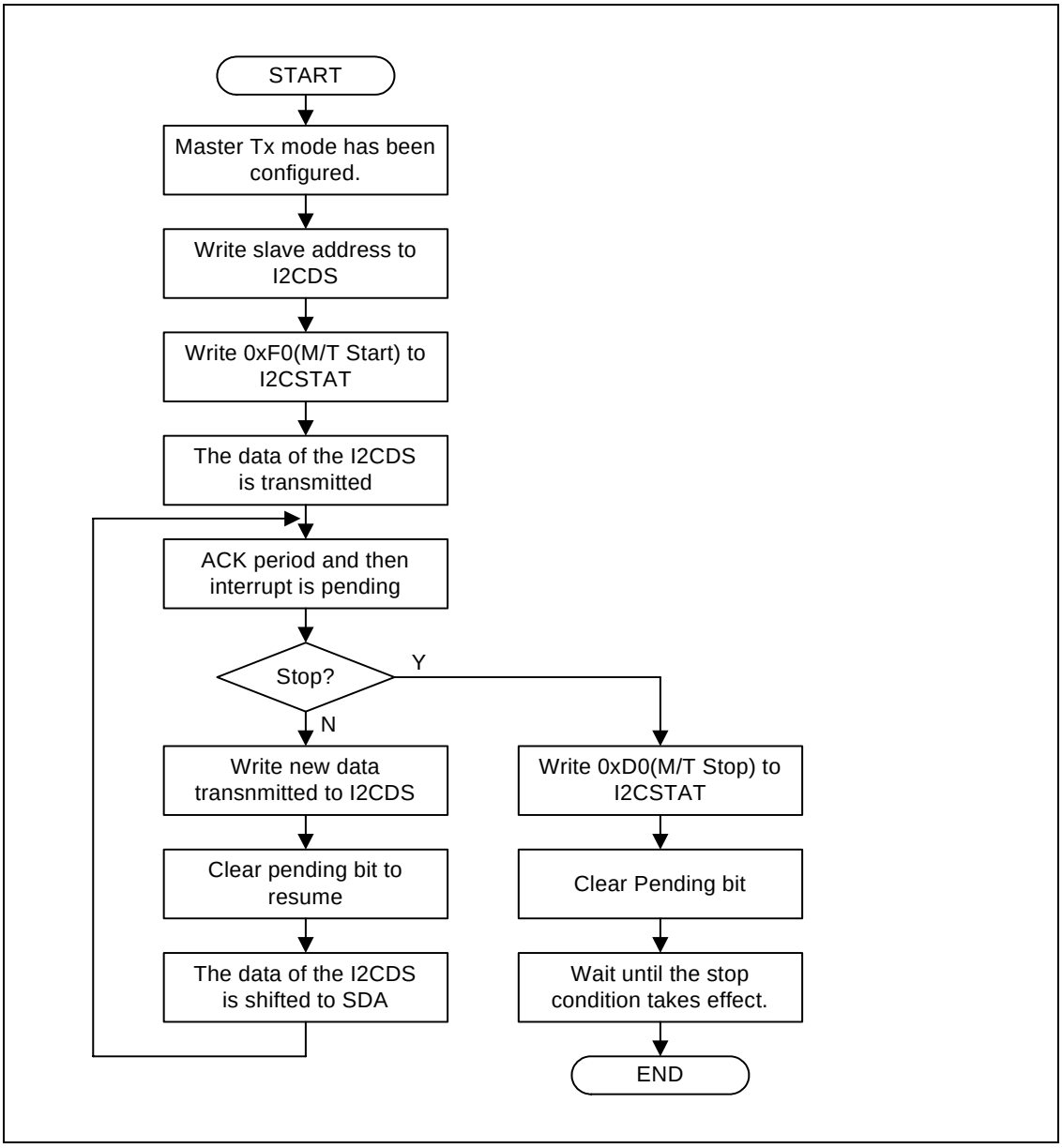


Figure 20-6. Operations for Master/Transmitter Mode

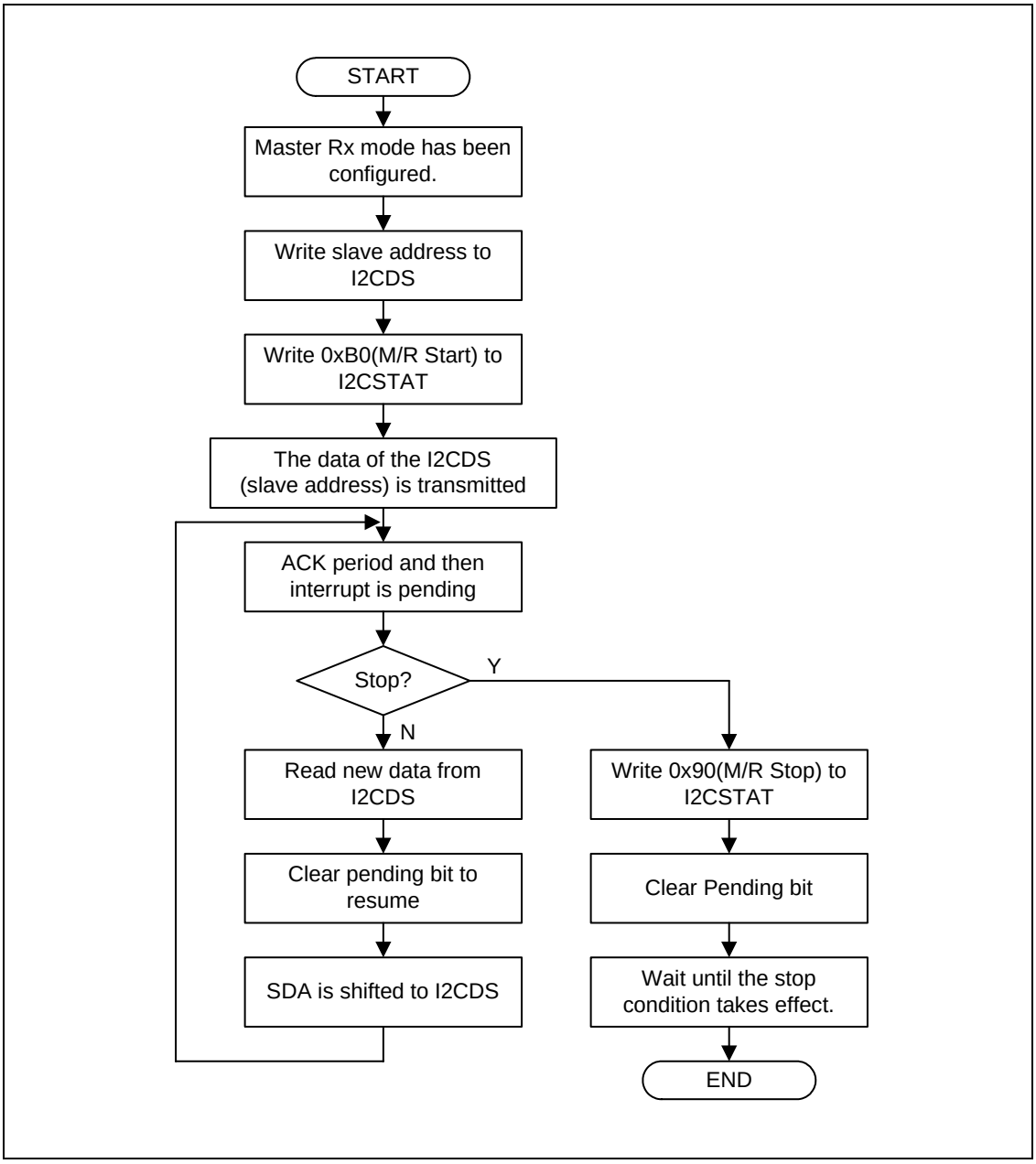


Figure 20-7. Operations for Master/Receiver Mode

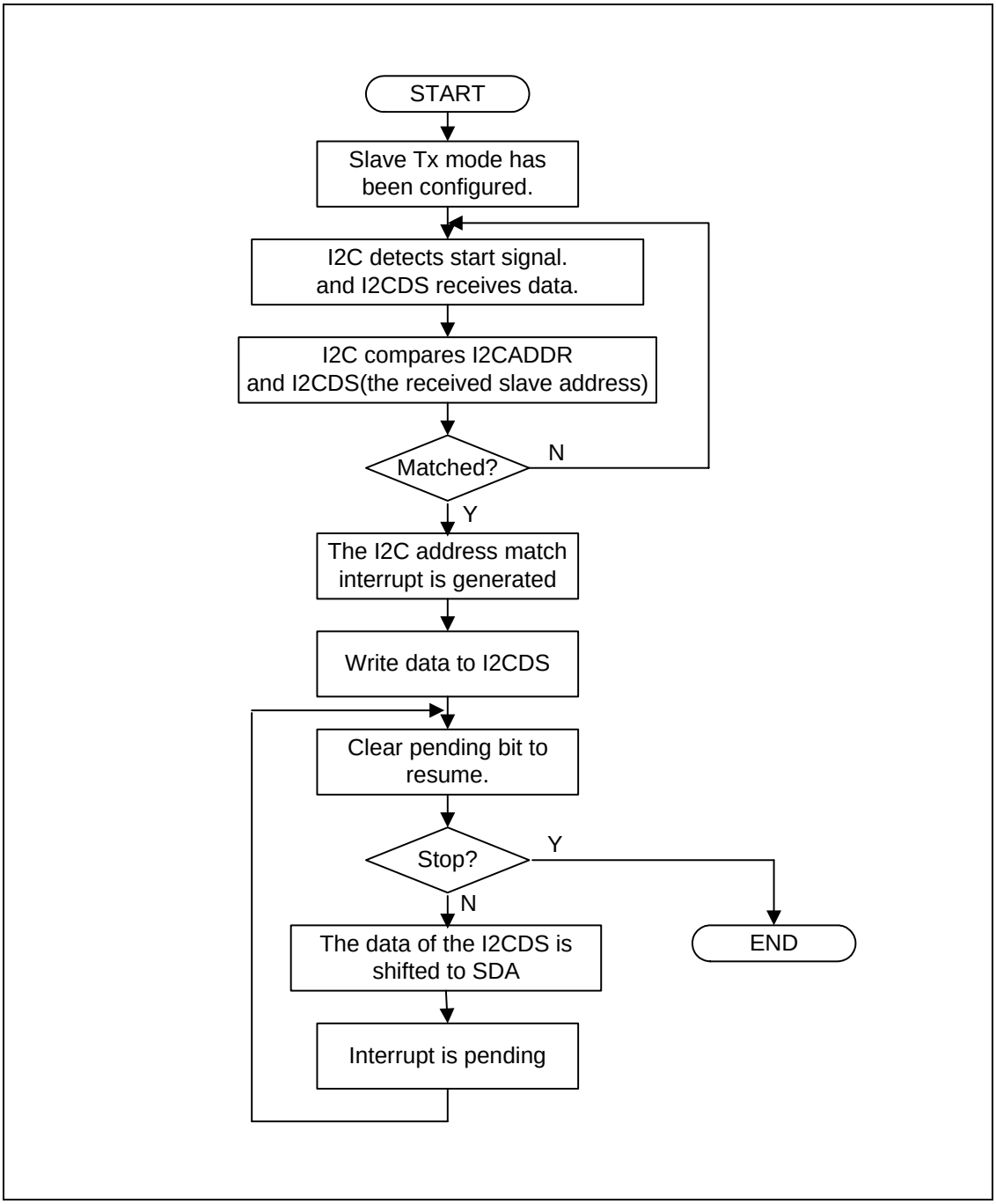


Figure 20-8. Operations for Slave/Transmitter Mode

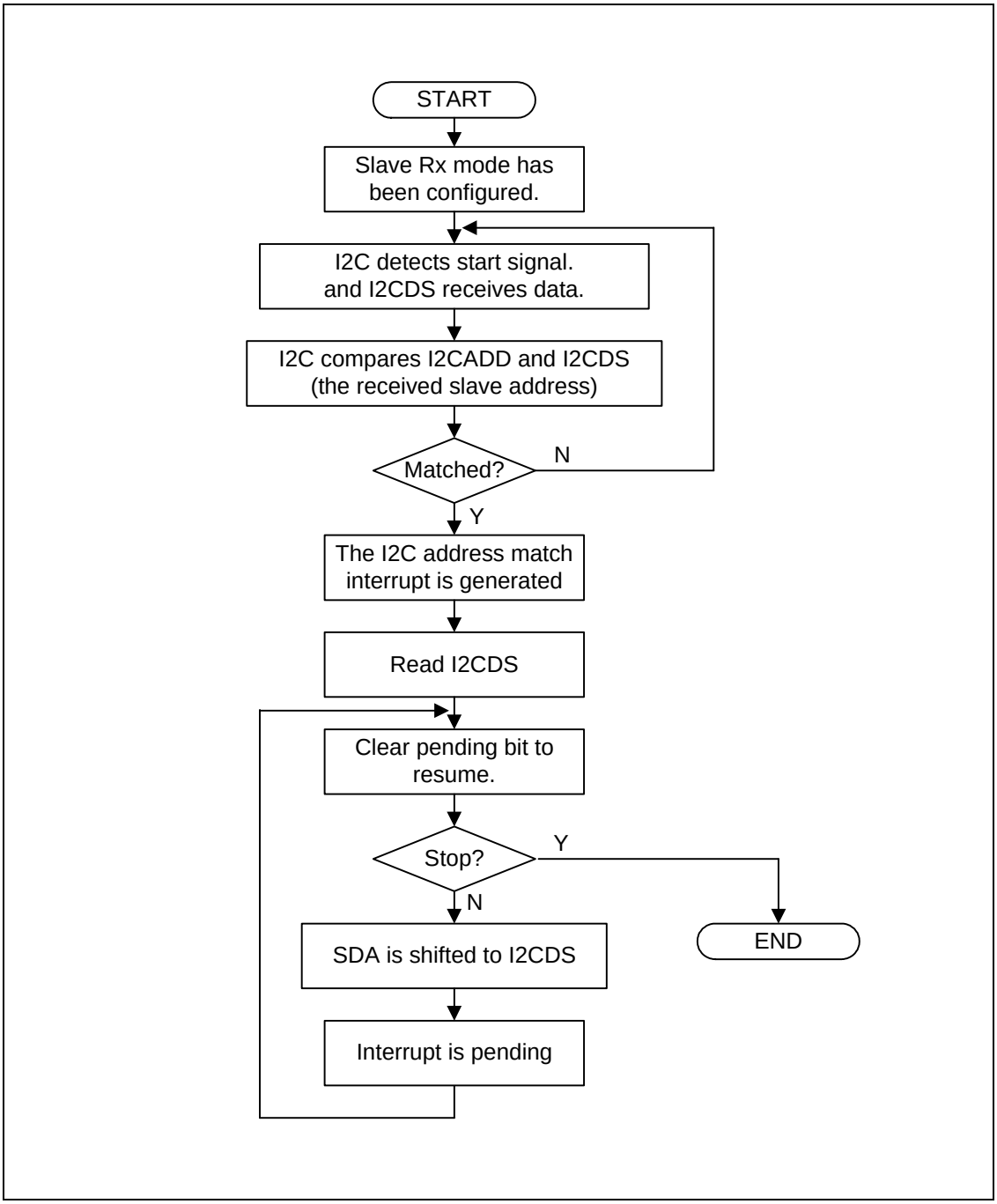


Figure 20-9. Operations for Slave / Receiver Mode

20.3 I²C -BUS INTERFACE REGISTER

Bit	R/W	Symbol	Description	Reset Value
I²C -bus Control Register (I²C CON) ***Address : C000 0D00h***				
[7]	R/W	**ACK_ENB** (1)	I²C -bus acknowledge enable bit 0 = Disable ACK generation 1 = Enable ACK generation In Tx mode, the I²C DS is free in the ACK time. In Rx mode, the I²C DS is L in the ACK time.	0
[6]	R/W	**TX_CLK_SRC**	TX clock source selection bit 0 = PCLK/16 1 = PCLK/512	0
[5]	R/W	**TX/RX INT_ENB** (5)	Tx/Rx Interrupt enable/Disable bit 0 = Disable interrupt 1 = Enable interrupt	0
[4]	R/W	**INT PED_FLAG** **(2) (3)**	Interrupt pending flag When this bit is read as 1, the I²C SCL is tied to L and the I²C is stopped. To resume the operation, clear this bit to 0. 0 = 1) Read - No interrupt pending 2) Write - Clear pending condition and resume the operation 1 = 1) Read - Interrupt is pending 2) Write - N/A	0
[3:0]	R/W	**TRNS_CLK_VAL** (4)	Transmit clock prescaler Transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx Clock = PCLK/(I²C CON[3:0]+1)	Undefined

NOTES:
1. Interfacing with EEPROM, ACK generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. A I²C -bus interrupt occurs 1) when a 1-byte transmit or receive operation is completed, 2) when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To time the setup time of I²C SDA before I²C SCL rising edge, I²C DS has to be written before clearing the I²C interrupt pending bit.
4. I²C CLK is determined by I²C CON[6]. Tx clock can vary by SCL transition time.
When I²C CON[6]=0, I²C CON[3:0]=0x0 or 0x1 is not available.
5. If I²C ON[5]=0, I²C ON[4] does not operate correctly, so it is recommended to set I²C CON[4]=1instead of using the I²C interrupt.

I²C -bus Control/Status Register (I²C STAT)
Address : C000 0D02h

Bit	R/W	Symbol	Description	Reset Value
[7:6]	R/W	**Mode selection**	I^2C -bus master/slave Tx/Rx mode select bits: 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode	0
[5]	R/W	**BUSY_SIG_STAT/** **START STOP condition**	I^2C -Bus busy signal status bit: 0 = read) I^2C -bus not busy. (I^2C always senses BUS start/stop condition.) write) I^2C -bus STOP signal generation 1 = read) I^2C -bus busy write) I^2C -bus START signal generation. The data in I^2C DS will be transferred automatically just after the start signal. Also, the delay for checking the start condition is inserted automatically.	0
[4]	R/W	**SERIAL_O_ENB**	I^2C -bus data output enable/disable bit: 0=Disable Rx/Tx 1=Enable Rx/Tx	0
[3]	R/W	**ARBIT_STAT** **_FLAG**	I^2C -bus arbitration procedure status flag bit: 0 = Bus arbitration successful 1 = Bus arbitration failed during serial I/O	0
[2]	R/W	**ADDR_SLV_FLAG**	I^2C -bus address-as-slave status flag bit: 0 = cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the I^2C ADD	0
[1]	R/W	**ADDR_ZERO** **_FLAG**	I^2C -bus address zero status flag bit: 0 = cleared when START/STOP condition was detected at the SDA/SCL line 1 = Received slave address is 00000000b	0
[0]	R/W	**LRB_STAT**	I^2C -bus last-received bit status flag bit 0 = Last-received bit is 0 (ACK was received. 1 = Last-receive bit is 1 (ACK was not received)	0
Master I^2C -bus Address Register (I^2C ADD) ***Address : C000 0D04h***				
[7:0]	R/W	**SLV_ADDR**	7-bit slave address, latched from the I^2C -bus: When serial output enable=0 in the I^2C STAT, I^2C ADD is write-enabled. The I^2C ADD value can be read any time, regardless of the current serial output enable bit (I^2C STAT) setting. I^2C ADD is used only when the I^2C mode is selected to slave receive/transmit mode. Slave address = [7:1] Not mapped = [0]	XXXX_XXX X

Bit	R/W	Symbol	Description	Reset Value
I^2C -bus Transmit/Receive Data Shift Register (I^2C DS) ***Address : C000 0D06h***				
[7:0]	R/W	**DAT_SHIFT**	8-bit data shift register for I^2C -bus Tx/Rx operation: When serial output enable = 1 in the I^2C STAT, I^2C DS is write-enabled. The I^2C DS value can be read any time, regardless of the current serial output enable bit (I^2C STAT) setting. **NOTE:** The bit[0] of data which is transferred just after the start condition, is determined by the mode selection bit. If the mode selection bit is "receive", the bit will be 1(read). If the mode selection bit is "transmit", the bit will be 0(write).	XXXX_XXXX

TABLE 20-1. I^2C -BUS INTERFACE REGISTER

CHAPTER 21

SPDIF CONTROLLER

21. SPDIF CONTROLLER

21.1 OVERVIEW

The SPDIF Controller supports Standard IEC958 Digital audio interface and Input/Output Mode. It enables to transmit high speed data with the DAM controller.

FEATURES

- SPDIF Input/Output interface
- 8 Sample double buffer control
- DMA controller interface

BLOCK DIAGRAM

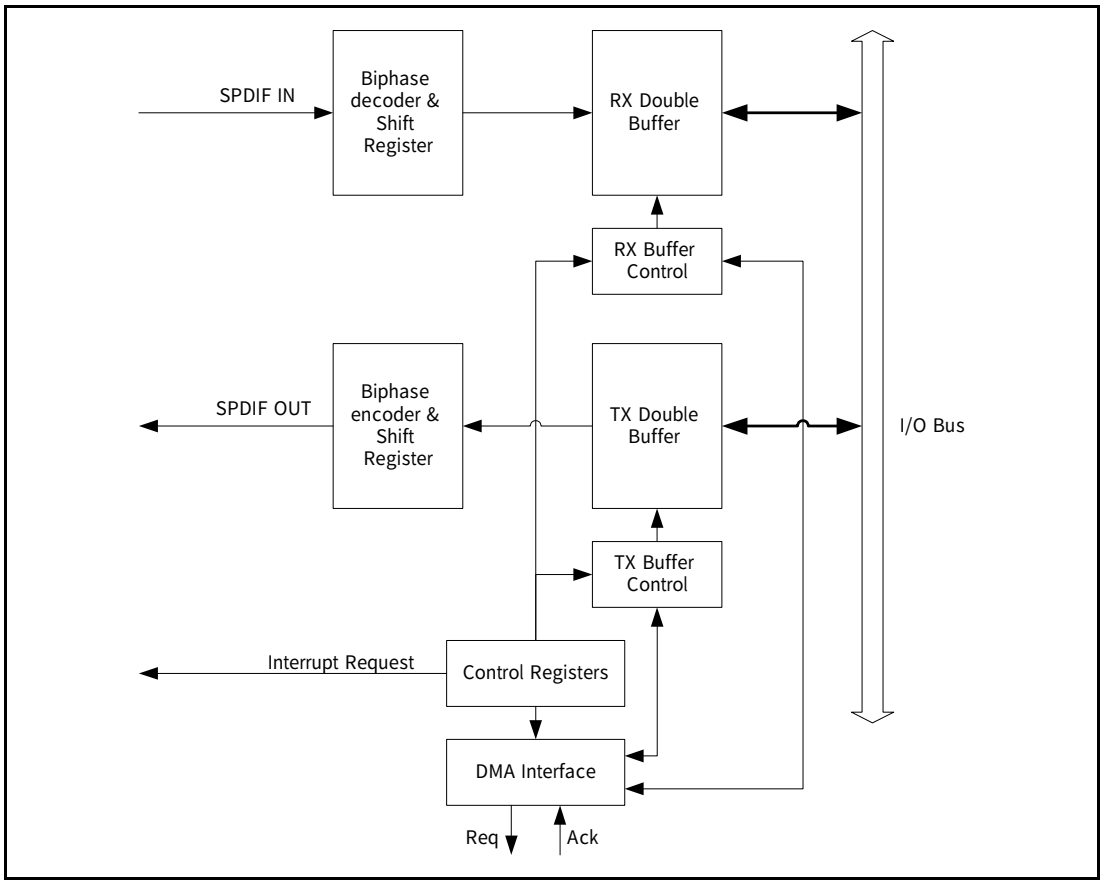


Figure 21-1. SPDIF Block Diagram

21.2 OPERATION

21.2.1 SPDIF Input

The SPDIF controller biphase decodes the data coming via the SPDIF input terminal and stores it in a double buffer. Then it transfers the data to memory by a DMA request. The input data format is as shown below:

31	30	29:28	27	26	25	24	23:0
x	biphase decoding error	[Premable] Type 00 = B (start of new frame or Left channel) 01 = W (Right channel) 10 = M (Left channel)	P	C	U	V	PCM Data or MPEG Audio stream data

TABLE 21-1. SPDIF INPUT DATA FORMAT

The SPDIF input data decoding clock source and frequency is determined by the SPDIF input clock source register and the division ratio register of the Power manager. For this, the SPDIF input frequency has to be 10 times the bit rate. For example, if a sampling frequency is 44.1 KHz, the bit rate becomes 2.8 MHz and the SPDIF input frequency has to be 28 MHz.

21.2.2 SPDIF Output

The SPDIF controller writes data read from memory by a DMA request to an internal double buffer. Then it biphase encodes the data and sends it to the SPDIF output terminal. The output data format is as shown below:

31:28	27	26	25	24	23:0
xxxx	x	C	U	V	PCM Data or MPEG Audio stream data

TABLE 21-2. SPDIF OUTPUT DATA FORMAT

The SPDIF output data encoding clock source and frequency is determined by the SPDIF output clock source and the division ratio of the Power manager. For this, the SPDIF output frequency has to be two times the bit rate * (SPDIFTXDIV+1). For example, if a sampling frequency is 44.1 KHz, the bit rate becomes 2.8 MHz and the SPDIF output frequency has to be 2.8 * 2 * 3 = 16.8 MHz.

21.2.3 SPDIF Control Register (SPDIFCON)

The SPDIFCON is the register that controls the SPDIF operation. The SPDIF_ENB enables the operations of all blocks. The SPDIF_TXENB and the SPDIF_RXENB enable the TX and the RX operations respectively.

Address : C000 4200h

Bit	R/W	Symbol	Description	Reset Value
[15:14]	R/W	**Reserved**	-	-
[13]	R/W	**SPDIF_ENB**	SPDIF Operation Enable	0
[12:10]	R/W	**Reserved**	-	-
[9]	R/W	**SPDIF_TXENB**	SPDIF TX Enable	0
[8:5]	R/W	**Reserved**	-	-
[4]	R/W	**SPDIF_RXENB**	SPDIF RX Enable	0

TABLE 21-3. SPDIF CONTROL REGISTER (SPDIFCON)

21.2.4 SPDIF Interrupt Enable Register (SPDIFINTENB)

The SPDIFINTENB determines the initiation of an interrupt when a biphase decoding error occurs on the SPDIF input operation.

When the BIPERRINTENB bit is '1', an interrupt occurs.

Address : C000 4202h

Bit	R/W	Symbol	Description	Reset Value
[15:5]	R/W	**Reserved**	-	-
[4]	R/W	**BIPERRINTENB**	Biphase decoding error interrupt enable	0
[3:0]	R/W	**Reserved**	-	-

TABLE 21-4. SPDIF INTERRUPT ENABLE REGISTER (SPDIFINTENB)

21.2.5 SPDIF Interrupt Status Register (SPDIFSTATUS)

The SPDIFSTATUS is the pending register of the biphase error interrupt.

Address : C000 4204h

Bit	R/W	Symbol	Description	Reset Value
[15:5]	R/W	**Reserved**	-	-
[4]	R/W	**BIPERR**	Biphase decoding error interrupt pending	0
[3:0]	R/W	**Reserved**	-	-

TABLE 21-5. SPDIF INTERRUPT STATUS REGISTER (SPDIFSTATUS)

21.2.6 SPDIF TX Clock Divider Register (SPDIFTXDIV)

The SPDIFTXDIV is the resister that determines the division ratio of the SPDIF output clock. For N-division, write the N-1 value.

Address : C000 4206h

Bit	R/W	Symbol	Description	Reset Value
[15:0]	R/W	**TXDIV**	TX clock divider	0

TABLE 21-6. SPDIF TX CLOCK DIVIDER REGISTER (SPDIFTXDIV)

21.3 SPDIF CONTROLLER REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
SPDIF Control Register (SPDIFCON) ***Address : C000 4200h***				
[15:14]	R/W	**Reserved**	-	-
[13]	R/W	**SPDIF_ENB**	SPDIF Operation Enable	0
[12:10]	R/W	**Reserved**	-	-
[9]	R/W	**SPDIF_TXENB**	SPDIF TX Enable	0
[8:5]	R/W	**Reserved**	-	-
[4]	R/W	**SPDIF_RXENB**	SPDIF RX Enable	0
SPDIF Interrupt Enable Register (SPDIFINTENB) ***Address : C000 4202h***				
[15:5]	R/W	**Reserved**	-	-
[4]	R/W	**BIPERRINTENB**	Biphase decoding error interrupt enable	0
[3:0]	R/W	**Reserved**	-	-
SPDIF Interrupt Status Register (SPDIFSTATUS) ***Address : C000 4204h***				
[15:5]	R/W	**Reserved**	-	-
[4]	R/W	**BIPERR**	Biphase decoding error interrupt pending	0
[3:0]	R/W	**Reserved**	-	-
SPDIF TX Clock Divider Register (SPDIFTXDIV) ***Address : C000 4206h***				
[15:0]	R/W	**TXDIV**	TX clock divider	0

TABLE 21-7. SPDIF CONTROLLER REGISTERS LIST

CHAPTER 22

AC '97

22. AC97

22.1 OVERVIEW

The AC97 controller supports AC97 revision 2.2 features. The AC97 controller and codec use AC-link for data transmission. AC-link is a serial interface for transferring digital audio, modem, Mic-in, codec register control, and status information.

The AC97 Codec sends the digitized audio samples that the AC97 controller stores in memory. For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the Codec via the AC-link. The external digital-to-analog converter (DAC) in the Codec then converts the audio sample to an analog audio waveform.

This chapter describes the programming model for the AC97 controller. The information in this chapter requires an understanding of the AC97 revision 2.2 specification.

FEATURES

- PCM front (L/R), rear (L/R), center/LFE out.
- Stereo PCM in, momo Mic-in.
- DMA based operation for audio data
- Polling and interrupt based operation for controller.
- Variable sample rate (up to 48 kHz, dependent on external codec).
- All channel support 16/18/20 bits/sample.
- Read/Write access to AC97 codec.

Optional double rate sampling feature and MODEM interface are not supported. Audio data transfer is executed through DMA (max 5 channels). Codec register read/write access is executed in programmed IO mode.

Note: The AC97 and I2S controllers may not be used at the same time.

22.2 PIN DESCRIPTION

The AC97 signals form the AC-link, which is a point-to-point synchronous serial interconnect that supports full-duplex data transfers. All digital audio streams and command/status information are communicated over the AC-link. The AC-link uses GPIOs. Software must configure the GPIOs to use them as the AC-link. The AC-link pins are listed below.

22.2.1 External Interface Signal

There are five signals connected to external AC97 codec. The AC-LINK is a point-to-point serial interconnect.

Name	Direction	Description
AC_SYNC	O	48 kHz frame indicator and synchronization signal
AC_RESET	O	Codec reset signal
SDATA_OUT	O	Serial audio output data to codec
BITCLK	I	12.288 MHz clock from codec
SDATA_IN0	I	Serial audio input data from codec

TABLE 22-1. EXTERNAL INTERFACE SIGNAL

22.3 OPERATION

22.3.1 AC-link Protocol

The AC97 Codec incorporates a five-pin digital serial interface that links it to the AC97 Controller. AC-link is a full-duplex, fixed-clock, PCM digital stream. It employs a time division multiplexed (TDM) scheme to handle control register accesses and multiple input and output audio streams. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams. Each stream has 20-bit sample resolution and requires a DAC and an ADC with a minimum 16-bit resolution.

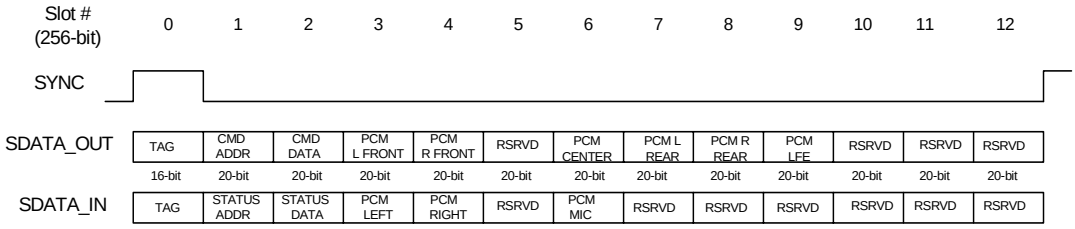


Figure 22-1. AC97 Standard Bidirectional Audio Frame

The above figure shows Tag and Data Phase organization for the controller and the Codec. The figure also lists the slot definitions that the AC97 Controller supports. The AC97 Controller provides synchronization for all data transaction on the AC-link. A data transaction is made up of 256 bits of information broken up into groups of 13 time slots, and is called a frame.

Time slot 0 is called the Tag Phase and is 16 bits long. The other 12 time slots are called the Data Phase. The Tag Phase contains one bit that identifies a valid frame and 12 bits that identify the time slots in the Data Phase that contain valid data. Each time slot in the Data Phase is 20 bits long. A frame begins when SYNC goes high. The amount of time that SYNC is high corresponds to the Tag Phase.

AC97 frames occur at fixed 48 kHz intervals and are synchronous to the 12.288 MHz bit rate clock, BITCLK. The controller and the Codec use SYNC and BITCLK to determine when to send transmit data and when to sample received data. A transmitter transitions the serial data stream on each rising edge of BIT_CLK and a receiver samples the serial data stream on the falling edges of BITCLK.

The transmitter must tag the valid slots in its serial data stream. The valid slots are tagged in slot 0. Serial data on the AC-link is arranged by most significant bit (MSB) to least significant bit (LSB). The Tag Phase's first bit is bit 15 and the first bit of each slot in the Data Phase is bit 19. The last bit in any slot is bit 0.

22.3.1.1 AC-link Output Frame (SDATA_OUT)

The audio output frame data stream corresponds to the multiplexed bundles that make up the digital output data that targets the AC97 DAC inputs and control registers. Each audio output frame supports up to twelve 20-bit outgoing data time slots. If the data mode is not 20-bit mode, the unused least significant bits are padded with zeroes.

A new audio output frame begins with a low-to-high SYNC transition synchronous to BITCLK's rising edge. BITCLK's falling edge immediately follows and AC97 samples SYNC's assertion. BITCLK's falling edge marks the instance that AC-link's sides are each aware that a new audio frame has started. On BITCLK's next rising edge, the AC97 controller transitions SDATA_OUT into the slot 0's first bit position (valid frame bit).

Each new bit position is presented to AC-link on a BITCLK rising edge and then sampled by AC97 on the following BITCLK falling edge. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time-aligned. The SDATA_OUT composite stream is MSB-justified (MSB first).

The AC97 controller fills all non-valid slot bit positions with zeroes. If fewer than 20 valid bits exist in an assigned valid time slot, the controller stuffs all trailing non-valid bit positions of the 20-bit slot with zeroes. For example, if a 16-bit sample stream is being played to an AC97 DAC, the first 16 bit positions are presented to the DAC MSB-justified. They are followed by the next four bit positions that the controller stuffs with zeroes. This process ensures that the least significant bits do not introduce any DC biasing, regardless of the implemented DAC's resolution (16-, 18-, or 20-bit).

Note : When the AC97 controller transmits mono audio sample streams, the software must ensure that the left and right sample stream time slots are filled with identical data.

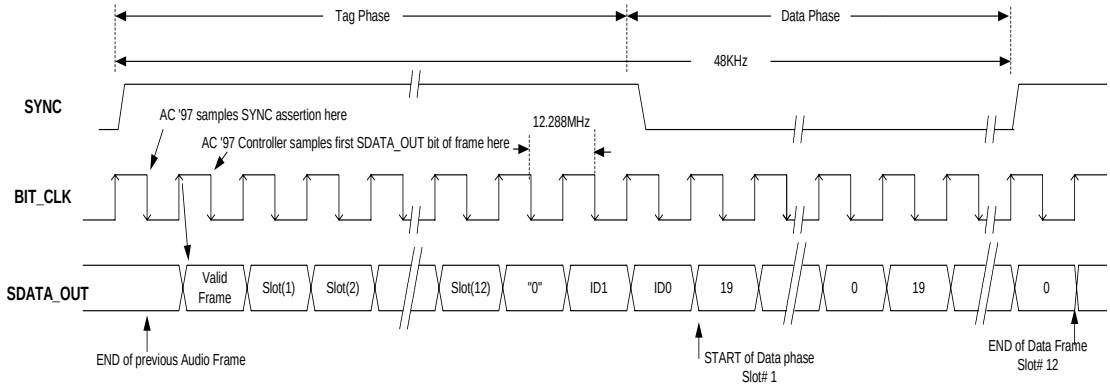


Figure 22-2. AC-link Audio Output Frame

22.3.1.2 AC-link INput Frame (SDATA_IN)

The AC-link audio input frame consists of twelve 20-bit time slots. Slot 0 is reserved and contains 16 bits that are used for AC-link protocol infrastructure. The controller must poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the codec is in the ready state before it puts the controller into operation.

When the controller is sampled Codec ready, the next 12 bit positions sampled indicate which of the 12 time slots are assigned to input data streams and whether they contain valid data. The next figure illustrates the time slotbased AC-link protocol. A new audio input frame begins when SYNC transitions from low to high. The low to high transition is synchronous to BITCLK's rising edge. On BITCLK's next falling edge, AC97 samples SYNC's assertion. This falling edge marks the moment that AC-link's sides are each aware that a new audio frame has started. The next time BITCLK rises, the controller transitions SDATA_IN to the first bit position in slot 0 (Codec ready bit).

Each new bit position is presented to AC-link on a BITCLK rising edge and then sampled by ACUNIT on the following BITCLK falling edge. This sequence ensures that data transitions and subsequent sample points are time-aligned for both incoming and outgoing data streams. The SDATA_IN composite stream is MSB-justified (MSB first) and the AC97 Codec fills non-valid bit positions with zeroes. SDATA_IN data is sampled on BITCLK falling edges.

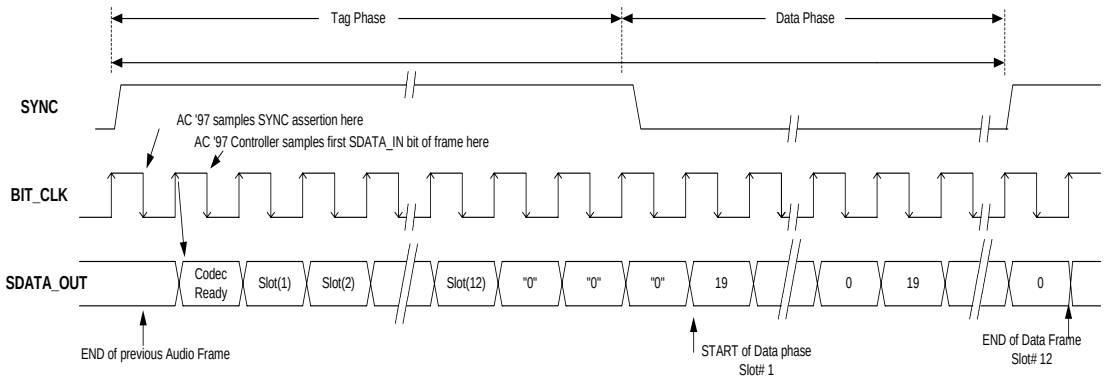


Figure 22-3. AC97 Input Frame

22.3.2 AC97 Controller Operation

All AC97 controller registers can be accessed by the processor and audio data can be accessed only by DMA. Codec registers also can be accessed by the processor after the AC-LINK is activated.

22.3.2.1 Initialization

Prior to activate the AC97 controller, GPIO has to be configured properly. AC97 uses GPIOL[10:6] 5 pins. These pins are configured as GPIO AltFunction1 for AC97 audio in/out function. The GPIO setting steps are as follows:

1) **GPIOL AltFnSelL** register (C000 1036h) is set into '1010_xxxx_xxxx_xxxxb'.
2) **GPIOL AltFnSelH** register (C000 1056h) is set into 'xxxx_xxxx_xx10_1010b'

When global reset signal is 0 or bit 2 of AC_CTRL_REG (cold reset bit) is 0, the AC97 controller and connected codec are in reset state. After bit 2 of AC_CTRL_REG becomes 1, the AC97 controller registers can be accessed. But codec registers are still inaccessible until the AC-LINK is activated.

- All registers except AC_CTRL_REG are in reset state.
- All DMA requests are de-asserted.
- Data buffer status is set to empty state.
- AC-LINK is going to inactive state.

Valid audio output data must be prepared and DMA controller must be configured properly before the host enables the AC-LINK. The AC-LINK is enabled by writing bit 0 of AC_CTRL_REG to 0 (AC-link off bit).

AC97 Control Register (AC_CTRL_REG)

Address : C000 0E00h

Bit	R/W	Symbol	Description	Reset Value
2	RW	**CLD_RESET**	0 : Reset AC97 controller and codec. All data in the controller and the codec will be lost 1 : Normal operation. The value of this bit is retained after suspends, hence, if this bit was set to 1 before a suspend, a cold reset is not generated on a resume.	0b
1	RW	**WRM_RESET**	0 : Warm reset is not generated. 1 : Causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. Available only when AC97 is in powerdown mode.	0b
0	RW	**AC_LINK_OFF**	0 : Enables AC-link between controller and codec. 1 : Disables AC-link between controller and codec. When AC-link is off, only data transfer through AC-link is unavailable. BITCLK is still activated in this mode. Simply by clearing this bit, AC-link is reactivated. When powerdown mode is activated, BITCLK is off. And the AC97 controller and codec is in powerdown state. To activate AC-link again, cold or warm reset procedures are required.	1b

TABLE 22-2. AC97 CONTROL REGISTER (AC_CTRL_REG)

AC97 Config Register (AC_CONFIG_REG)

Address : C000 0E02h

Bit	R/W	Symbol	Description	Reset Value
6 : 4	RW	**EXT_CH_OUT**	Extended channel output enable bits. [6] : Center channel enable. [5] : Rear channel enable. [4] : LFE channel enable.	0h
3 : 2	RW	**OUT_DA_SEC**	Output Data width selection. 0 = 16 bit, 1 = 18 bit, 2 = 20 bit	0h
1 : 0	RW	**IN_DA_SEC**	Input Data width selection. 0 = 16 bit, 1 = 18 bit, 2 = 20 bit	0h

TABLE 22-3. AC_CONFIG_REG

22.3.2.2 Accessing Codec Registers

Codec registers are accessed by translating a 7-bit address to a 32-bit physical address. The software has to use the following formula to translate a 7-bit codec address to 32 bit physical address.
Physical address for a codec = 0xC000 0F00 + Shift Left Once (7-bit codec address)

The software must first check the AC-LINK status by reading AC_CODEC_ACCESS register. The AC-LINK is free if the register value is 0. If the host processor requests an access to any codec register, this bit is set to 1. This bit is cleared by the controller when the codec write/read operation has been completed.

The controller sets bit 6 of the AC_STATUS_REG after the completion of a codec write operation, and the bit 5 of AC_STATUS_REG after the completion of a codec read operation.
Reading a codec register is done using the following steps.

i) First the software issues a read command to a codec register. The controller responds to this operation with invalid data. The controller then initiates a read access across the AC-LINK.
ii) The completion of a codec read operation is signaled by setting bit 5 of AC_STATUS_REG.
iii) The software then reads the AC_CODEC_DATA register and the controller returns valid data.

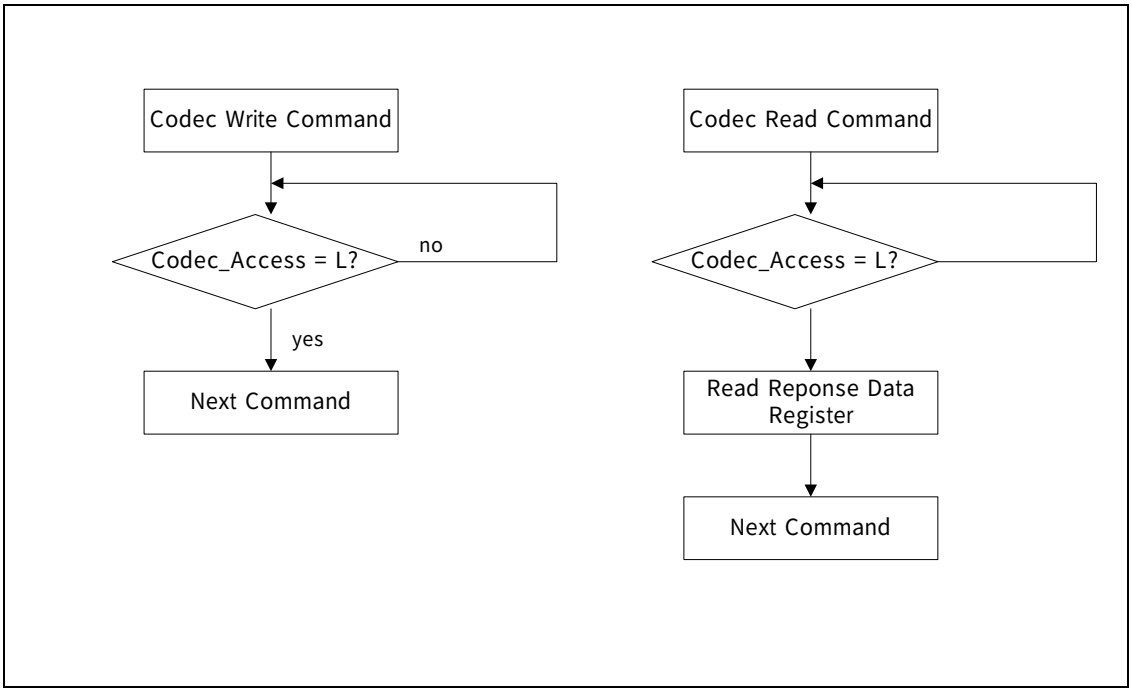


Figure 22-4. AC '97 Command Read/Write Flow Chart

AC97 Status Enable Register (AC_STA_ENA_REG)

Address : C000 0E04h

Bit	R/W	Symbol	Description	Reset Value
7	RW	**COD_RD_ST**	Codec Ready status enable. 0 : Disable codec ready status. 1 : Enable codec ready status.	0b
6	RW	**COD_REG_WD_ST**	Codec Register Write Done status enable. 0 : Disable codec register write command done status. 1 : Enable codec register write command done status.	0b
5	RW	**COD_REG_RD_ST**	Codec Register Read Done status enable. 0 : Disable codec register read command done status. 1 : Enable codec register read command done status.	0b
4	RW	**FOUT_BUF_ UFLW_ST**	Front Out Buffer Underflow status enable. 0 : Disable front out buffer underflow status. 1 : Enable front out buffer underflow status.	0b
3	RW	**ROUT_BUF_ UFLW_ST**	Rear Out Buffer Underflow status enable. 0 : Disable rear out buffer underflow status. 1 : Enable rear out buffer underflow status.	0b
2	RW	**PCM_INBUF_ OFLW_ST**	PCM In Buffer Overflow status enable. 0 : Disable PCM in buffer overflow status. 1 : Enable PCM in buffer overflow status.	0b
1	RW	**MIC_INBUF_ OFLW_ST**	MIC In Buffer Overflow status enable. 0 : Disable Mic in buffer overflow status. 1 : Enable Mic in buffer overflow status.	0b
0	RW	**CT_LF_OBUF_UFL W_ST**	Center/LFE Out Buffer Underflow status enable. 0 : Disable Center/LFE out buffer underflow status. 1 : Enable Center/LFE out buffer underflow status.	0b

TABLE 22-4. AC_STA_ENA_REG

AC97 Global Status Register (AC_STATUS_REG)

Address : C000 0E06h

Bit	R/W	Symbol	Description	Reset Value
7	RW	**COD_READY**	Codec Ready. Reflects the status of the codec ready bit. 0 : Codec is not ready. 1 : Codec is ready.	0
6	RW	**COD_REG_WD**	Codec Register Write Done. Set to '1' after controller sends command address and data to codec. This bit is cleared when the processor starts new access to codec registers. 0 : Codec register write command is not completed. 1 : Codec register write command is completed.	0
5	RW	**COD_REG_RD**	Codec Register Read Done. Set to '1' after controller receives status address and data from codec. This bit is cleared when the processor starts new read access to codec. 0 : Codec register read command is not completed. 1 : Codec register read command is completed.	0
4	RW	**FOUT_BUF_ UFLW**	Front Out Buffer Underflow. Last valid data is repeatedly sent out. 0 : Front out buffer is not empty. 1 : Front out buffer is empty.	0
3	RW	**ROUT_BUF_ UFLW**	Rear Out Buffer Underflow. Last valid data is repeatedly sent out. 0 : Rear out buffer is not empty. 1 : Rear out buffer is empty.	0
2	RW	**PCM_INBUF_ OFLW**	PCM In Buffer Overflow. Data in the receive buffer is overwritten. 0 : PCM in buffer is not full. 1 : PCM in buffer is full.	0
1	RW	**MIC_INBUF_ OFLW**	MIC In Buffer Overflow. Data in the receive buffer is overwritten. 0 : Mic in buffer is not full. 1 : Mic in buffer is full.	0
0	RW	**CT_LF_OBUF_UFL W**	Center/LFE Out Buffer Underflow. Last valid data is repeatedly sent out. 0 : Center/LFE out buffer is not empty. 1 : Center/LFE out buffer is empty.	0

TABLE 22-5. AC_STATUS_REG

The Status Register Bits are cleared by writing 1 to each bit.

AC97 State Machine Register (AC_STATE_MACHINE)

Address : C000 0E08h

Bit	R/W	Symbol	Description	Reset Value
2 : 0	RW	**AC_ST_MCH**	AC97 state machine. 000b : Idle State. 001b : Init State. The controller registers are ready to be accessed by the processor, but ACLINK is off. 010b : Active State. Both the controller and codec are activated and ACLINK is on. 011b : Powerdown State. Both the controller and codec are in powerdown mode. ACLINK is off. 100b : Warm Reset State. Wake up process from powerdown mode to normal operation is progressed.	000b

TABLE 22-6. AC_STATE_MACHINE

AC97 Codec Address Register (AC_CODEC_ADDR)

Address : C000 0E0Ch

Bit	R/W	Symbol	Description	Reset Value
6 : 0	R	**AC_CODEC_ ADDR**	7 bit Codec register address of the last accessed codec register by the processor.	0h

TABLE 22-7. AC_CODEC_ADDR

AC97 Codec Register Read Data Register (AC_CODEC_DATA)

Address : C000 0E0Eh

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**AC_CODEC_ DATA**	Codec register data of the last read access by the processor. Use this register when CPU wants to read codec registers. Valid codec register data is available after Codec Register Read Done bit (bit 5 of AC_STATUS_REG) is set. Received data is stored in this register.	0h

TABLE 22-8. AC_CODEC_DATA

AC97 Codec Access Register (AC_CODEC_ACCESS)

Address : C000 0E10h

Bit	R/W	Symbol	Description	Reset Value
0	R	**AC_CODEC_ ACCESS**	Codec access in progress flag. 0 : Codec access is not in progress, so new codec access command available 1 : Codec access is in progress, so CPU must wait until this bit cleared.	0b

TABLE 22-9. AC_CODEC_ACCESS

22.3.3 Clocks and Sampling Frequencies

By default the controller transmits and receives data at a sampling frequency of 48 kHz. However, it can sample data at frequencies of less than 48 kHz if the codec supports "on demand" slot requests.

All data transfers across the AC-LINK are synchronized to the rising edge of the SYNC signal. The controller divides the BITCLK by 256 generate the SYNC. This yields a 48 kHz SYNC signal whose period defines a frame. Data is transitioned on the AC-LINK on every rising edge of BITCLK and subsequently sampled on the receiving side of the AC-LINK on each immediately following falling edge of BITCLK.

The controller synchronizes data between two different clock domains - the BITCLK and the peripheral bus clock. Whether the peripheral bus clock is slower or faster than BITCLK, the controller can synchronize between two clock domains.

22.3.4 Buffers

The AC97 controller has 5 buffers :

1) PCM out, Rear out, Center/lfe out buffer : 16 x 20-bit each
2) PCM in buffer : 16 x 20-bit
3) Mic in buffer : 16 x 20-bit

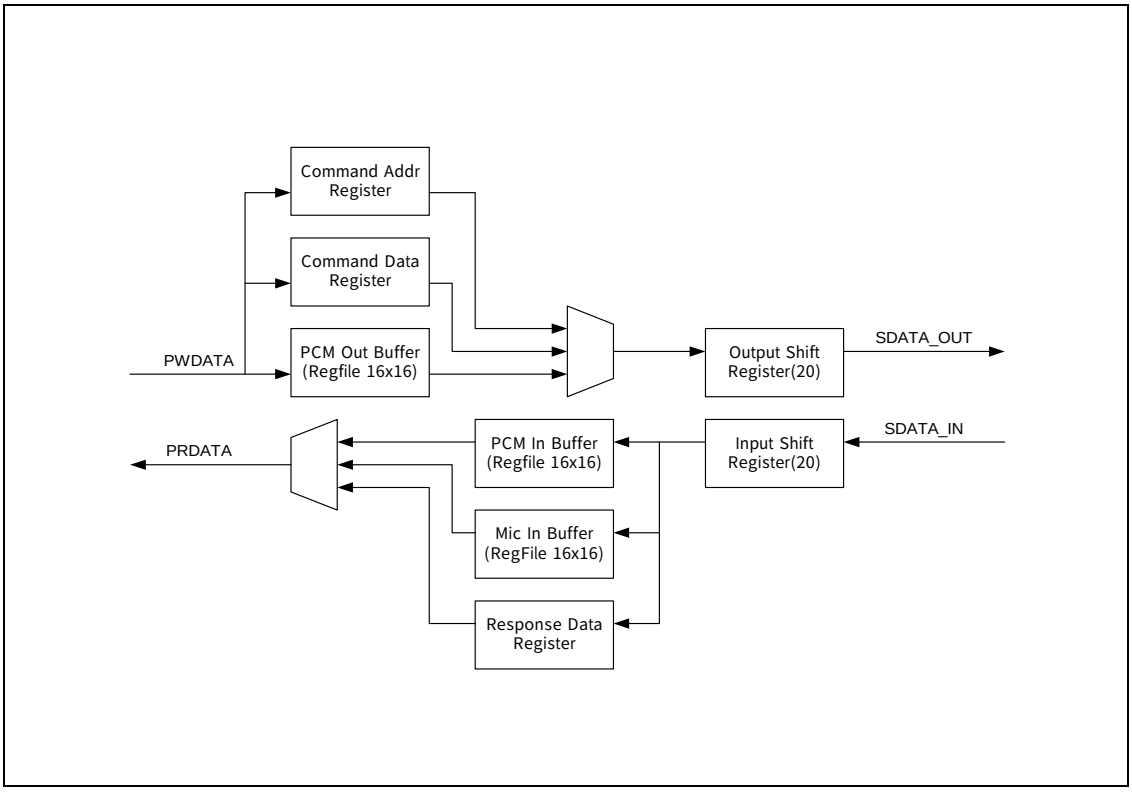


Figure 22-5. Internal Data Path

If the Output buffer contains 8 words of data or more, the controller triggers an output DMA request. Also if the input buffer contains more than or equal to 8 words of data, the controller triggers an input DMA request. That is to say that audio data buffers are controlled as double buffers

22.3.5 Valid Data Structure

Audio data must be in paired structures. For example, the PCM output buffer has to contain front left, front right data alternately for AC-LINK output convenience. Likewise, rear left, rear right data are to be stored alternately and center and LFE data are to be stored alternately.

1. In the case of 16-bit data mode, valid external memory data structures are as follows.

   1) 32 bit word mode

   MS half word = front right, rear right, LFE(Low Frequency Effect) data

   LS half word = front left, rear left, center data

MS half word (FL, RL, Center)	LS half word (FR, RR, LFE)

   In this case, the DMA channel being used is to be configured as follows.

   a) If output

   increment source address, source/target data format is word.

   b) If input

   increment target address, source and target data format is word.

   2) 16 bit half word mode

   First word = front left, rear left, center data (MS, LS both available)

   Second word = front right, rear right, LFE data (MS, LS both available)

Can be used for other channel	First word (FL, RL, Center)
Can be used for other channel	Second word (FR, RR, LFE)

   DMA channel being used is to be configured as follows.

   a) If output,

   increment source address, source and target data format is LS(MS) half word.

   b) If input,

   increment target address, source and target data format is LS(MS) half word.

The unused half word (in the above case, MS half word) can be used for other channel pair data. For example, if LS half word contains front left/right channel data, MS half word can contain rear left/right channel data. Various configurations are possible when the DMA controller is set correctly.

2. In the case of 18-bit or 20-bit data mode, valid external memory data structure is like 16-bit half word mode except for using the remaining half word.

Not used	First word (FL, RL, Center)
Not used	Second word (FR, RR, LFE)

The DMA channel being used is to be configured as follows.

a) If output,
Increment source address, source and target data format is word.

b) If input,
Increment target address, source and target data format is word.

In many audio applications such as MP3 or MPEG audio players, audio data is generated channel by channel. That is to say, after a certain amount of left channel data is written to the external memory, the same amount of right channel data is then written and so on. Valid data structures as above are achieved by the proper setting of memory address increment values and memory format when decoded audio data is written to memory.

22.3.6 Operation Flow

The AC97 controller starts operation after the reset signal is de-asserted. Before activating the AC-LINK interface for transmitting and receiving audio data with codec, the DMA parameter must be configured properly.

If AC-LINK is activated and connected, codec is ready, and the controller and codec can transfer audio data via AC-LINK. The controller uses a maximum of 5 DMA channels, corresponding to PCM front out, rear out, center/LFE out, PCM in, Mic in audio data.

When the processor activates the AC-LINK by setting AC_CTRL_REG as 0b100, the controller starts generating an ACSYNC signal. The following are the functional steps for AC97.

The sequence of DMA parameter and AC97 controller setting can be changed.

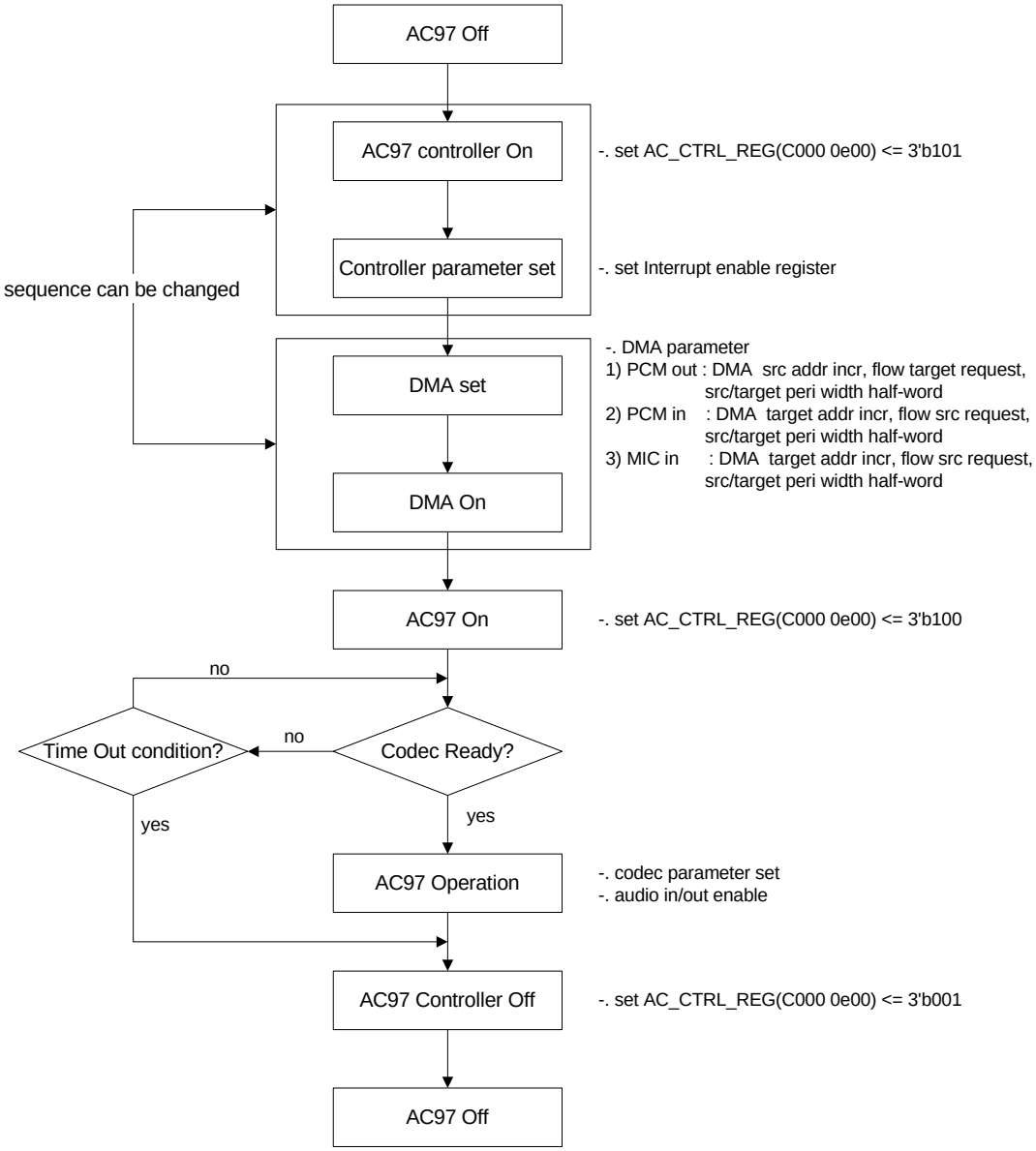


Figure 22-6. AC '97 Operation Flow Chart

22.4 AC97 REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
AC97 Control Register (AC_CTRL_REG) ***Address : C000 0E00h***				
2	RW	**CLD_RESET**	Cold Reset.	0b
1	RW	**WRM_RESET**	Warm Reset.	0b
0	RW	**AC_LINK_OFF**	AC-link Off.	1b
AC97 Config Register (AC_CONFIG_REG) ***Address : C000 0E02h***				
6 : 4	RW	**EXT_CH_OUT**	Extended channel output enable bits.	0h
3 : 2	RW	**OUT_DA_SEC**	Output Data width selection.	0h
1 : 0	RW	**IN_DA_SEC**	Input Data width selection.	0h
AC97 Status Enable Register (AC_STA_ENA_REG) ***Address : C000 0E04h***				
7	RW	**COD_RD_ST**	Codec Ready status enable.	0b
6	RW	**COD_REG_WD_ ST**	Codec Register Write Done status enable.	0b
5	RW	**COD_REG_RD_ ST**	Codec Register Read Done status enable.	0b
4	RW	**FOBUF_UFLW_ST**	Front Out Buffer Underflow status enable.	0b
3	RW	**ROBUF_UFLW_ ST**	Rear Out Buffer Underflow status enable.	0b
2	RW	**INBUF_OFLW_ST**	PCM In Buffer Overflow status enable.	0b
1	RW	**MINBUF_OFLW_ ST**	MIC In Buffer Overflow status enable.	0b
0	RW	**CLOBUF_UFLW_ST**	Center/LFE Out Buffer Underflow status enable.	0b
AC97 Global Status Register (AC_STATUS_REG) ***Address : C000 0E06h***				
7	RW	**COD_READY**	Codec Ready. Reflects the status of the codec ready bit.	0
6	RW	**COD_REG_WD**	Codec Register Write Done.	0
5	RW	**COD_REG_RD**	Codec Register Read Done.	0
4	RW	**FOBUF_UFLW**	Front Out Buffer Underflow.	0
3	RW	**ROBUF_UFLW**	Rear Out Buffer Underflow.	0
2	RW	**INBUF_OFLW**	PCM In Buffer Overflow.	0

Bit	R/W	Symbol	Description	Reset Value
1	RW	**MINBUF_OFLW**	MIC In Buffer Overflow.	0
0	RW	**CLOBUF_UFLW**	Center/LFE Out Buffer Underflow.	0
AC97 State Machine Register (AC_STATE_MACHINE) ***Address : C000 0E08h***				
2 : 0	RW	**AC_ST_MCH**	AC97 state machine.	000b
AC97 Codec Address Register (AC_CODEC_ADDR) ***Address : C000 0E0Ch***				
6 : 0	R	**AC_CODEC_ ADDR**	7 bit Codec register address of the last accessed codec register	0h
AC97 Codec Register Read Data Register (AC_CODEC_DATA) ***Address :*** **C000 0E0Eh**				
15 : 0	R	**AC_CODEC_ DATA**	Codec register data of the last read access by the processor	0h
AC97 Codec Access Register (AC_CODEC_ACCESS) ***Address :*** **C000 0E10h**				
0	R	**AC_CODEC_ ACCESS**	Codec access in progress flag.	0b

TABLE 22-10. AC97 REGISTER LIST

AC97 Codec Registers

Address : C000 0F00h ~ C000 0F7Eh

AC97 Codec 7 bit register addresses are mapped to C000 0F00h ~ C000 0F7Eh.
For example, AC97 Codec reset register address 00h is mapped to C000 0F00h.

CHAPTER 23

I^2S CONTROLLER

23. I2S CONTROLLER

23.1 OVERVIEW

The I2S controller controls the serial interface I2S LINK for 16-bit stereo audio in/out.

FEATURES

- Supports 8kHz to 48kHz sampling frequency
- 16-bit audio in/out
- Supports normal I2S and MSB-Justified I2S format

Audio data transfer is executed through DMA(max 2 channels).

23.2 PIN DESCRIPTION

There are five signals connected to external I2S Codec.

Name	Direction	Description
SYSCLK	O	SYSCLK = BITCLK x 4 = SYNC x 256. Generated by PWRMAN used by codec only
BITCLK	O	bit-rate clock=SYNCx64. Generated by PWRMAN and used by both controller and codec
I2S_SYNC	O	Left/Right audio data identifier
I2SDATA_OUT	O	Serial audio output data
I2SDATA_IN	I	Serial audio input data

TABLE 23-1. PIN DESCRIPTION

23.3 I2S CONTROLLER OPERATION

Processor can access I2S controller register directly. Audio data transfer by DMA.

23.3.1 Initialization

Prior to activating the I2S controller, the GPIO is to be configured properly. I2S uses GPIOL[10:6] 5 pins. These pins are configured as GPIO AltFunction2 for I2S audio in/out function. The GPIO setting steps are as follows:

1) Set GPIOL AltFNSelL register (C000 1036h) as 1111_xxxx_ xxxx_xxxxb
2) Set GPIOL AltFnSelH register (C000 1056h) as xxxx_xxxx_xx11_1111b

In order to activate all clocks used by the controller and codec, bit 1 of ASCLKENREG (C000 090Ch) of PWRMAN must be enabled. If this bit is set to 1, the Peripheral bus clock for I^2S controller(PCLK_ I^2S), the it rate clock(BITCLK), and the system clock used by codec(SYSCLK) are activated.

1) PCLK_ I^2S : peripheral bus clock for I^2S controller
2) BITCLK : bit rate clock for controller and codec
3) SYSCLK : system clock for codec

When the global reset signal is 0 or bit 0 of I^2S _CTRL_REG(I^2S on bit) is 0, the I^2S controller is initialized and is in an inactive state. After the I^2S ON bit becomes 1, the I^2S controller is enabled and control registers are accessible by the host CPU. The I^2S audio in/out function is enabled after both the I^2S ON bit and I^2S LINK enable bit (bit 1 of I^2S _CTRL_REG) are 1.

Before enabling I^2S LINK, the operation mode must be selected. Possible modes are I^2S mode and MSB-justified mode. Bit 0 of I^2S _CONFIG_REG represents the operation mode of I^2S.

I^2S Control Register (I^2S _CTRL_REG)

Address : C000 4400h

This register controls common I^2S functions.

Bit	R/W	Symbol	Description	Reset Value
1	RW	**I^2S _LINK**	I^2S LINK enable 0 = disable I^2S LINK, 1 = enable I^2S LINK	0b
0	RW	**I^2S _ON**	I^2S On 0 = I^2S off and initialize I^2S controller, 1 = I^2S on If this bit is 0, the following is occurred: -. disables I^2S LINK activity. -. resets transmit and receive FIFO. - .De-asserts all DMA requests. -. disables all interrupts. -. initialize configuration register.	0b

TABLE 23-2. I^2S CONTROL REGISTER

I²S Configuration Register (I²S _CONFIG_REG)

Address : C000 4402h

This register controls I²S operation modes.

Bit	R/W	Symbol	Description	Reset Value
3	RW	**LOOP_BACK**	Loop back enable 0 = disable loop back operation. 1 = enable loop back operation. audio input directly to output.	0b
2	RW	**PLAY**	Play enable 0 = disable audio data output to external codec. 1 = enable audio data output to external codec.	0b
1	RW	**RECORD**	Record enable 0 = disable recording audio data from external codec. 1 = enable recording audio data from external codec. record enable bit must be set to 1 in loop back operation.	0b
0	RW	**LINK_MODE**	I²S LINK mode 0 = I²S mode. Valid audio data starts after 1 clock cycle of SYNC transition. 1 = MSB-Justified mode. Valid audio data starts simultaneously with SYNC transition.	0b

TABLE 23-3. I²S CONFIGURATION REGISTER

I²S Status Enable Register (I²S _STA_ENA_REG)

Address : C000 4404h

This register controls whether the occurrence of certain condition will cause setting of the status register.

Bit	R/W	Symbol	Description	Reset Value
1	RW	**IN_OVR_EN**	Input FIFO overrun status enable 0 = Input FIFO overrun status disabled. Status bit will be 0 without regard to FIFO condition. 1 = Input FIFO overrun status enabled. Status bit will be set to 1 if this condition occurs. Also, an interrupt is issued. This interrupt can be masked by INTC. Refer to INTC mask register.	0b
0	RW	**OUT_UDR_EN**	Output FIFO underrun status enable 0 = Output FIFO underrun status disabled. Status bit will be 0 without regard to FIFO condition. 1 = Output FIFO underrun status enabled. Status bit will be set to 1 if this condition occurs. Also, an interrupt is issued. This interrupt can be masked by INTC. Refer to INTC mask register.	0b

TABLE 23-4. I²S STATUS ENABLE REGISTER

I2S Status Register (I2S _STATUS_REG)

Address : C000 4406h

Bit	R/W	Symbol	Description	Reset Value
2	RW	**LINK_BUSY**	I2S LINK busy status. 0 = I2S LINK is not busy 1 = I2S LINK is busy (data transmit or receive in progress)	0b
1	RW	**IN_OVR**	Input FIFO over run status 0 = normal state 1 = Input FIFO overrun occurred.	0b
0	RW	**OUT_UDR**	Output FIFO under run status 0 = normal state 1 = Output FIFO underrun occurred.	0b

The Bits of the Status Register are cleared by software writing 1 to each bit.

TABLE 23-5. I2S STATUS REGISTER

23.3.2 Clocks and Sampling Frequencies

The BITCLK is the rate at which audio data bits enter or leave the I2S LINK. The SYSCLK is required by the codec to run delta sigma ADC operations.

BITCLK and SYSCLK are supplied by internal PLL and configured as output pins. By setting AUDICSETREG (C000 0922h), different sampling frequencies 8 kHz to 48 kHz are supported (refer to PWRMAN).

23.3.3 Buffers

The I2S controller has 2 buffers :

1) PCM Out buffer : 16 x 16-bit
2) PCM In buffer : 16 x 16-bit

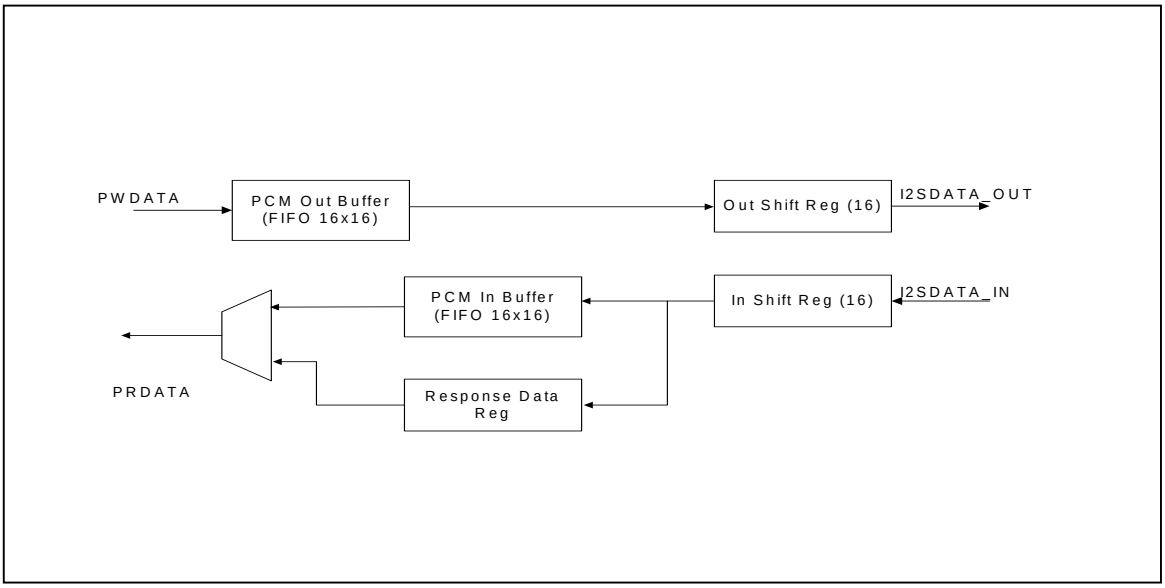


Figure 23-1. I²S Buffer Block Diagram

The audio data buffers are controlled as double buffers. That is, if the output buffer has less than or equal to 8 words of data, the output DMA request is triggered by the controller, and if the input buffer has more than or equal to 8 words of data, the input DMA request is triggered.

23.3.4 Valid Data Structure

Valid audio data structures are as follows:

1) 32 bit word mode

   MS half word = right channel data

   LS half word = left channel data

MS half word (right)	LS half word (left)

In this case, the DMA channel being used is to be configured as follows:

a) Output DMA channel

   Increment source address; source and target data format is word.

b) Input DMA channel

   Increment target address; source and target data format is word.

2) 16 bit half word mode

first word = left channel data (MS, LS are both available)

second word = right channel data (MS, LS are both available)

not used	first word (left)
not used	second word (right)

In this case, the DMA channel being used is to be configured as follows:

a) output DMA channel

Increment source address; source and target data format is LS(MS) half word.

b) input DMA channel

Increment target address; source and target data format is LS(MS) half word.

In many audio applications such as MP3 play or MPEG audio play, audio data is generated by channels. After a certain amount of left channel data is written to memory, the same amount of right channel data is written, and so on. The valid data structure above is achieved by proper setting of the memory address increment value and memory format when decoded audio data is written to memory.

For word-by-word case 2) above, address increment value is 2 for each audio channel and memory format is word. For single word mode 1) above, the address increment value is 1 and memory format is LS(MS) half word.

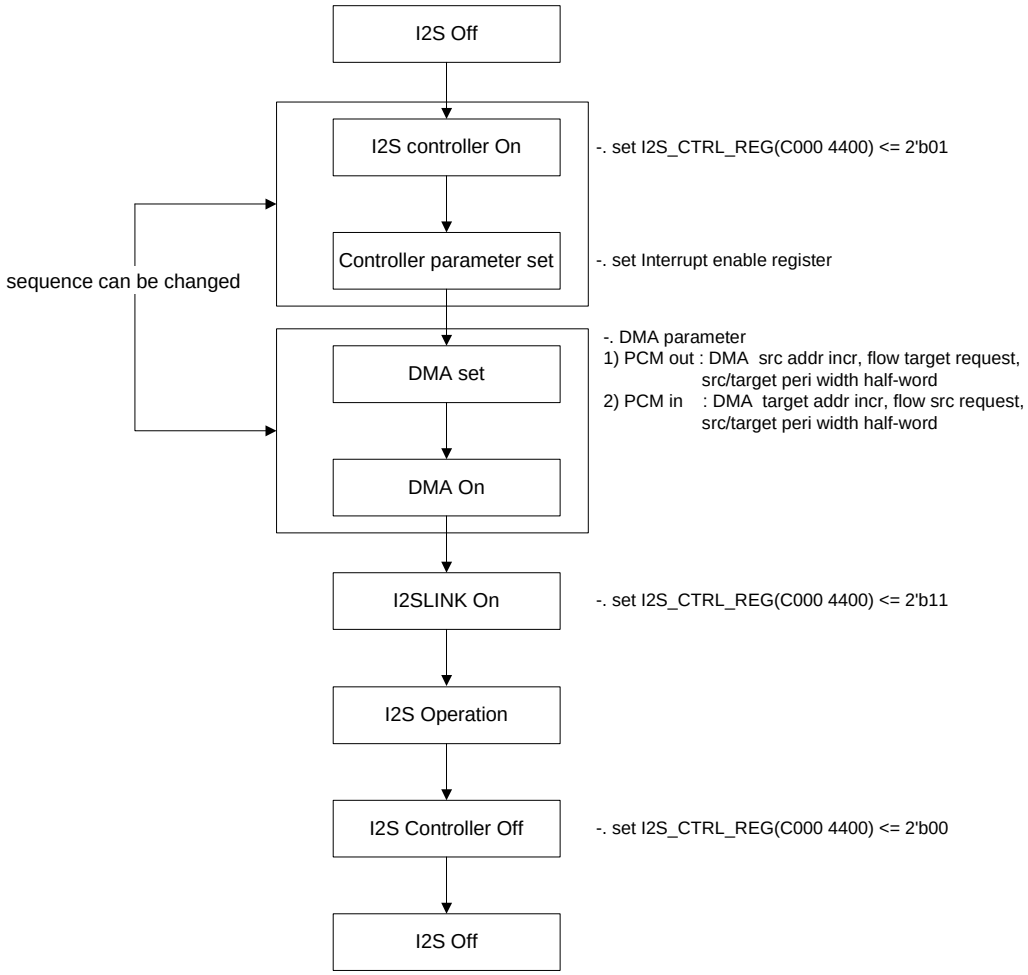
23.3.5 Operation Flow

The I^2S controller starts operation after the reset signal is no longer being sent. Before activating the I^2S LINK interface for transmitting and receiving audio data with codec, the DMA parameter must be configured properly.

If I^2S LINK is activated and the connected codec is ready, the controller and codec can transfer audio data via I^2S LINK. The controller uses max 2 DMA channels, each corresponding to PCM Out and PCM In audio data.

When the processor activates I^2S LINK by setting I^2S _CTRL_REG to 11b, the controller starts generating the I^2S SYNC signal. Following are the functional steps for I^2S:

The sequence of DMA parameter setting and I^2S controller setting can be changed.


I2S Off
I2S controller On
-. set I2S_CTRL_REG(C000 4400) <= 2'b01
Controller parameter set
-. set Interrupt enable register
sequence can be changed
DMA set
-. DMA parameter
1) PCM out : DMA src addr incr, flow target request, src/target peri width half-word
2) PCM in : DMA target addr incr, flow src request, src/target peri width half-word
DMA On
I2SLINK On
-. set I2S_CTRL_REG(C000 4400) <= 2'b11
I2S Operation
I2S Controller Off
-. set I2S_CTRL_REG(C000 4400) <= 2'b00
I2S Off

23.4 I2S CONTROLLER REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
I2S Control Register (I2S _CTRL_REG) ***Address : C000 4400h***				
1	RW	**I2S _LINK**	I2S LINK enable	0b
0	RW	**I2S _ON**	I2S On	0b
I2S Config Register (I2S _CONFIG_REG) ***Address : C000 4402h***				
3	RW	**LOOP_BACK**	Loop back enable	0b
2	RW	**PLAY**	Play enable	0b
1	RW	**RECORD**	Record enable	0b
0	RW	**LINK_MODE**	I2S LINK mode	0b
I2S Status Enable Register (I2S _STA_ENA_REG) ***Address : C000 4404h***				
1	RW	**IN_OVR_EN**	Input FIFO over run status enable	0b
0	RW	**OUT_UDR_EN**	Output FIFO under run status enable	0b
I2S Status Register (I2S _STATUS_REG) ***Address : C000 4406h***				
2	RW	**LINK_BUSY**	I2S LINK busy status	0b
1	RW	**IN_OVR**	Input FIFO over run status	0b
0	RW	**OUT_UDR**	Output FIFO under run status	0b

TABLE 23-6. I2S CONTROLLER REGISTER LIST

CHAPTER 24

SSP/SPI

24. SSP/SPI

24.1 OVERVIEW

The SSP/SPI is a full-duplex synchronous serial interface. It supports Synchronous Serial Protocol(SSP) and Serial Peripheral Interface(SPI) protocol. It can connect to a variety of external converters, serial memory, and many other devices which use serial protocols for transferring data.

There are 4 I/O pin signals associated with SSP/SPI transfers: the SSPCLK, the SSPRXD data receive line, the SSPTXD data transfer line, and SSPFRM (Frame Indicator in SSP mode, Chip Select in SPI mode).

FEATURES

- SPI Protocol, SSP Protocol compatible
- 16-bit Shift Register for transmit
- 16-bit Shift Register for receive
- 5-bit Pre-scale counter
- Polling, Interrupt, and DMA transfer mode

BLOCK DIAGRAM

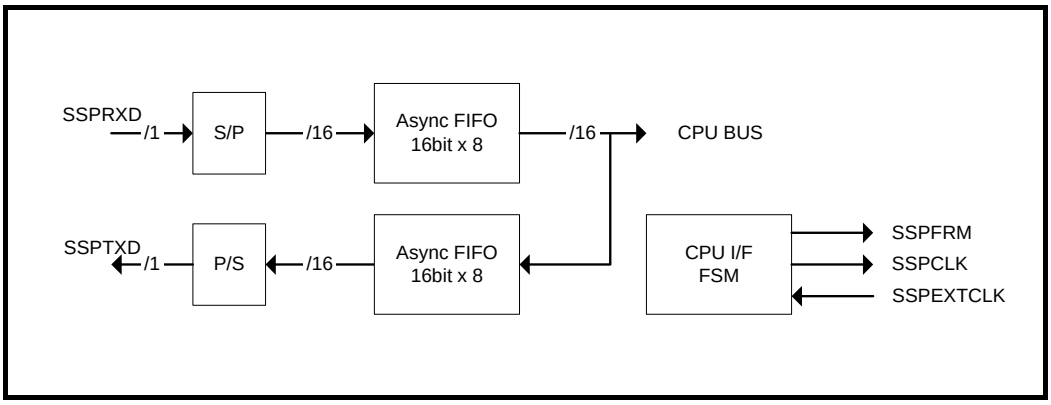


Figure 24-1. SSP/SPI Block Diagram

24.2 PIN DESCRIPTION

The Pins for the communication between the SSP/SPI Block and external peripherals are listed in the following table. These pins are used as the GPIO or other Alternative functions.

Name	Direction	Description
SSPCLK	O	Serial Bit Clock (SSPCLK) provides a clock signal to external devices for synchronizing the transferred Serial Data.
SSPFRM	O	Notify the start and end of Serial Data.
SSPRXD	I	Use to receive Data from external devices.
SSPTXD	O	Use to send Data to external devices.

TABLE 24-1. PIN DESCRIPTION

24.3 OPERATION

The SSI/SPI Block transfers Serial Data from/to external devices via FIFO in the SSP/SPI Block. The transfer operation is initiated by CPU, using the programmed I/O system or the DMA, to/from the system memory. The SSI/SPI Data transfer is performed in full duplex.

When the SSI/SPI sends Data to the PIO Mode, the transfer operation is completed by Reading 'Read FIFO' or Writing to 'Write FIFO' by means of a program.

In the case of communication with DMA Mode,- In DMA transfer mode, the DMAENB bit in the DMA and the SSPSPICONT0 bit are set to 1 to enable the DMA transfer

For Data reception using the SSI/SPI Block, the Read operation is automatically performed until FIFO is be FULL by writing one Data to TX FIFO. If the RXONLY bit is cleared, the Read operation is performed as many times as Data was written to TX FIFO.

Signal waveforms by SSP Mode and SPI Mode are as shown below.

24.3.1 SPI Mode

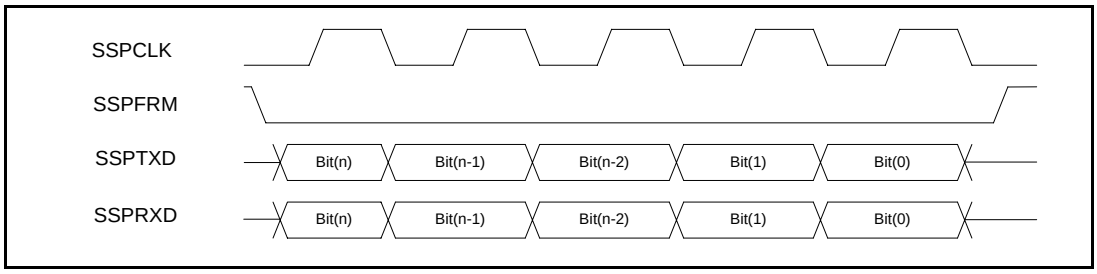


Figure 24-2. SPI Mode Signal

To enable the data transfer mode, SSPFRM signal is required to be low when SSPCLK is on the rising edge. The MSB of stored data will be transferred first. MSB Data bits out are output first. The input of the Data read is performed in a similar way.

The Polarity and Phase of SSPCLK can be converted by the use of a programming.

24.3.2 SSP Mode

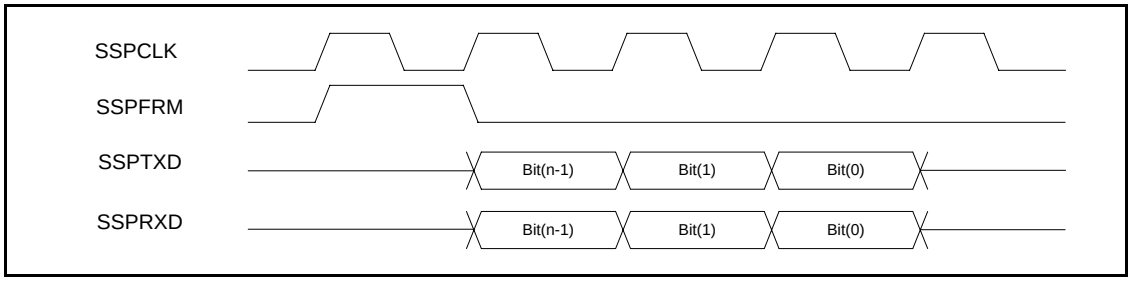


FIGURE 24-3. SSP MODE SIGNAL

When Data output is ready in the SSP Block, the SSPFRM is out for 1 Clock. In the next clock, the Data is out via the SSD TXD. The MSB out of the Data bit is output first. The input of the Data read is performed in a similar way. The Word length can be determined by the SSPSPICONT 0 Register.

The Polarity and Phase are converted by the use of a programming.

24.4 SSP/SPI CONTROLLER REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
SSP/SPI Control Register0 (SSPSPICONT0) ***Address : C000 3F00h***				
[4:0]	R/W	**DIVCNT**	Set internal clock divide value. Value should be bigger than 0 ex) DIVCNT=1 : 2devide DIVCNT=2 : 3devide	2
[8:5]	R/W	**NUMBIT**	Set Bit width of Data. (n+1)bit, MAX 16bit	7
[9]	R/W	**EXTCLKSEL**	Use External Clock 0 : Internal Clock (3.6864Mhz) 1 : I_SSPEXTCLK.	0
[10]	R/W	**FFCLR**	Initialize internal FIFO. It should toggle once initially 0 : IDLE 1 : RESET	0
[11]	R/W	**ENB**	SPI/SPP Enable 0 : Disable 1 : Enable	0
[12]	R/W	**DMAENB**	Set SIO Mode. 0 : PIO Mode 1 : DMA Mode	0
[13]	R/W	**RXONLY**	Set SIO Mode Writing data to Tx Buffer, automatically transfer until Rx FIFO Full. To stop transfer Reset FFCLR.Will stop after finishing current access. 0 : Read When Writing 1 : Read Only	0
[14]	R/W	**ZENB**	Make TXD Pin Hi-Z status 0 : Always 1 : Only When Transmitting	1
[15]	R	**Reserved**	-	-
SSP/SPI Control Register1 (SSPSPICONT1) ***Address : C000 3F02h***				
[1:0]	R/W	**TYPE**	Set SIO Mode 00 : SSP 01 : SPI 1x: Reserved	X
[2]	R/W	**SCLKSH**	Set Phase of External out SSPCLK 0 : 90degrees 1 : 0degrees	X
[3]	R/W	**SCLKPOL**	Set Polarity of External out SSPCLK 0 : Inverting 1 : Normal	X
[15:4]	R	**Reserved**	-	-
SSP/SPI Data Register (SSPSPIDATA) ***Address : C000 3F04h***				
[7:0]	R/W	**DATA**	Data to be transmitted when write. Read transmitted data when Read	X
[15:0]	R	**Reserved**	**-**	-
SSP/SPI Status Register (SSPSPISTAT) ***Address : C000 3F06h***				
[0]	R	**RFFEMPTY**	Set 1 when receiving buffer empty	X

Bit	R/W	Symbol	Description	Reset Value
[1]	R	**RFFFULL**	Set 1 when receiving buffer Full	X
[2]	R	**WFFEMPTY**	Set 1 when transmit buffer empty	X
[3]	R	**WFFFULL**	Set 1 when transmit buffer full	X
[4]	R/W	**IRQR**	Generate interrupt when transmit buffer is full. To clear, write '1'	0
[5]	R/W	**IRQW**	Generate interrupt when receiving buffer is empty. To clear, write '1'	0
[6]	R/W	**IRQE**	Generate interrupt when each Rx/Tx finished	0
[12:7]	R	**Reserved**	-	-
[13]	R/W	**IRQRENB**	IRQR Enable Register 0 : Disable 1 : Enable	0
[14]	R/W	**IRQWENB**	IRQW Enable Register 0 : Disable 1 : Enable	0
[15]	R/W	**IRQEENB**	IRQE Enable Register 0 : Disable 1 : Enable	X

TABLE 24-2. SSP/SPI CONTROLLER REGISTERS LIST

CHAPTER 25

TRANSPORT STEAM INTERFACE (MPEG I/F)

25. TRANSPORT STREAM INTERFACE (MPEG I/F)

25.1 OVERVIEW

The MPEG I/F block receives the output of the MPEG transport decoder chip and then Store the transmitted data the Main Memory using the FastDMA of the MP2520F.

This block supports with 8-bit Parallel and 1-bit Serial Modes, and maximum programmable Packet size is 256 bytes.

FEATURES

- Programmable Packet Size
- Support 8-bit Parallel and 1-bit Serial Mode

BLOCK DIAGRAM

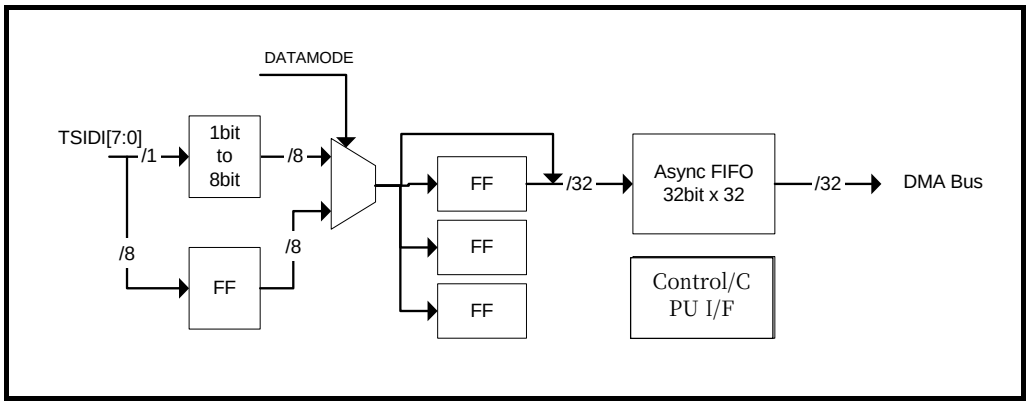


Figure 25-1. Transport Stream I/F Block Diagram

TRANSPORT SUBSYSTEM INTERFACE DIAGRAM

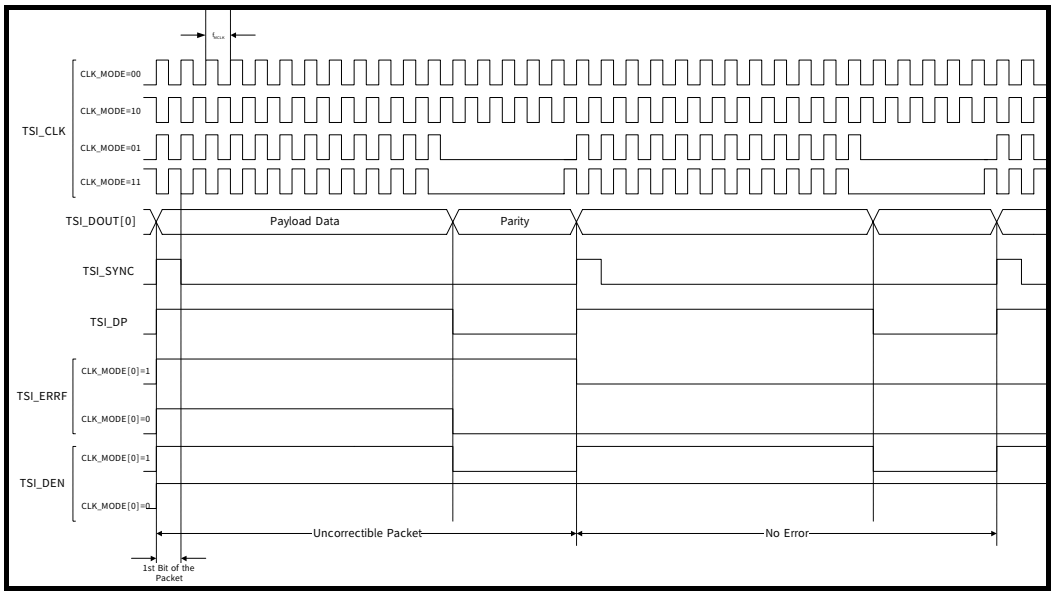


Figure 25-2. In Serial Mode

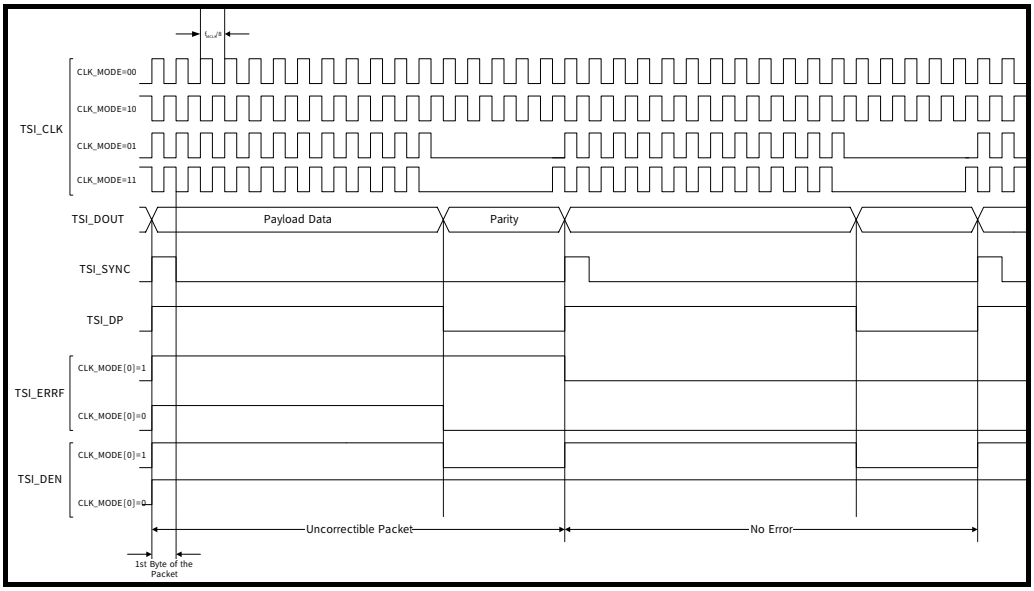


Figure 25-3. In Parallel Mode

25.2 PIN DESCRIPTION

I/O Signals	Description
TSICLK	(INPUT) Clock
TSISYNC	(INPUT) SYNC, This is used as the Packet Start Signal.
TSIDP	(INPUT) Data/Parity Signal 1: Data 0: Parity
TSIERR	(INPUT) Error flag. Set in case of uncorrectable packet by MPEG Transport Decoder.
TSIDI[7:0]	(INPUT) 8-bit Data Bus. When in Serial mode, TSIDI[0] is used as the data input pin.

TABLE 25-1. PIN DESCRIPTION

25.3 OPERATION

Before the transmission of Data, the MPEG transport decoder's Data format, either Parallel or Serial transmission mode to be entered must be determined and MP2520F's DATAMODE bit is set to corresponding mode. The effective Byte Size for one Packet is defined by the WORDCNT.

If the ENB Bit is set to '1', the transmission is initiated. The transmitted Data is stored in the Main Memory via the MP2520's internal FastDMA.

Whenever one packet is transmitted, an interrupt can be produced by setting the IRQPend Bit. If an interrupt is produced, the ERRFLAG is referred to in order to check if an Error exists in the transmitted Packet.

25.4 TRANSPORT STREAM I/F REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
Transport Stream I/F Control Register (MPEGIFCONT) ***Address : 0xC000 3C00***				
[5:0]	R/W	**WORDCNT**	Sets the number of transmitting 32-bit Word between SYNCs. Generates Interrupt after finishing assigned number of transmits in this register.	3
[6]	R/W	**ENB**	MPEG-IF Enable 0 : Disable 1 : Enable	0
[7]	R/W	**DATAMODE**	Data format 0 : 8-bit Mode 1 : 1-bit Serial Mode	0
[13:8]	R	**Reserved**	-	-
[14]	R	**ERRFLAG**	Indicates current Packet status 0 : No Error 1 : Error Checks error status by checking ERRFLAG bit after finishing transmit.	X
[15]	R/W	**IRQPend**	Read One Frame [Read] 0 : No Interrupt 1 : Pending Interrupt [Write] 1 : Clear Interrupt Pending Register	X

TABLE 25-2. TRANSPORT STREAM I/F REGISTERS LIST

CHAPTER 26

ADC & TPC
(TOUCH PANEL CONTROLLER)

26. ADC & TPC (TOUCH PANEL CONTROLLER)

26.1 OVERVIEW

The Touch Panel Controller (TCP) controls the switch, comparator, and ADC to read the X, Y, position of the Touch Panel touched. It also reads the data from any ADC Channel. All data is transmitted into external memory using the DMA. Refer to Figure 26-1.

FEATURES:

The TPC module offers the following features:

- 10-bit ADC for touch panel and voltage detection
- On-chip voltage reference for ADC
- 16x16-bit FIFO for X, Y, Z, U1 and U2
- Embedded touch panel circuitry (Switch and Comparator)
- Supports auto, manual, and Touched Detection Enable Mode (TDEM)
- Programmable pen down and pen-up interrupt to interrupt handler
- Provides data-ready and FIFO-full interrupts

BLOCK DIAGRAM

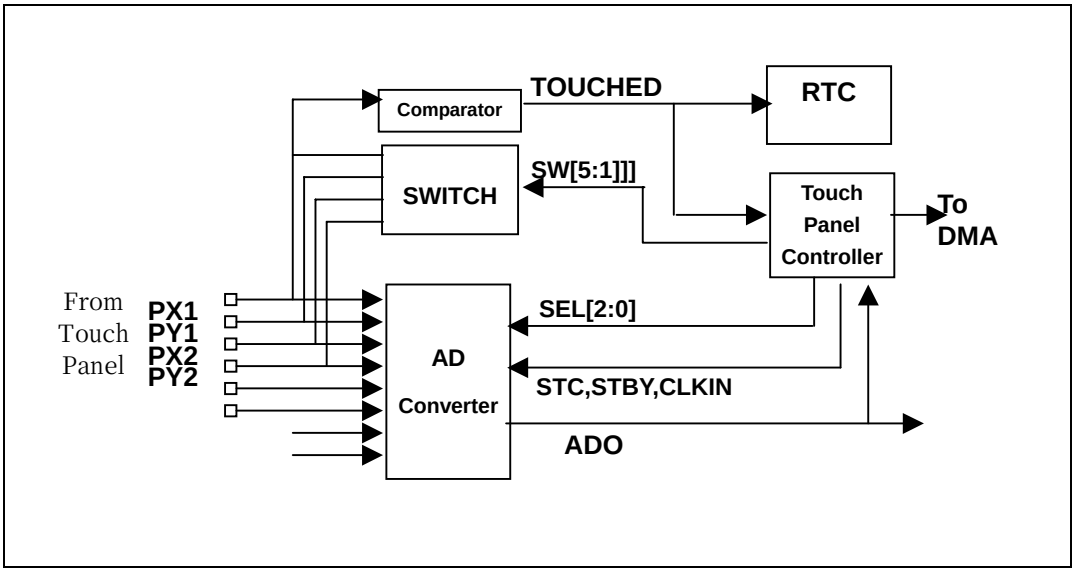


Figure 26-1. TPC System Block Diagram

This block consists of three analog blocks and one control block.

The Comparator detects pen down. The switch creates the bias required for TOUCH PAD when it reads each coordinate. The AD Converter (ADC) converts analog signals entered through a PAD into digital signals. Finally, the TPC (Touch Panel Controller) controls the analog blocks and transfers the data attained from the ADC to the outside through the DMA.

26.2 OPERATION

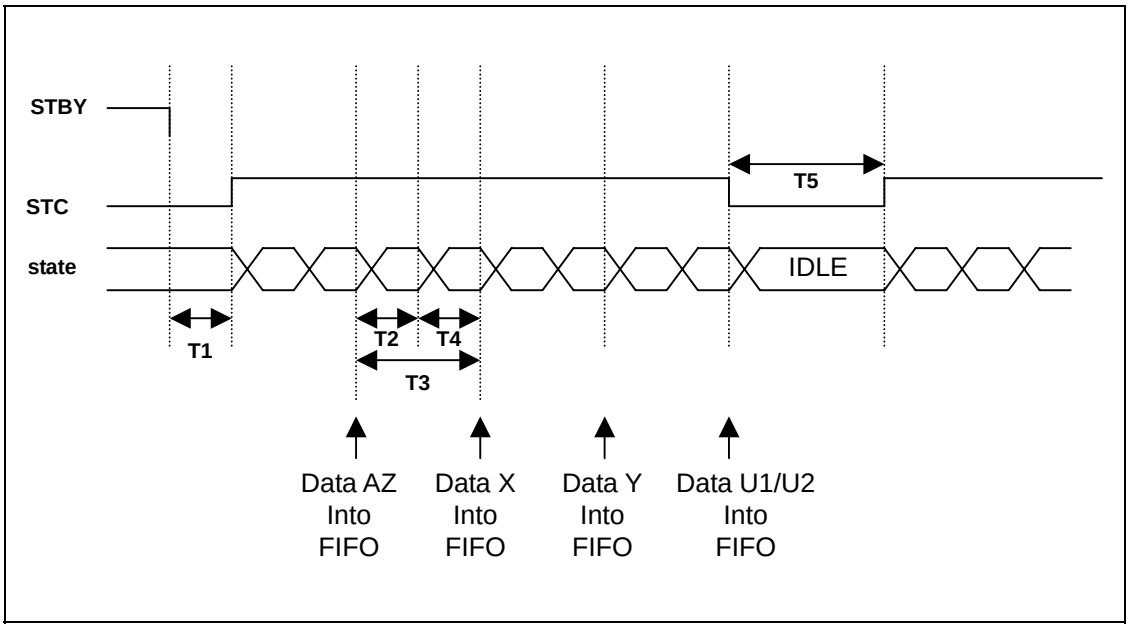


Figure 26-2. Pen Input Sampling Time

26.2.1 CLOCK CONTROL

The clock uses the PCLK. In addition, the ADC uses the clock divided through the Prescaler. The frequency can be divided from a minimum of two times to a maximum of 256 times. The APSV in Table 26-1 determines the division of the clock. When the PADE in Table 26-2 is set to '1' and the APSY is set to 'non-0', the clock occurs.

Address : TP_BASE + 0x05

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**TPSNS**	Touched Input Sensitivity	0
[7:0]	R/W	**APSV**	Prescaler Value	0

TABLE 26-1. CLOCK CONTROL REGISTER(TPC_CLK_CNTL)

Address : TP_BASE + 0x00

Bit	R/W	Symbol	Description	Reset Value
[15]	R/W	**ADCEN**	AD Converter Enable	
[14]	R/W	**PADE**	Touch Panel Enable	0b
'[13]	R/W	**AUTO**	AUTO Mode Enable	0b
[12]	R/W	**U1E**	U1 Channel Enable	0b
[11]	R/W	**U2E**	U2 Channel Enable	0b
[10]	R/W	**MOD**	Touch Panel Enable	0b
[9]	R/W	**AZE**	Auto-ZERO Enable	0b
[8:7]	R	**Reserved**	-	000b
[6]	R/W	**COMPD**	Comparator Power Down Mode	1'b1
[5]	R/W	**TDEM**	Touch Detection Enable Mode	0b
[4]	R/W	**FIFOCLR**	FIFO Clear	0bj
[3]	R	**TOUCHED**	Touched Status	0b
[2]	R	**FIFOFULL**	FIFO Full Status	0b
[1]	R	**FIFOEMPTY**	FIFO Empty Status	0b
[0]	R	**STBY**	ADC Status	0b

TABLE 26-2. CONTROL REGISTER(TPC_CNTL)

26.2.2 SAMPLING RATE CONTROL

A Data Sampling Rate is determined by the parameter to control the ADC. As shown in figure 26-2, four parameters (T1, T2, T4 and T5) are used to control the ADC Sampling Rate. These parameters are listed in Table 26-3.

Register	Parameter	Description	Min/Max
BGCNT	T1	Bandgap warm up time	0/255
DSCNT	T2	Transistor switching and input selecting set up time	0/255
DMCNT	T4	The Decimation ratio of the second-state FIR	4/255
IDLECNT	T5	The number of clocks between the last capture and the first capture of two pen input points	0/255

TABLE 26-3. SAMPLING RATE CONTROL PARAMETERS

T2 and T4 out of the above parameters determine the time required for the sampling of each data. The T2 (DSCNT) indicates the required time to switch the ADC analog channel. In addition, the T4 indicates the required time to convert analog signals after sampling into digital signals. The ADC of the MP2520F needs 5 cycles to convert analog signals into digital signals: the minimum value of the DMCNT must be 4.

The Registers to specify these parameters are listed in Table 26-4 and 26-5.

Address : TP_BASE + 0x07

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**DMCNT**	The decimation ratio of the second-stage FIR (DSCNT>=1)	0
[7:0]	R/W	**DSCNT**	The input signal data set up time after transistor switching circuit and input select are settled	0

TABLE 26-4. TIMING PARAMETER REGISTER 1(TPC_TIME_PARM1)

Address : TP_BASE + 0x08

Bit	R/W	Symbol	Description	Reset Value
[15:8]	R/W	**BGCNT**	Bandgap warm up time	0
[7:0]	R/W	**IDLECNT**	The number of clocks between the last capture and the first capture of two pen input points	0

TABLE 26-5. TIMING PARAMETER REGISTER 2(TPC_TIME_PARM2)

The Sampling rate to read X and Y coordinates from the Touch PAD is determined by the number of the selected channels, the DILECNT, the DSCNT, and the DMCNT. Table 26-4 shows the way to determine the sampling frequency according to the data types filled in FIFO. The FIFO is always filled with data in order of AZ, X, Y, U1 and U2.

The # of Data Type	Equation	FIFO Data Format
5	FCLK/[5x(DSCNT+DMCNT+1)+IDLECNT]	AZ, X, Y, U1, U2,...
4	FCLK/[4x(DSCNT+DMCNT+1)+IDLECNT]	AZ, X, Y, U1,.. or AZ, X, Y, U2,...
3	FCLK/[3x(DSCNT+DMCNT+1)+IDLECNT]	AZ, X, Y, AZ, X, Y,... or X, Y, U1,.. or X, Y, U2,...
2	FCLK/[2x(DSCNT+DMCNT+1)+IDLECNT]	X, Y, X, Y,... or U1, U2, U1, U2,...
1	FCLK/[(DSCNT+DMCNT+1)+IDLECNT]	U1, U1,... or U2, U2,...

TABLE 26-6. SAMPLING RATE CALCULATION

26.2.3 MANUAL MODE

PADE	AUTO	TDEM	U1E	U2E	MOD	AZE	Operation
0	X	X	X	X	X	X	No Valid Data
1	0	X	0	0	0	X	No Valid Data
			0	0	1	0	Read X, Y
			0	0	1	1	Read X, Y, AZ
			1	0	1	0	Read X, Y, U1
			1	0	1	1	Read X, Y, AZ, U1
			0	1	1	0	Read X, Y, U2
			0	1	1	1	Read X, Y, AZ, U2
			1	1	1	0	Read X, Y, U1, U2
			1	0	0	x	Read U1
			0	1	0	x	Read U2
			1	1	0	x	Read U1, U2

TABLE 26-7. MANUAL MODE OPERATION

When the AUTO in Table 26-2 is set to '0', Manual Mode is executed. In addition, when the PADE and the ADCEN is set to '1', Sampling is initiated. The sampling proceeds in order of AZ, X, Y, U1 and U2 channels, and the channel to read is selected by the values of U1E, U2E, MOD and AZE.

Transformed data are stored in the TP_X_VALUE, TP_Y_VALUE, TP_AZ_VALUE, TP_U1_VALUE and TP_U2_VALUE registers. In order to complete the sampling, the STBY value in Table 26-2 must be '1'.
Table 26-7 shows the operation according to register values in Manual Mode.

After reading he transformed data, PADE, U1 and U2 must be set to '0' to read data again.

The registers to store the transformed values are listed in Table 26-8 to Table 26-12.

Address : TP_BASE + 0x0a

Bit	R/W	Symbol	Description	Reset Value
[15:11]	R/W	**READ_X**	Switch Control for Read X	5'h5
[10]	R	**Reserved**	-	-
[9:0]	R	**X_VALUE**	X value	0

TABLE 26-8. X VALUE REGISTER(TPC_X_VALUE)

Address : TP_BASE + 0x0b

Bit	R/W	Symbol	Description	Reset Value
[15:11]	R/W	**READ_Y**	Switch Control for Read Y	5'ha
[10]	R	**Reserved**	-	-
[9:0]	R	**Y_VALUE**	Y value	0

TABLE 26-9. Y VALUE REGISTER(TPC_Y_VALUE)

Address : TP_BASE + 0x0c

Bit	R/W	Symbol	Description	Reset Value
[15:11]	R/W	**AUTO_ZERO**	Switch Control for Read Auto-zero	5'h5
[10]	R	**Reserved**	-	-
[9:0]	R	**AZ_VALUE**	Auto-zero value	0

TABLE 26-10. AUTO ZERO VALUE REGISTER(TPC_Y_VALUE)

Address : TP_BASE + 0x0d

Bit	R/W	Symbol	Description	Reset Value
[15:11]	R/W	**SW_DFALT**	Switch Control for Read U1,	5'h04
[10]	R	**Reserved**	-	-
[9:0]	R	**U1_VALUE**	U1 value	0

TABLE 26-11. U1 VALUE REGISTER(TPC_U1_VALUE)

Address : TP_BASE + 0x0e

Bit	R/W	Symbol	Description	Reset Value
[15:10]	R	**Reserved**	-	-
[9:0]	R	**U2_VALUE**	U2 value	0

TABLE 26-12. U2 VALUE REGISTER(TPC_U2_VALUE)

26.2.4 AUTO MODE

PADE	AUTO	TDEM	U1E	U2E	MOD	AZE	Data Format FIFO
0	X	X	X	X	X	X	No Valid Data
1	1	0	0	0	0	X	No Valid Data
			0	0	1	0	X, Y, X, Y,…
			0	0	1	1	AZ[1], X[2], Y[3], AZX, Y,…
			1	0	1	0	X, Y, U1, X, Y, U1,…
			1	0	1	1	AZ, X, Y, U1, AZ, X, Y, U1,…
			0	1	1	0	X, Y, U2, X, Y, U2,…
			0	1	1	1	AZ, X, Y, U2, AZ, X, Y, U2,…
			1	1	1	0	AZ, X, Y, U1U2,…
			1	0	0	x	U1, U1, U1,…
			0	1	0	x	U2, U2, U2,…
			1	1	0	x	U1, U2, U1, U2,…

TABLE 26-13. AUTO MODE OPERATION

[1] AZ : Auto Zero Value
[2] X : X Value
[3] Y : Y Value

When the AUTO bit is set to 1, the TPC operates in AUTO mode. In this mode, the sampling operation is carried out continuously, and all sampled data is first stored into FIFO. Whenever FIFO is full, data is transmitted into external memory using the DMA. Data stored in FIFO have information about the sampled channel, and data type (X, Y, AZ, U1 and U2), and sampled data. For more information about data format, refer to Table 26-13 Auto Mode Operation.

26.2.5 SWITCHING CONTROL

The switch block has five switches. Switches are controlled differently for each mode. READ_X, READ_Y, AUTO_ZERO, and SW_DFALT registers contain control information for each mode. For more information, Refer to TABLE.2.8 to 26.11.

Operation	SW[5:1]	Read Channel
READ_X	5'b00101	1/3
READ_Y	5'b01010	0/2
AUTO_Z	5'b00101	0
Default	5'b01000	0
READ_U1	5'b01000	0 ~ 7
READ_U2	5'b01000	0 ~ 7

TABLE 26-14. SWITCH DEFAULT CONTROL

READ_X VALUE

In order to read the data on the X coordinate, set SW1 and SW3 to 'ON' and then read data from channel 1/3.

READ_Y VALUE

In order to read the data on the Y coordinate, set SW2 and SW4 to 'ON' and then read data from channel 0/2.

READ_AZ VALUE

This mode is used to measure the voltage between switches. For example, you may read data from channel 2 after connecting SW1 to SW3 to measure the voltage between both ends of SW2. Likewise, you may read data from channel 3 after connecting SW2 to SW4 to measure the voltage between the both ends of SW3.

READ U1 VALUE

Read data from a channel out of ADC channels.

READ U2 VALUE

Read data from a channel out of ADC channels.

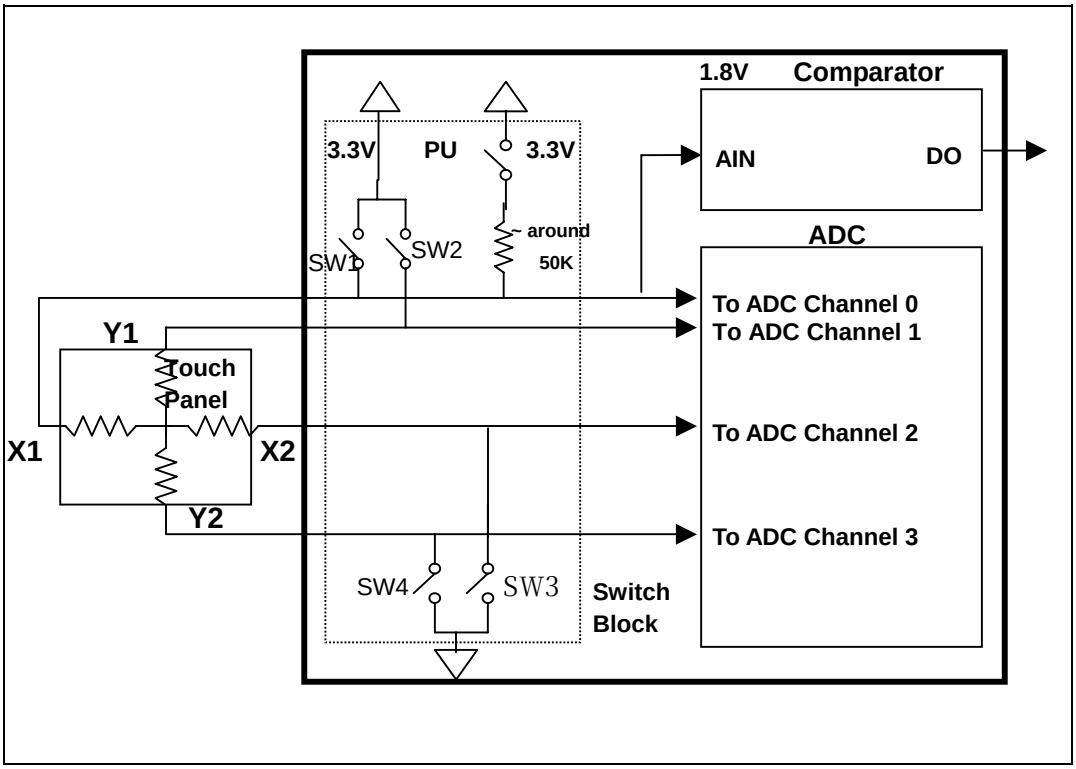


Figure 26-3. Switching Control

26.2.6 INTERRUPT

The TPC has five interrupt sources. Three are for the TOUCH PANEL. The other two sources are for auxiliary input. Each Interrupt is enabled and controlled by the TPC_INTR Register.

1) TOUCH INTERRUPT

The TOUCH Interrupt occurs when the comparator output (TOUCH) signal is toggled from 1 to 0, and the zero state is continued for some period specified by the TPSNS Register. For example, when the TPSNS is zero, an interrupt is generated as soon as it detected by the system clock.

2) TOUCH PANEL COMPARE INTERRUPT

The Touch Panel Compare Interrupt is generated when data sampled is compared to some threshold value that is specified by the TPTHRES Register. The Compare condition is controlled by the TPCC bit.

If TPCC is 0, the interrupt occurs when sampled data is less than TPTHRES, and if TPCC is 1, the interrupt occurs when sampled data is greater than TPTHRES.

3) PEN DATA INTERRUPT

The PEN Data Interrupt occurs when at least one valid data sample is stored in the FIFO.

4) U1 COMPARE INTERRUPT

The U1 compare interrupt is generated when data sampled is compared to some threshold value that is specified by the U1THRES Register. The compare condition is controlled by the U1CC bit.

5) U2 COMPARE INTERRUPT

The U2 Compare Interrupt is generated when data sampled is compared to some threshold value that is specified by the U2THRES Register. The compare condition is controlled by the U2CC bit.

26.2.7 FIFO and Data FORMAT

In the case of non-Manual Mode, all data are stored in the FIFO. In addition, the data are stored in an external memory via the DMA. The data to store in the external memory consist of the source channel of the data and the type of the data as well as the values transformed from analog values. The size of data output from the ADC is 10 bits. This 10-bit data, the ADC channel information, and the data type are stored together in the FIFO. The data formats by the pertinent DATA type are listed in Table 26-15.

ASEL[2]/TOUCHED	ASEL[1:0]	DTYPE[2:0]	ADO[9:0]

TABLE 26-15. DATA FORMAT

ASEL[2:0]: Analog Input Channel.

TOUCHES: The TOUCHED bit is used only when Comparator Output DTYPE is related to a Touch PAD. This bit can be used as the criterion to evaluate the validity of the data entered by the software.

DTYPE	AZ	X	Y	U1	U2
Value	1	2	3	4	5

TABLE 26-16. DATA TYPE

26.3 ADC & TOUCH PANEL CONTROLLER REGISTER LIST

Bit	R/W	Symbol	Description	Reset Value
TOUCH PANEL CONTROL REGISTER (TPC_CNTL) ***Address : TP_BASE + 0x00***				
[15]	R/W	**AD_COV_EN**	AD Converter Enable – Controls the ADC. This bit must be enabled to sample data from the ADC.	
[14]	R/W	**PADE**	Touch Panel Enable – Controls the Touch Panel Controller. This bit must be enable during the sampling. In the manual mode(AUTO==0), this bit must be cleared to read data sampled.	0b
'[13]	R/W	**AUTO_MD**	AUTO Mode Enable – Sets the AUTO mode. When enabled, data sampled is stored in FIFO automatically. When disabled, data sampled is stored into TPC_X_VALUE, TPC_Y_VALUE, TPC_AZ_VALUE, TPC_U1_VALUE and TPC_U2_VALUE for each X, Y, AZ, U1, and U2.	0b
[12]	R/W	**U1_EN**	U1 Channel Enable – Controls the sampling for the U1 channel.	0b
[11]	R/W	**U2_EN**	U2 Channel Enable – Controls the sampling for the U2 channel.	0b
[10]	R/W	**MOD**	Touch Panel Enable – Controls the sampling for the X,Y channels.	0b
[9]	R/W	**AUTO_ZERO**	Auto-ZERO Enable – Controls the sampling for the Auto-Zero(AZ) channel.	0b
[8:7]	R	**Reserved**	-	000b
[6]	R/W	**CO_PW_MD**	Comparator Power-Down Mode – When enabled, the comparator is in power-down mode. In order to detect the TOUCH, this bit must be disabled.	1'b1
[5]	R/W	**TDET_MD**	Touch Detection Enable Mode – This bit is valid when AUTO=1(AUTO Mode). In AUTO Mode, if this bit is enabled, just the sampling for X, Y, and AZ is started when comparator output is active.	0b
[4]	R/W	**FF_CLR**	FIFO Clear – When enabled, FIFO is cleared.	0bj
[3]	R	**TOUCHED**	Touched Status – Reads the comparator output.	0b
[2]	R	**FF_FULL**	FIFO Full Status – Reads the full status of FIFO.	0b
[1]	R	**FF_EMT**	FIFO Empty Status – Reads the empty status of FIFO.	0b
[0]	R	**STBY**	ADC Status – Reads the ADC status. When this bit is set, ADC is busy. When this bit is cleared, ADC is in idle state.	0b

Bit	R/W	Symbol	Description	Reset Value
INTERRUPT CONTROLLER REGISTER (TPC_INTR) ***Address : TP_BASE + 0x01***				
[15:13]	R	**Reserved.**	-	-
[12]	R/RW	**U1CCE**	Compare Interrupt Enable for U1 channel – this bit controls the compare interrupt for the U1 channel.	
[11]	R/RW	**U2_CCE**	Compare Interrupt Enable for U2 channel – this bit controls the compare interrupt for the U2 channel.	
[10:8]	R/W	**TP_INT_EN**	Touch Panel Interrupt Enable [10] : Touch Interrupt – Enable/Disable Touch interrupt signal [9] : Touch Panel Compare Interrupt – Enable/Disable Compare Interrupt for Touch Panel [8] : Pen Data Interrupt. – Enable/Disable Pen Data Interrupt	000b
[7:5]	R	**Reserved**	-	
[4]	R	**U1_IF**	U1 Compare Interrupt Flag – Indicates that compare interrupt is pending for U1 channel	
[3]	R	**U2_IF**	U2 Compare Interrupt Flag - Indicates that compare interrupt is pending for U1 channel	0b
[2:0]	R		Touch Pad Interrupt Flag [2] : Touch interrupt Flag – Indicates the touch interrupt is pending. [1] : Touch Panel Compare Interrupt Flag – Indicates that compare interrupt is pending for the X,Y channels [0] : Pen data Interrupt Flag – Indicates that data interrupt is pending for the X,Y channels	000b
COMPARE REGISTER FOR TOUCH PANEL (TPC_COMP_TP) ***Address : TP_BASE + 0x02***				
[15:11]	R	**Reserved**	-	-
[10]	R/W	**TP_CC**	Touch Panel Compare Control 0 : Trigger when the compare value is greater then the sample 1: Trigger when the sample is greater then the compare value	0b
[9:0]	R/W	**TP_THRES**	Touch Panel Threshold level	0b
COMPARE REGISTER FOR U1 (TPC_COMP_U1) ***Address : TP_BASE + 0x03***				
[15:11]	R	**Reserved**	-	-
[10]	R/W	**U1_CC**	Compare Control for U1 channel 0 : Trigger when the compare value is greater then the sample 1: Trigger when the sample is greater then the compare value.	0b
[9:0]	R/W	**U1_THRES**	U1 Channel Threshold level – Contains the value to be compared with the sampled data in the U1 Channel	128

Bit	R/W	Symbol	Description	Reset Value
COMPARE REGISTER FOR U2 (TPC_COMP_U2) ***Address : TP_BASE + 0x04***				
[15:11]	R	**Reserved**	-	-
[10]	R/W	**U2_CC**	Compare Control for U2 channel 0 : Trigger when the compare value is greater then the sample 1: Trigger when the sample is greater then the compare value	0b
[9:0]	R/W	**U2_THRES**	U2 Channel Threshold level – Contains the value to be compared with the sampled data in the U2 Channel	128
CHANNEL SELECTION REGISTER(TPC_CH_SEL) ***Address : TP_BASE + 0x05***				
[15]	R	**Reserved.**	-	-
[14:12]	R/W	**U2_SEL**	Channel Selection for U2	000b
[11:0]	R/W	**U1_SEL**	Channel Selection for U1	000b
[8:6]	R/W	**Y_SEL**	Channel Selection for Y Read	000b
[5:3]	R/W	**X_SEL**	Channel Selection for X Read	000b
[2:0]	R/W	**AZ_SEL**	Channel Selection for AUTO Zero	000b
CLOCK CONTROL REGISTER (TPC_CLK_CNTL) ***Address : TP_BASE + 0x06***				
[15:8]	R/W	**TP_SNS**	Touched Input Sensitivity – this register sets the sensitivity for the comparator output. It reduce the glitch effect.	0
[7:0]	R/W	**A_PS_VAL**	Prescaler Value – sets the divide ratio for the prescaler When zero, no clock is generated for the ADC. When one, Divider ratio is two. So we can set from fclk/2 to fclk/512	0
TP TIMING PARAMETER REGISTER 1 (TPC_TIME_PARM1) ***Address : TP_BASE + 0x07***				
[15:8]	R/W	**BG_CNT**	Bandgap warm up time (Refer to Figure 27- 2)	0
[7:0]	R/W	**IDLE_CNT**	The number of clocks between the last capture and the first capture of two pen input points	0
TP TIMING PARAMETER REGISTER 2 (TPC_TIME_PARM2) ***Address : TP_BASE + 0x08***				
[15:8]	R/W	**DS_CNT**	The input signal data set up time after transistor switching circuit and input select are settled	0
[7:0]	R/W	DM_CNT	**The decimation ratio of the second-stage FIR (DSCNT>=1)**	0
TP TIMING PARAMETER REGISTER 3 (TPC_TIME_PARM3) ***Address : TP_BASE + 0x09***				

Bit	R/W	Symbol	Description	Reset Value
[15:4]	R	**Reserved**	-	0
[3:0]	R/W	**ADC_TIME**	ADC Conversion Time – setS the cycles needed to convert the data sample. This value must be greater than four. This is generated from the conversion time of ADC embedded	4
X REGISTER (TPC_X_VALUE) ***Address : TP_BASE + 0x0a***				
[15:11]	R/W	**READ_X**	Switch Control for Read X	5'h5
[10]	R	**Reserved**	-	-
[9:0]	R	**X_VALUE**	X value	0
Y REGISTER (TPC_Y_VALUE) ***Address : TP_BASE + 0x0b***				
[15:11]	R/W	**READ_Y**	Switch Control for Read Y	5'ha
[10]	R	**Reserved**	-	-
[9:0]	R	**Y_VALUE**	Y value	0
AZ REGISTER (TPC_AZ_VALUE) ***Address : TP_BASE + 0x0c***				
[15:11]	R/W	**AUTO_ZERO**	Switch Control for Read Auto-zero	5'h5
[10]	R	**Reserved**	-	-
[9:0]	R	**AZ_VALUE**	Auto-zero value	0
U1 REGISTER (TPC_U1_VALUE) ***Address : TP_BASE + 0x0d***				
[15:11]	R/W	**SW_DFALT**	Switch Control for Read U1	5'h04
[10]	R	**Reserved**	-	-
[9:0]	R	**U1_VALUE**	U1 value	0
U2 REGISTER (TPC_U2_VALUE) ***Address : TP_BASE + 0x0e***				
[15:11]	R	**Reserved**	-	-
[10]	R	**Reserved**	-	-
[9:0]	R	**U2_VALUE**	U2 value	0

CHAPTER 27

SD/MMC CONTROLLER

27. SD/MMC CONTROLLER

27.1 OVERVIEW

Multi-Media Card (MMC), Secure Digital (SD) memory card and SDIO device are supported by the SD/MMC controller. MMC specification version 2.11, SD memory card specification version 1.0 and SDIO card specification version 1.0 are appropriate for the SD/MMC controller.

FEATURE

- Compatible with the Multi-Media Card System Specification, version 2.11
- Compatible with the SD Memory Card Specification, version 1.0 and SDIO Card Specification, version 1.0
- Supports clock speeds up to 10 MHz in MMC mode
- Supports clock speeds up to 25 MHz in SD mode
- Contains an Internal Clock Prescaler
- Contains 64 bytes of FIFO for data receive/transmit
- Supports PIO and DMA mode data transfer
- Supports 4-bit data bus

27.2 PIN DESCRIPTION

The external SD/MMC card is connected to three (single data line) or six (4 data line) signals.

Name	Direction	Description
SDICLK	O	SD/MMC Interface Clock - Varies due to clock prescaler
SDICMD	B	SD/MMC Command/Response
SDIDAT[3:0]	B	SD/MMC Data

TABLE 27-1. PIN DESCRIPTION

27.3 SD/MMC CONTROLLER OPERATION

The clock frequency for the transmission of the controller and the device can be adjusted by the clock prescale register (SPIDER) of the SD controller. The samplings of commands and data are synchronized by this clock.

27.3.1 Bus protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- **Command**: A command is an operation starting token. It's sent from the controller to a card, and is transferred serially on the CMD line.
- **Response**: A response is a token that is sent from a card as an answer to a previously received command to the controller, and is transferred serially on the CND line.
- **Data**: Data can be transferred from the controller to the card or vice versa, and it is transferred via the DAT line.

Operation without data token is as follows:

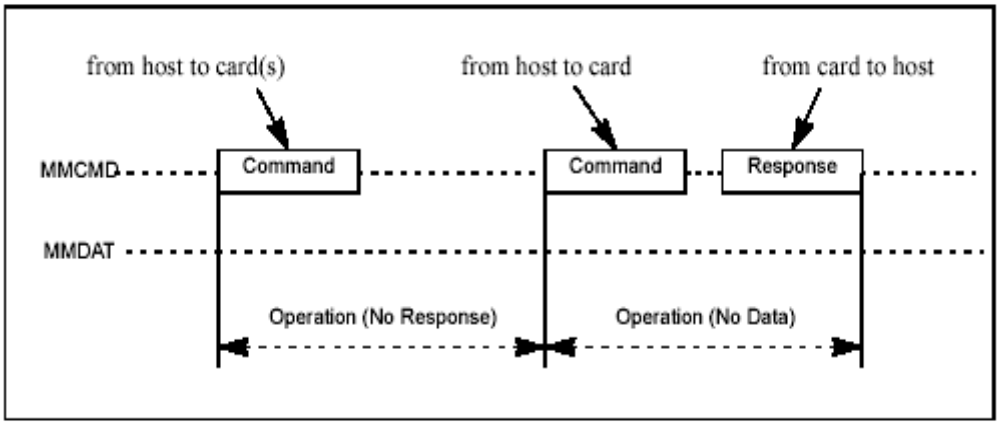


Figure 27-1. Operation Without Data

Data transfers from/to the card are done in block. CRC bits always follow Data blocks. Defines the single and multiple block operations. For faster write operations, the multiple block operation mode is better. The controller terminates a multiple block transmission when a stop command follows on the CMD line. The host can configure data transfer to use single or multiple data lines. The following is the operation with data token:

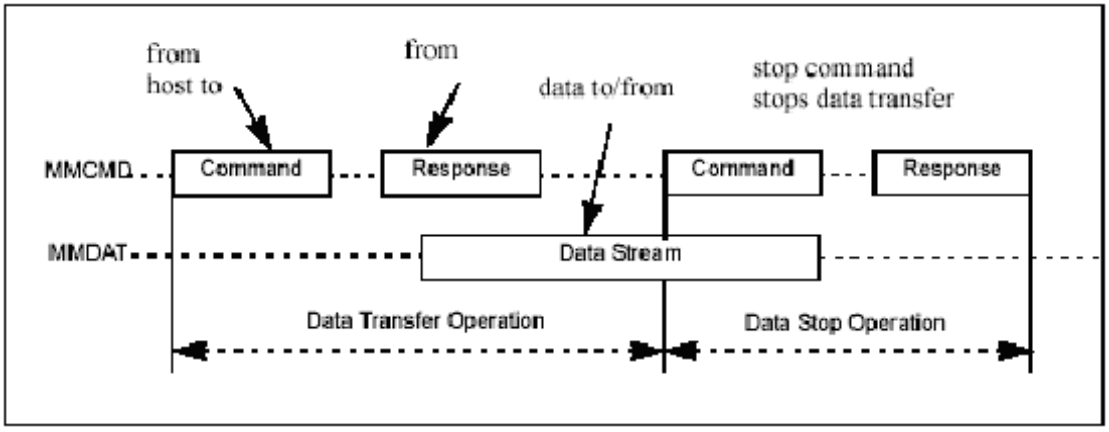


Figure 27-2. Operation With Data

27.3.2 Initialization

6 Pins of GPIOL[5:0] is used by the SD/MMC controller. For the SD/MMC interface function, configure these six pins as GPIO Alt Function 1.

1. Set **GPIOL AltFnSelL** register (C000 1036h) to xxxx_1010_1010_1010b.

To program the SDI modules, follow these basic steps:

1. Set **SDICON** and **SDIIntMsk0/1** to configure properly with clock and interrupt enable.
2. Set **SDIPRE** to configure with a proper value.
3. Wait 74 SDCLK clock cycle in order to initialize the card.

For the sequences to execute their actual operations, refer the operation sequence examples in 27.3.5.

27.3.3 Error Detection

The controller checks the following errors and stores the results into the Command Status Register (**SDICmdSta**) and the Data Status Register (**SDIDatSta**).

- Response CRC error: Command response shows the calculation of CRC error.
- Response time out: No response begins before the specific number of clocks
- Write data CRC error: A CRC status error on the data is returned by card.
- Read data CRC error: The data shows the calculation of CRC error.
- Read time out: No read data operation begins before the specified number of clocks.

SDI Control Register (SDICON)

Address : C000 1500h

Bit	R/W	Symbol	Description	Reset Value
4	R/W	**BYT_ORDER**	Byte order bit. This bit is to be set to '1'	0b
3	R/W	**RCV_IO_INT**	Receive SDIO interrupt from card. 0 = ignore interrupt 1 = receive SDIO interrupt	0b
2	R/W	**RWAIT_EN**	Read wait enable generation. Delay the next block to be transmitted from the card for SDIO 0 = disable 1 = enable read wait generation	0b
1	R/W	**FIFO_RESET**	FIFO reset. When 1, FIFO value reset and this bit is cleared automatically. 0 = normal mode 1 = FIFO reset	0b
0	R/W	**ENCLK**	ENCLK. Determines whether FSCLK Out is enabled. 0 = disable(prescaler off), 1 = clock enable	0b

TABLE 27-2. SDI CONTROL REGISTER (SDICON)

SDI Prescaler Register (SDIPRE)

Address : C000 1502h

Bit	R/W	Symbol	Description	Reset Value
7:0	R/W	**CLK_SCALE**	Determines SDI clock(SDCLK) rate per above equation. Baud rate = PCLK / (Prescaler value + 1)	00h

TABLE 27-3. SDI PRESCALER REGISTER (SDIPRE)

27.3.4 Clocks

The Processor enables/disables the SD bus clock (SDICLK) by means of the bit 0 (ENCLK) of the Control Register (**SDICON**). The SD bus clock frequency is adjusted by the value of the Prescaler Register (**SDIPRE**). The clock frequency is determined by the following expression:

Bus Clock Frequency = PCLK / (Prescaler value + 1)

27.3.5 SDIO Operation

There are SDIO Interrupt Receiving and Read Wait Request Generation in the types of the SDIO operation. These two types of operations are enabled by the RCV_IO_INT bit (i.e. bit [3]) and the RWAIT_EN bit (i.e. bit [2]) of the **SDICON** register respectively. Each step is per the following:

27.3.5.1 SDIO Interrupt

In 1-bit mode, an interrupt is received into the SDDAT1 pin. In 4-bit mode, it is shared by received data and interrupt and the range of interrupt detection is as follows:

1) Single Block: Time between A and B
   A : 2 clocks after completion of a data packet
   B : Completion of sending end bit of the next with-data command

2) Multi Block and SDIDatConH[5] = 0: Time between A and B, restart from C
   A : 2 clocks after completion of a data packet
   B : 2 clocks after A
   C : 2 clocks after end bit of abort command response

3) Multi Block and SDIDatConH[5] = 1: Time between C and B, restart from A
   A : 2 clocks after completion of a data packet
   B : 2 clocks after A

27.3.5.2 Read Wait Request

Regardless of bit mode, the Read Wait Signal is transmitted into the SDDAT2 pin in case of the following:

1) 2 clocks after end of a data block in read multiple operations
2) Transmission ends when the processor writes '1' to SDIDatSta[10]

27.3.6 Operation Sequence Example

27.3.6.1 Multiple Block Write with polling and single data line

The write block operation sequence with a single data line, multiple blocks and a polling case is as follows:

1. CMD7 selection of specific sdcard.
   1) Set **SDICmdArgH & SDICmdArgL** at 0000h.
   2) Set **SDICmdCon** at 0747h (wait response, immediate command start, command id = 7).
   3) Wait until sdcard finishes responding (check SDICmdSta[9]), and clear the status bit.
2. Clear command and data status register.
   1) Write **SDICmdSta** 0200h (clear response finish bit).
   2) Write **SDIDatSta** 07ffh (clear all status bits).
3. Set **SDIDatConL & SDIDatConH** to the proper value.
   1) Set **SDIDatConL** as (3000h | BlkNum) - polling, normal transfer, Tx start.
   2) Set **SDIDatConH** as 0012h - Tx starts after response, block mode, single data line.

4. Clear **SDICmdArgL** and **SDICmdArgH** - no argument for write block.
5. Set **SDICmdCon** as 0359h - short response, wait response, immediate start, command id=25.
6. Wait until response finish. (**SDICmdSta**[9] == 1), then write 1e00h to **SDICmdSta** to clear command status.
7. Write data for Tx to **SDIDAT** until all (BlkNum x BlkSize) bytes are transferred.

   When Tx FIFO is available (SDIFSTA[13]==1), data can be written.
8. Wait until DatFin active (**SDIDatSta**[4]), then force stop. --- Set the STOP bit of **SDIDatCon**[14].
9. Initiate the stop command as follows:
   1) Write **SDICmdArgL** as 0000h.
   2) Write **SDICmdArgL** as 0000h.
   3) Write **SDICmdCon** as 134ch.
10. When Read wait request occurs (SDIDatSta[10]==1), write '1' to this bit to xlear.
11. Clear **SDIDatConL** and **SDIDatConH** by writing '1' to all bits.

SDI Command Argument Register Low (SDICmdArgL)

Address : C000 1504h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	CMD_ARGL	Command Argument bit[15:0]	0000h

TABLE 27-4. SDI COMMAND ARGUMENT REGISTER LOW (SDICMDARGL)

SDI Command Argument Register High (SDICmdArgH)

Address : C000 1506h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	CMD_ARGH	Command Argument bit[31:16]	0000h

TABLE 27-5. SDI COMMAND ARGUMENT REGISTER HIGH (SDICMDARGH)

SDI Command Control Register (SDICmdCon)

Address : C000 1508h

Bit	R/W	Symbol	Description	Reset Value
12	R/W	**ABT_CMD**	Abort command. Determines whether command type is for abort(for SDIO) 0 = normal command 1 = abort command (CMD12, CMD52)	0
11	R/W	**CMD_DAT**	Command with data or not for SDIO 0 = without data 1 = with data	0
10	R/W	**HOST_RCV**	Determines whether host receives a 136-bit long response or not 0 = short response 1 = long response	0
9	R/W	**HOST_WAITS**	Determines whether host waits for a response or not 0 = no response 1 = wait response	0
8	R/W	**CMD_OP_ST**	Determines whether command operation starts or not 0 = command ready 1 = command start	0
7:0	R/W	**CMD_INDEX**	Command index with start 2bit (8bit)	0

TABLE 27-6. SDI COMMAND CONTROL REGISTER (SDICMDCON)

SDI Command Status Register (SDICmdSta)

Address : C000 150Ah

Bit	R/W	Symbol	Description	Reset Value
12	R	**RSP_CRC**	CRC check failed when command response received. This flag is cleared by setting this bit to '1' 0 = not detected 1 = crc fail	0
11	R	**CMD_SENT**	Command sent(not concerned with response). This flag is cleared by setting this bit to '1'. 0 = not detec, 1 = command end	0
10	R	**CMD_TOUT**	Command response timeout(64clk). This flag is cleared by setting this bit to '1'.. 0 = not detected 1 = timeout	0
9	R	**RSP_FIN**	Command response received. This flag is cleared by setting this bit to '1'. 0 = not detect 1 = response end	0
8	R	**CMD_ON**	Command transfer in progress 0 = not detected 1 = in progress	0
7:0	R	**RSPINDEX**	Response index 6bit with start 2bit (8bit)	0

TABLE 27-7. SDI COMMAND STATUS REGISTER (SDICMDSTA)

SDI Response Register 0 (SDIRSP0)

Address : C000 150Ch

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**CRD_STA0**	Card status[15:0](short), card status[111:96](long)	0000h

TABLE 27-8. SDI RESPONSE REGISTER 0 (SDIRSP0)

SDI Response Register 1 (SDIRSP1)

Address : C000 150Eh

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**CRD_STA1**	Card status[31:16](short), card status[127:112](long)	0000h

TABLE 27-9. SDI RESPONSE REGISTER 1 (SDIRSP1)

SDI Response Register 2 (SDIRSP2)

Address : C000 1510h

Bit	R/W	Symbol	Description	Reset Value
15:8	R	**CRC7**	CRC7(with end bit, short), card status[95:88](long)	0
7:0	R	**CRD_STA2**	unused(short), card status[87:80](long)	0

TABLE 27-10. SDI RESPONSE REGISTER 2 (SDIRSP2)

SDI Response Register 3 (SDIRSP3)

Address : C000 1512h

Bit	R/W	Symbol	Description	Reset Value
15:0	R	**CRD_STA3**	unused (short), card status[79:64](long)	0

TABLE 27-11. SDI RESPONSE REGISTER 3 (SDIRSP3)

SDI Response Register 4 (SDIRSP4)

Address : C000 1514h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**CRD_STA4**	unused(short), card status[63:48](long)	0

TABLE 27-12. SDI RESPONSE REGISTER 4 (SDIRSP4)

SDI Response Register 5 (SDIRSP5)

Address : C000 1516h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**CRD_STA5**	unused(short), card status[47:32](long)	0

TABLE 27-13. SDI RESPONSE REGISTER 5 (SDIRSP5)

SDI Response Register 6 (SDIRSP6)

Address : C000 1518h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R	**CRD_STA6**	unused(short), card status[31:16](long)	0

TABLE 27-14. SDI RESPONSE REGISTER 6 (SDIRSP6)

SDI Response Register 7 (SDIRSP7)

Address : C000 151Ah

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	**CRD_STA6**	unused(short), card status[15:0](long)	0

TABLE 27-15. SDI RESPONSE REGISTER 7 (SDIRSP7)

SDI Block Size Register (SDIBSize)

Address : C000 151Eh

Bit	R/W	Symbol	Description	Reset Value
11:0	R/W	**BLK_SIZ_VAL**	Block Size value(0~4095 byte)	0

TABLE 27-16. SDI BLOCK SIZE REGISTER (SDIBSIZE)

SDI Data Control Register Low (SDIDatConL)

Address : C000 1520h

Bit	R/W	Symbol	Description	Reset Value
15	R/W	**Reserved**	-	-
14	R/W	**STOP_FORCE**	STOP Determines whether data transfer was stopped by force 0 = normal 1 = stop by force	0
13:12	R/W	**DAT_MODE**	Determines which direction of data transfer 00 = ready 01 = only busy check start 10 = data receive start 11 = data transmit start	0

Bit	R/W	Symbol	Description	Reset Value
11:0	R/W	**BLK_NUM**	Block Number(0~4095), don't care when in stream mode	0

TABLE 27-17. SDI DATA CONTROL REGISTER LOW(SDIDATCONL)

SDI Data Control Register High (SDIDatConH)

Address : C000 1522h

Bit	R/W	Symbol	Description	Reset Value
5	R/W	**PRD_TYPE**	Determines whether SDIO interrupt period is 2 cycle or extended to more cycles when last data block is transferred (for SDIO) 0 = exactly 2 cycle 1 = more cycle (like single block)	0
4	R/W	**TARSP**	Determines when data transmit start after response receive 0 = directly after DatMode set 1 = after response received(assume DatMode set to 2'b11)	0
3	R/W	**RACMD**	Determines when data receive start after command sent 0 = directly after DatMode set 1 = after command sent (assume DatMode set to 2'b10)	0
2	R/W	**BACMD**	Determines when busy receive start after command sent 0 = directly after DatMode set 1 = after command sent (assume DatMode set to 2'b01)	0
1	R/W	**BLK_MODE**	Data transfer mode 0 = stream data transfer 1 = block data transfer	0
0	R/W	**WIDE_BUS**	Determines enable wide bus mode 0 = standard bus mode(only SDIDAT[0] used) 1 = wide bus mode(SDIDAT[3:0] used)	0

TABLE 27-18. SDI DATA CONTROL REGISTER HIGH (SDIDATCONH)

SDI Data Remain Counter Register Low (SDIDatCntL)

Address : C000 1524h

Bit	R/W	Symbol	Description	Reset Value
15:12	R	**BLK_NUM_CNT**	Remaining Block number [3:0]	0
11:0	R	**BLK_CNT**	Remaining data of 1 block	0

TABLE 27-19. SDI DATA REMAIN COUNTER REGISTER LOW (SDIDATCNTL)

SDI Data Remain Counter Register High (SDIDatCntH)

Address : C000 1526h

Bit	R/W	Symbol	Description	Reset Value

Bit	R/W	Symbol	Description	Reset Value
7:0	R	**BLK_NUM_CNT**	Remaining Block number [11:4]	0

TABLE 27-20. SDI DATA REMAIN COUNTER REGISTER HIGH (SDIDATCNTH)

SDI Data Status Register (SDIDatSta)

Address : C000 1528h

Bit	R/W	Symbol	Description	Reset Value
10	R	**RD_WAIT_REQ**	Read wait request signal transmitted to SD card. The request signal is stopped. This flag is cleared by setting this bit to '1'.. 0 = did not occur 1 = read wait request occurred	0
9	R	**IO_INT_DET**	SDIO interrupt detect. This flag is cleared by setting this bit to '1'. 0 = not detected 1 = SDIO interrupt detect	0
8	R	**FF_FAIL**	FIFO fail error when FIFO occurs overrun/underrun/misaligned data saving. This flag is cleared by setting this bit to '1'. 0 = not detected 1 = FIFO fail	0
7	R	**CRC_STA**	CRC Status error when data block sent(CRC check failed). This flag is cleared by setting this bit to '1'1. 0 = not detected 1 = crc status fail	0
6	R	**DAT_CRC**	Data block received error(CRC check failed). This flag is cleared by setting this bit to '1'. 0 = not detected 1 = receive crc fail	0
5	R	**DAT_TOUT**	Data receive timeout. This flag is cleared by setting this bit to '1'. 0 = not detected 1 = timeout	0
4	R	**DAT_FIN**	Data transfer complete(data counter is zero). This flag is cleared by setting the bit to '1'. 0 = not detected 1 = data finish detect	0
3	R	**BYSY_FIN**	Only busy check finish. This flag is cleared by setting this bit to '1'. 0 = not detected 1 = busy finish detect	0
2	R	**SBIT_ERR**	Start bit is not detected on all data signals in wide bus mode. This flag is cleared by setting this bit to '1'. 0 = not detected 1 = command end	0
1	R	**TX_DAT_ON**	Data transmit in progress 0 = not active 1 = data Tx in progress	0
0	R	**RX_DAT_ON**	Data receive in progress 0 = not active, 1 = data Rx in progress	0

TABLE 27-21. SDI DATA STATUS REGISTER (SDIDATSTA)

SDI FIFO Status Register (SDIFSTA)

Address : C000 152Ah

Bit	R/W	Symbol	Description	Reset Value
13	R	**TF_DET**	This bit indicates that FIFO data is available for transmit when DatMode is in data transmit mode. 0 = not detected(FIFO full) 1 = detected(0 ≤ FIFO ≤ 15)	0
12	R	**RF_DET**	This bit indicates that FIFO data is available for receive when DatMode is in data receive mode. 0 = not detected(FIFO empty) 1 = detect(1 ≤ FIFO ≤ 16)	0
11	R	**TF_HALF**	Set when TxFIFO has less than 33 bytes. 0 = 33 ≤ FIFO ≤ 64 1 = 0 ≤ FIFO ≤ 32	0
10	R	**TF_EMPTY**	Set when Tx FIFO is empty. 0 = 1 ≤ FIFO ≤ 64 1 = empty	0
9	R	**RF_LAST**	Set when Rx FIFO has last data of all data block. 0 = not received yet 1 = last data ready	0
8	R	**RF_FULL**	Set when Rx FIFO is full. 0 = 0 ≤ FIFO ≤ 63 1 = full (64byte)	0
7	R	**RF_HALF**	Set when Rx FIFO has more than 31 bytes. 0 = 0 ≤ FIFO ≤ 31 1 = 32 ≤ FIFO ≤ 64	0
6:0	R	**FF_CNT**	Number of data(byte) in FIFO	0

TABLE 27-22. SDI FIFO STATUS REGISTER (SDIFSTA)

SDI Data Register (SDIDAT)

Address : C000 152Ch

Bit	R/W	Symbol	Description	Reset Value
7 : 0	R/W	**SDI_DAT**	This field contains the data to be transmitted or received over the SDI channel	0

TABLE 27-23. SDI DATA REGISTER (SDIDAT)

SDI Interrupt Mast Register0 (SDIIntMsk0)

Address : C000 1530h

Bit	R/W	Symbol	Description	Reset Value
1	R/W	**RES_CRC_MSK**	Response CRC check fail interrupt mask 0 = disable 1 = enable	0
0	R/W	**CMD_SNT_MSK**	Command sent(no response) interrupt mask 0 = disable 1 = enable	0

TABLE 27-24. SDI INTERRUPT MAST REGISTER0 (SDIINTMSK0)

SDI Interrupt Mast Register1 (SDIIntMsk1)

Address : C000 1532h

Bit	R/W	Symbol	Description	Reset Value
15	R/W	**TOUT_MSK**	Response timeout occur interrupt mask 0 = disable 1 = enable	0
14	R/W	**CMD_RCV_MSK**	Command response receive interrupt mask 0 = disable 1 = enable	0
13	R/W	**RWR_MSK**	Read wait request occur interrupt mask 0 = disable 1 = enable	0
12	R/W	**SDIO_IRQ_MSK**	SDIO interrupt from the card occur interrupt mask 0 = disable 1 = enable	0
11	R/W	**FF_FAIL_MSK**	FIFO fail error occur interrupt mask 0 = disable 1 = enable	0
10	R/W	**SCRCERR_MSK**	CRC status error occur interrupt mask 0 = disable 1 = enable	0
9	R/W	**DCRCERR_MSK**	Data receive CRC error occur interrupt mask 0 = disable 1 = enable	0
8	R/W	**DTIM_OUT_MSK**	Data receive timeout occur interrupt mask 0 = disable 1 = enable	0
7	R/W	**DCNT0_MSK**	Data counter zero interrupt mask 0 = disable, 1 = enable	0
6	R/W	**BUSCHK_MSK**	Busy check complete interrupt mask 0 = disable 1 = enable	0
5	R/W	**SB_ERR_MSK**	Start bit error detect interrupt mask 0 = disable 1 = enable	0
4	R/W	**TXHF_MSK**	Tx FIFO half full interrupt mask	0

Bit	R/W	Symbol	Description	Reset Value
			0 = disable, 1 = enable	
3	R/W	**TXEMT_MSK**	Tx FIFO empty interrupt mask 0 = disable 1 = enable	0
2	R/W	**RXLD_MSK**	Rx FIFO has last data interrupt mask 0 = disable 1 = enable	0
1	R/W	**RXFUL_MSK**	Rx FIFO full interrupt mask 0 = disable 1 = enable	0
0	R/W	**RXHF_MSK**	Rx FIFO half full interrupt mask 0 = disable 1 = enable	0

TABLE 27-25. SDI INTERRUPT MAST REGISTER1 (SDIINTMSK1)

SDI Data Timer Register Low (SDIDTimerL)

Address : C000 1536h

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	**TIMER_L**	Data/Busy timeout period LS 16 bits	0

TABLE 27-26. SDI DATA TIMER REGISTER LOW (SDIDTIMERL)

SDI Data Timer Register High (SDIDTimerH)

Address : C000 1538h

Bit	R/W	Symbol	Description	Reset Value
4 : 0	R/W	**TIMER_H**	Data/Busy timeout period MS 5 bits	0

TABLE 27-27. SDI DATA TIMER REGISTER HIGH (SDIDTIMERH)

SDI Shift Register Low (SDSftRegL)

Address : C000 153Ah

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	**SFT_REG L**	Shift register lower half word [15:0]	0

TABLE 27-28. SDI SHIFT REGISTER LOW (SDSFTREGL)

SDI Shift Register High (SDSftRegH)

Address : C000 153Ch

Bit	R/W	Symbol	Description	Reset Value
15 : 0	R/W	**SHT_REG_H**	Shift register higher half word [31:16]	0

TABLE 27-29. SDI SHIFT REGISTER HIGH (SDSFTREGH)

27.3.6.2 Multiple Block Read with polling and single data line

The block operation sequence with single data line, multiple blocks and polling case is as follows:

1. Select specific sdcard by CMD7.
   1) Set **SDICmdArgH & SDICmdArgL** as 0000h.
   2) Set **SDICmdCon** as 0747h (wait response, immediate command start, command id = 7).
   3) Wait until response from sdcard finish (check SDICmdSta[9]), then clear status bit.
2. Clear command and data status register.
   1) Write **SDICmdSta** 0200h (clear response finish bit).
   2) Write **SDIDatSta** 07ffh (clear all status bits).
3. Set **SDIDatConL & SDIDatConH** to the proper value.
   1) Set **SDIDatConL** as (2000h | BlkNum) - polling, normal transfer, Rx start.
   2) Set **SDIDatConH** as 000ah - Rx start after response, block mode, single data line.
4. Clear **SDICmdArgL** and **SDICmdArgH** - no argument for write block.
5. Set **SDICmdCon** as 0352h - short response, wait response, immediate start, command id=18.
6. Wait until response finishes (**SDICmdSta**[9] == 1), then write 1e00h to **SDICmdSta** to clear the command status.
7. Read data for Rx from **SDIDAT** until (BlkNum x BlkSize) bytes are all transferred.

   Data can be read when Rx FIFO is available (**SDIFSTA**[12]==1).
8. Wait until DatFin active (**SDIDatSta**[4]), then force stop. --- Set the STOP bit of **SDIDatCon**[14].
9. Initiate stop command as follows:
   1) Write **SDICmdArgL** as 0000h.
   2) Write **SDICmdArgL** as 0000h.
   3) Write **SDICmdCon** as 134ch.
10. If Read wait request occurs (**SDIDatSta**[10] == 1), then Write '1' to this bit to clear.
11. Clear **SDIDatConL** and **SDIDatConH** by writing '1' to all bits.

27.4 REGISTER MAP

Bit	R/W	Symbol	Description	Reset Value
SDI Control Register (SDICON) ***Address : C000 1500h***				
4	R/W	**BYT_ORDER**	Byte order bit. This bit is to be set to '1'	0b
3	R/W	**RCV_IO_INT**	Receive SDIO interrupt from card.	0b
2	R/W	**RWAIT_EN**	Read wait enable generation	0b
1	R/W	**FIFO_RESET**	FIFO reset.	0b
0	R/W	**ENCLK**	ENCLK	0b
SDI Baud Rate Prescaler Register (SDIPRE) ***Address : C000 1502h***				
7:0	R/W	**CLK_SCALE**	SDI clock(SDCLK) rate	00h
SDI Command Argument Register Low (SDICmdArgL) ***Address : C000 1504h***				
15 : 0	R/W	**CMD_ARGL**	Command Argument bit[15:0]	0000h
SDI Command Argument Register High (SDICmdArgH) ***Address : C000 1506h***				
15 : 0	R/W	**CMD_ARGH**	Command Argument bit[31:16]	0000h
SDI Command Control Register (SDICmdCon) ***Address : C000 1508h***				
12	R/W	**ABT_CMD**	Abort command	0
11	R/W	**CMD_DAT**	Command with data or not for SDIO	0
10	R/W	**HOST_RCV**	Determines whether host receives a 136-bit long response or not	0
9	R/W	**HOST_WAITS**	Determines whether host waits for a response or not	0
8	R/W	**CMD_OP_ST**	Determines whether command operation starts or not	0
7:0	R/W	**CMD_INDEX**	Command index with start 2bit(8bit)	0
SDI Command Status Register (SDICmdSta) ***Address : C000 150Ah***				
12	R	**RSP_CRC**	CRC check failed when command response was received.	0
11	R	**CMD_SENT**	Command sent(not concerned with response)	0
10	R	**CMD_TOUT**	Command response timeout(64clk)	0
9	R	**RSP_FIN**	Command response received	0

Bit	R/W	Symbol	Description	Reset Value
8	R	**CMD_ON**	Command transfer in progress	0
7:0	R	**RSPINDEX**	Response index 6bit with start 2bit (8bit)	0
SDI Response Register 0 (SDIRSP0) ***Address : C000 150Ch***				
15 : 0	R	**CRD_STA0**	Card status[15:0](short), card status[111:96](long)	0000h
SDI Response Register 1 (SDIRSP1) ***Address : C000 150Eh***				
15 : 0	R	**CRD_STA1**	Card status[31:16](short), card status[127:112](long)	0000h
SDI Response Register 2 (SDIRSP2) ***Address : C000 1510h***				
15:8	R	**CRC7**	CRC7(with end bit, short), card status[95:88](long)	0
7:0	R	**CRD_STA2**	unused(short), card status[87:80](long)	0
SDI Response Register 3 (SDIRSP3) ***Address : C000 1512h***				
15:0	R	**CRD_STA3**	unused (short), card status[79:64](long)	0
SDI Response Register 4 (SDIRSP4) ***Address : C000 1514h***				
15 : 0	R	**CRD_STA4**	unused(short), card status[63:48](long)	0
SDI Response Register 5 (SDIRSP5) ***Address : C000 1516h***				
15 : 0	R	**CRD_STA5**	unused(short), card status[47:32](long)	0
SDI Response Register 6 (SDIRSP6) ***Address : C000 1518h***				
15 : 0	R	**CRD_STA6**	unused(short), card status[31:16](long)	0
SDI Response Register 7 (SDIRSP7) ***Address : C000 151Ah***				
15 : 0	R/W	**CRD_STA6**	unused(short), card status[15:0](long)	0
SDI Block Size Register (SDIBSize) ***Address : C000 151Eh***				
11:0	R/W	**BLK_SIZ_VAL**	Block Size value(0~4095 byte)	0
SDI Data Control Register Low (SDIDatConL) ***Address : C000 1520h***				

Bit	R/W	Symbol	Description	Reset Value
15	R/W	**Reserved**	-	-
14	R/W	**STOP_FORCE**	STOP Determines whether data transfer stop by force or not	0
13:12	R/W	**DAT_MODE**	Determines which direction of data transfer	0
11:0	R/W	**BLK_NUM**	Block Number(0~4095)	0
SDI Data Control Register High (SDIDatConH) ***Address : C000 1522h***				
5	R/W	**PRD_TYPE**	Determines whether SDIO interrupt period is 2 cycles or more	0
4	R/W	**TARSP**	Determines when data transmit starts after response receive	0
3	R/W	**RACMD**	Determines when data receive starts after command sent	0
2	R/W	**BACMD**	Determines when busy receive starts after command sentt	0
1	R/W	**BLK_MODE**	Data transfer mode	0
0	R/W	**WIDE_BUS**	Determines enable wide bus mode	0
SDI Data Remain Counter Register Low (SDIDatCntL) ***Address : C000 1524h***				
15:12	R	**BLK_NUM_CNT**	Remaining Block number [3:0]	0
11:0	R	**BLK_CNT**	Remaining data of 1 block	0
SDI Data Remain Counter Register High (SDIDatCntH) ***Address : C000 1526h***				
7:0	R	**BLK_NUM_CNT**	Remaining Block number [11:4]	0
SDI Data Status Register (SDIDatSta) ***Address : C000 1528h***				
10	R	**RD_WAIT_REQ**	Read wait request signal transmitted to SD card	0
9	R	**IO_INT_DET**	SDIO interrupt detect	0
8	R	**FF_FAIL**	FIFO fail error	0
7	R	**CRC_STA**	CRC Status error when data block sent(CRC check failed)	0
6	R	**DAT_CRC**	Data block received error(CRC check failed)	0
5	R	**DAT_TOUT**	Data receive timeout	0
4	R	**DAT_FIN**	Data transfer complete(data counter is zero)	0
3	R	**BYSY_FIN**	Only busy check finish	0
2	R	**SBIT_ERR**	Start bit is not detected on all data signals in wide bus mode	0
1	R	**TX_DAT_ON**	Data transmit in progress	0

Bit	R/W	Symbol	Description	Reset Value
0	R	**RX_DAT_ON**	Data receive in progress	0
SDI FIFO Status Register (SDIFSTA) ***Address : C000 152Ah***				
13	R	**TF_DET**	FIFO data is available for transmit	0
12	R	**RF_DET**	FIFO data is available for receive	0
11	R	**TF_HALF**	Set when TxFIFO has less than 33 bytes	0
10	R	**TF_EMPTY**	Set when Tx FIFO is empty	0
9	R	**RF_LAST**	Set when Rx FIFO has last data of all data block	0
8	R	**RF_FULL**	Set when Rx FIFO is full	0
7	R	**RF_HALF**	Set when Rx FIFO has more than 31 bytes	0
6:0	R	**FF_CNT**	Number of data(byte) in FIFO	0
SDI Data Register (SDIDAT) ***Address : C000 152Ch***				
7 : 0	R/W	**SDI_DAT**	Data to be transmitted or received over the SDI channel	0
SDI Interrupt Mast Register0 (SDIIntMsk0) ***Address : C000 1530h***				
1	W	**RES_CRC_MSK**	Response CRC check fail interrupt mask	0
0	W	**CMD_SNT_MSK**	Command sent(no response) interrupt mask	0
SDI Interrupt Mast Register1 (SDIIntMsk1) ***Address : C000 1532h***				
15	W	**TOUT_MSK**	Response timeout occurs - interrupt mask	0
14	W	**CMD_RCV_MSK**	Command response received - interrupt mask	0
13	W	**RWR_MSK**	Read wait request occurs - interrupt mask	0
12	W	**SDIO_IRQ_MSK**	SDIO interrupt from the card occurs - interrupt mask	0
11	W	**FF_FAIL_MSK**	FIFO fail error occurs - interrupt mask	0
10	W	**SCRCERR_MSK**	CRC status error occurs - interrupt mask	0
9	W	**DCRCERR_MSK**	Data receive CRC error occurs - interrupt mask	0
8	W	**DTIM_OUT_MSK**	Data receive timeout occurs - interrupt mask	0
7	W	**DCNT0_MSK**	Data counter zero - interrupt mask	0
6	W	**BUSCHK_MSK**	Busy check complete - interrupt mask	0
5	W	**SB_ERR_MSK**	Start bit error detected - interrupt mask	0

Bit	R/W	Symbol	Description	Reset Value
4	W	**TXHF_MSK**	Tx FIFO half full - interrupt mask	0
3	W	**TXEMT_MSK**	Tx FIFO empty - interrupt mask	0
2	W	**RXLD_MSK**	Rx FIFO has last data - interrupt mask	0
1	W	**RXFUL_MSK**	Rx FIFO full - interrupt mask	0
0	W	**RXHF_MSK**	Rx FIFO half full - interrupt mask	0
SDI Data Timer Register Low (SDIDTimerL) ***Address : C000 1536h***				
15 : 0	R/W	**TIMER_L**	Data/Busy timeout period LS 16 bits	0
SDI Data Timer Register High (SDIDTimerH) ***Address : C000 1538h***				
4 : 0	R/W	**TIMER_H**	Data/Busy timeout period MS 5 bits	0
SDI Shift Register Low (SDSftRegL) ***Address : C000 153Ah***				
15 : 0	R/W	**SFT_REG L**	Shift register lower half word [15:0]	0
SDI Shift Register Low (SDSftRegL) ***Address : C000 153Ch***				
15 : 0	R/W	**SHT_REG_H**	Shift register higher half word [31:16]	0

TABLE 27-30. REGISTER MAP

CHAPTER 28

MEMORY STICK CONTROLLER

28. MEMORY STICK CONTROLLER

28.1 OVERVIEW

The MP2520F provides the Memory Stick Controller to access a SONY Memory Stick. Hard wired logic supports the Protocol as defined by the Memory Stick, and supports Card In/Out Detect and Memory Stick Interrupt functions.

Data transferred from/to the Memory Stick is stored in Internal Data FIFO. Therefore, the CPU can access the data in PIO Mode and transmit it to the Memory via the DMA.

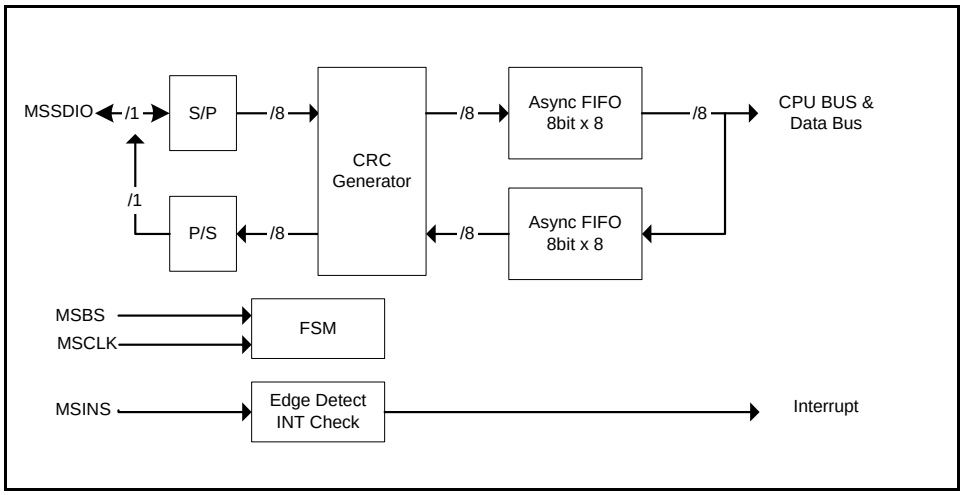


Figure 28-1. Memory Stick Controller Block Diagram

FEATURES

- Support DMA, PIO transfer mode
- 8 Byte Transmit FIFO, 8 Byte Receive FIFO
- CRC Code Generator
- Supports Card In/Out Detect, Memory Stick Interrupt

28.2 SIGNAL DESCRIPTION

The Interface Signals for a memory stick are as follows:

Name	Direction	Description
MSINS	I	Stick insertion/extraction detect-signal
MSCLK	O	Serial protocol clock signal Signals on MSBS and MSSDIO are output at trailing edge and input (latched) at leading edge. It is always output except for BS0 period.
MSSDIO	I/O	Serial protocol data signal The direction of the data and the data itself will change at each Bus State. Data is 8 bit, MSB First.
MSBS	O	Serial Protocol bus state signal Indicates Bus State (0~3) on SDIO and its timing of starting transfer.

TABLE 28-1. INTERFACE SIGNAL

28.3 MEMORY STICK CONTROLLER OPERATION

28.3.1 PROTOCOL OVERVIEW

The MSBS signal classifies data on MSSDIO into four states according to the attributes and transfer direction; one state (BS0) with no packet communication going on, and three (BS1, 2, and 3) states with packet communication being executed. The BS signal also controls the timing of data output.

BS1 through BS3 are dealt with as one packet, and one communication is always completed within one packet.

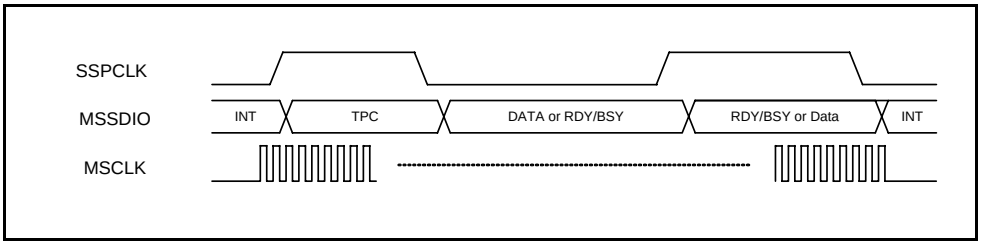


Figure 28-2. Timing Diagram

28.3.2 INITIALIZATION

If the previous Packet Transform is terminated abnormally, the Memory Stick Controller can be initialized by CPU. To initialize with the CPU, the MSRSTENB bit of the MSCTRL Register must be toggled.
After the initialization, to transfer data from/to the Memory Stick, the MSCTRL Register is set according to the Transfer type before the transmit.

The MSDMAENB determines whether to allow the CPU to use the DMA or access the contents of FIFO when a Read/Write Packet is processed.

The MSCRCENB determines the CRC Check will be used or not when a Packet Transfer is operated. In write packet mode, if MSCRCENB bit is set, the CRC Code made internally is added to the Data to be sent to a Memory Stick. When the bit is set in the Read Packet mode, the CRC Code made by the external Memory Stick is stored in the MSCRC Register to be read by the CPU.

The MSREADENB determines whether the Packet Transfer will be performed as Read Packet mode or Write Packet mode.

The MSDATACNT specifies the number of the data to be transferred in the Packet transfer.

The MSTIMEOUT specifies the number of auto-retry when the external Memory Stick does not respond to a Protocol.

The MSTPCDATA specifies the Operation of the Packet to be transferred into TRC (Transfer Protocol Command) defined by the Memory Stick Protocol.

28.3.3 DATA TRANSFER

If the MSRUN bit of the MSCTRL is set after the initialization of the Packet to be transferred, the Packet Transfer is initiated.

When DMA DMA mode is selected, data transfer is done by DMA.

When PIO mode is enabled and Write Packet mode is selected, Write Packed transfer is executed when the effective data is stored in write FIFO.

When Read Packet mode is selected while PIO mode is enabled, Read Packet Transfer is executed until the ReadFIFO becomes full.

28.3.4 INTERRUPT

The Memory stick Controller of the MP2520F has six Interrupt Sources.

With the MSINS Signal, the MSINIRQENB enables Memory Stick in detect interrupt when the Memory Stick is inserted.

The MSOUTIRQENB enable Memory Stick out detect interrupt when the Memory Stick is extracted.

The MSENDIRQENB initiates an Interrupt when the transfer of the data specified by the MSDATACNT is completed.

The MSUNDERIRQENB/MSOVERIRQENB initiates an Interrupt when an underflow or overflow occurs in FIFO on Data Transfer.

The MSINTIRQENB initiates an interrupt to the CPU when the Memory Stick produces an interrupt.

28.4 MEMORY STICK CONTROLLER REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
Memory Stick Control Register (MSCTRL) ***Address : C000 1600h***				
15	R	**Reserved**	-	-
14	R/W	**MSRUN**	(Writes) Operate Memory Stick Controller 0 : Disable 1 : Enable (Read) Check Memory Stick Controller status 0 : Idle 1 : Busy	0
13	R/W	**MSDMAENB**	Selects DMA Mode or PIO Mode 0 : PIO mode 1 : DMA mode	0
12	R/W	**MSRSTENB**	Initiates internal Block 0 : Normal 1 : Soft Reset	0
11	R/W	**MSREADENB**	Sets Read/Write operation 0 : Write Operation 1 : Read Operation	0
10	R/W	**MSCRCENB**	Sets CRC check option when Data Transfer 0 : Disable 1 : Enable	0
9 : 0	R/W	**MSDATACNT**	Set Transfer Data Size	0
Memory Stick FIFO Register (MSFIFO) ***Address : C000 1602h***				
15 : 8	R	**Reserved**	-	-
7 : 0	R/W	**MSFIFO**	FIFO Data Read / Write	0
Memory Stick FIFO Status Register (MSFIFOST) ***Address : C000 1604h***				
15 : 4	R	**Reserved**	-	-
3	R	**RFFFULL**	Reads FIFO Full Flag	0
2	R	**RFFEMPTY**	Reads FIFO Empty Flag	1
1	R	**WFFFULL**	Writes FIFO Full Flag	0
0	R	**WFFEMPTY**	Writes FIFO Empty Flag	1

Bit	R/W	Symbol	Description	Reset Value
Memory Stick interrupt Control Register (MSINTCTRL) ***Address : C000 1606h***				
15 : 12	R	**Reserved**	-	-
11	R/W	**MSINIRQENB**	Memory Stick In Detect Interrupt Enable 0 : Disable 1 : Enable	0
10	R/W	**MSOUTIRQENB**	Memory Stick Output Detect Interrupt Enable 0 : Disable 1 : Enable	0
9	R/W	**MSENDIRQENB**	Invokes Interrupt after data transferring set by MSDATACNT 0 : Disable 1 : Enable	0
8	R/W	**MSUNDERIRQENB**	Underflow Interrupt Enable 0 : Disable 1 : Enable	0
7	R/W	**MSOVERIRQENB**	Overflow Interrupt Enable 0 : Disable 1 : Enable	0
6	R/W	**MSINTIRQENB**	Memory Stick INT Interrupt Enable 0 : Disable 1 : Enable	0
5	R/W	**MSINIRQPEND**	Memory Stick In Detect Interrupt Pending Register, Set this bit to 1 to clear it.	0
4	R/W	**MSOUTIRQPEND**	Memory Stick Output Detect Interrupt Pending Register	0
3	R/W	**MSENDIRQPEND**	Transfer Complete Pending Register	0
2	R/W	**MSUNDERIRQPEND**	Underflow Interrupt Pending Register	0
1	R/W	**MSOVERIRQPEND**	Overflow Interrupt Pending Register	0
0	R/W	**MSINTIRQPEND**	Memory Stick INT Interrupt Pending Register	0
Memory Stick CRC Register (MSCRC) ***Address : C000 1608h***				
15 : 0	R	**CRCREG**		0
Memory Stick Timeout Register (MSTIMEOUT) ***Address : C000 160Ah***				
15 : 8	R	**Reserved**		-
7 : 0	R/W	**TIMEOUT**	Memory Stick will be initiated if Memory Stick does not respond in TIMEOUT time	1
Memory Stick TPC Register (MSTPC) ***Address : C000 160Ch***				
15 : 8	R	**Reserved**	-	-
7 : 0	R/W	**TPC.**	TPC Data	1

Bit	R/W	Symbol	Description	Reset Value
Memory Stick TPC Register (MSTPC) ***Address : C000 160Eh***				
15 : 8	R	**Reserved**	-	-
7 : 0	R	**NUMDATA**	Contains the number of the transmitted bytes via the Memory Stick Protocol.	1

TABLE 28-2. MEMORY STICK CONTROLLER REGISTERS LIST

MAGIC EYES

CHAPTER 29

CD-ROM DECODER

29. CD-ROM DECODER

29.1 OVERVIEW

29.1.1 CDRSYNCDESC Block

The CDRSYNCDESC block receives a CDP signal input from external and detect s Sync. After then, this block Descrambles the signal according to CDRD_DESCENB or write Data to the Memory.

If the Sync is detected, the block writes 2340 Byte unconditionally. If, however, Data error occurs or new Sync is detected before writing, the block stops the writing operation and generates o_EndRAW.

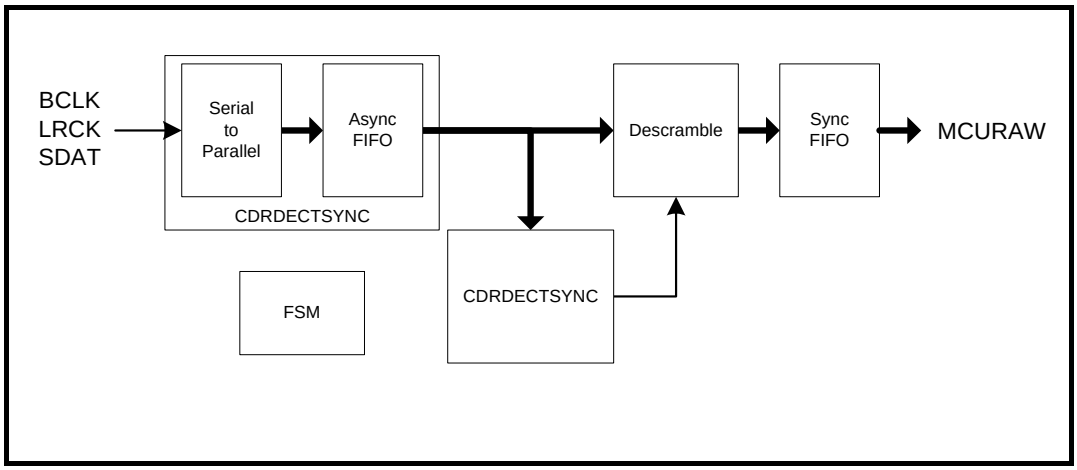


Figure 29-1. CDRSYNCDESC Block Diagram

Supported CD Format

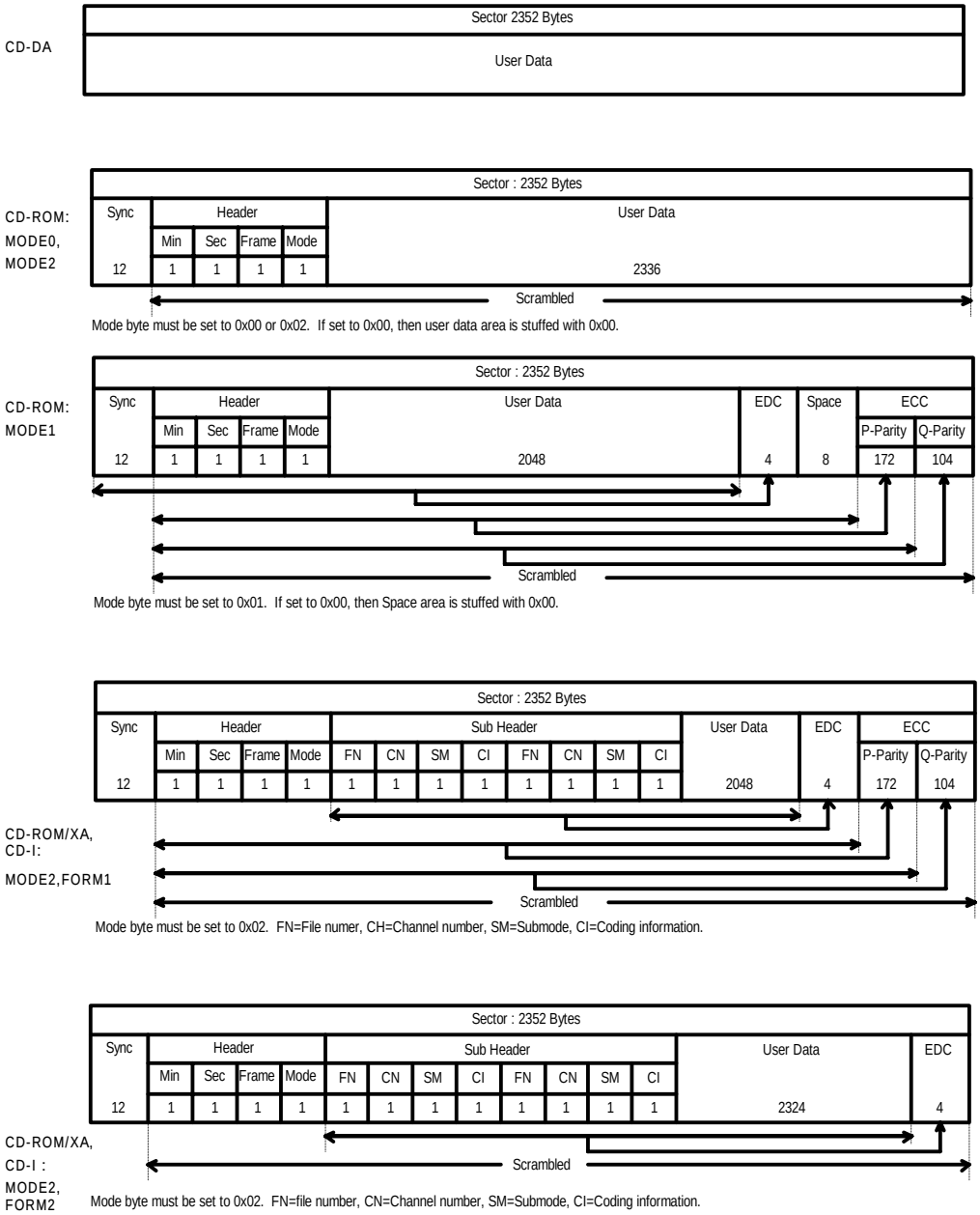


Figure 29-2. Supported CD Formats

29.1.2 CDRECCEDC Block

The CDRECCEDC executes ECC and EDC with the contents of the Memory specified by the CPU or TOPFSM. The block writes the results to the external Memory and returns the states of EDC Error and the value of MSF Mode.

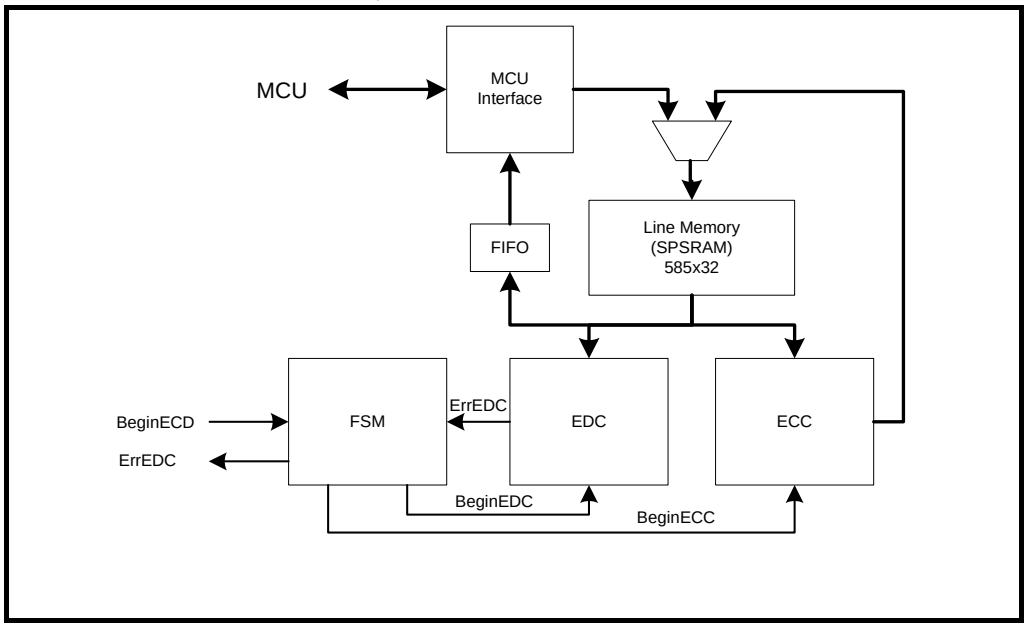


Figure 29-3. Internal Block Diagram

29.2 OPERATION

29.2.1 CDROM Programming Guide

29.2.1.1 Manual mode

1. Initialization
   A. Servo에 MSF Setting
   B. Execute RAWCapture Only, RAWCapture .

2. Interrupt : 1Frame

```
if (RAWCaptureOnly) {
    if (CDRRAWMSF==WantMSF) {
        RAWBank++;
        RunRawCapture(RAWBank);
        RunECCEDC(RAWBank-1, CDRDECADDR);
        RAWCaptureOnly=0;
    } else {
        if (TimeOut++ > 10) return FALSE_TIMEOUT;
        RunRawCapture(RAWBank);
    }
} else {
    if (CDRECCEDCBusy) {
        while(CDRECCEDCBusy);
        return FALSE_SHORTFRAME;
    }
    if (CDRDECMSFMode==WantMSFMode) {
        RAWBank++;
        RunRawCapture(RAWBank);
        RunECCEDC(RAWBank-1, CDRDECADDR);
        CDRDECADDR += 2340;
        WantMSF ++;
        if (DecNum++ == WantDecNum) return ALLFRAME_DONE;
        return TRUE;
    } else {
        return FALSE_SKIP;
    }
}
```

29.3.1.2 Auto Mode

29.3 CDROM DECODER CONTROL REGISTER

CDP Input Format Register (CDPIFORMAT)

Address : CXXX 0000h

Bit	R/W	Symbol	Description	Reset Value
[1:0]	R/W	**FORMAT**	Set CDP Data Format 00 : 16BCKs 01 : 25BCKs Last 10 : 24BCKs First 11 : 32BCKs Last	-
[2]	R/W	**MSBFIRST**	Set SDAT Format 0 : MSB First 1 : LSB First	-
[3]	R/W	**POLBCK**	Polarity of BCK 0 : Rising Edge 1 : Falling Edge	-
[15:4]	R	**Reserved**	-	-

TABLE 29-1. CDP INPUT FORMAT REGISTER (CDPIFORMAT)

CDP Decoding Control Register (CDPDECCTRL)

Address : CXXX 0002h

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**NUMFRAME**	Set Number of Frame for Decoding. (N+1)	-
[8]	R/W	**DESCENB**	Descramble Enable Control. 0 : Disable 1 : Enable	-
[9]	R/W	**AUTOMODE**	Set decoding method 0 : Sofrware mode 1 : H/W Detect mode	-
[10]	R/W	**AUTOENB**	Set manual or automatic 0 : Manual mode 1 : Automatic mode	-
[11]	R/W	**CAPENB**	Operate RAW Data Capture Block 0 : Disable 1 : Enable	
[12]	R	**Reserved**	-	-
[13]	R/W	**ECDRUN**	Operate ECC&EDC block by bit1 setting at manual mode. Check status of ECC&EDC Block at read (1: Busy)	
[14]	R/W	**RAWRUN**	Operate RAW Data Capture Block by bit1 setting at manual mode. Check status of Capture Block at read (1: Busy)	-
[15]	R/W	**DECRUN**	Operate decoder by bit1 setting at manual mode. Check Top block status when read. (1: Busy)	0

TABLE 29-2. CDP DECODING CONTROL REGISTER (CDPDECCTRL)

CDP Raw Data Base Address #0 Register (CDPRAWADDR0L/H)

Address : 0xCXXX 0004 (32bit Access)

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**RAWADDR0**	Set Temporary Buffer Address for CDP RAW Data capturing	-

TABLE 29-3. CDP RAW DATA BASE ADDRESS #0 REGISTER (CDPRAWADDR0L/H)

CDP Raw Data Base Address #1 Register (CDPRAWADDR1L/H)

Address : 0xCXXX 0008 (32bit Access)

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**RAWADDR1**	Set Temporary Buffer Address for CDP RAW Data Capturing	-

TABLE 29-4. CDP RAW DATA BASE ADDRESS #1 REGISTER (CDPRAWADDR1L/H)

CDP Decoded Data Base Address Register (CDPDECADDRL/H)

Address : 0xCXXX 000C (32bit Access)

Bit	R/W	Symbol	Description	Reset Value
[31:0]	R/W	**DECADDR**	Set Base Address for last data from ECC/EDC .	-

TABLE 29-5. CDP DECODED DATA BASE ADDRESS REGISTER (CDPDECADDRL/H)

CDP Timeout Register (CDPTIMEOUT)

Address : 0xCXXX 0010

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	**TIMEOUT**	Generate interrupt when Frame can not be found during Frame defined from TIMEOUT	-
[15:4]	R	**Reserved**	-	-

TABLE 29-6. CDP TIMEOUT REGISTER (CDPTIMEOUT)

CDP Target & RAW Min/Mode Control Register (CDPTRGRAWMODEMIN)

Address : 0xCXXX 0012

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	MIN	Set Minute Information of CDP Sector for Decoding Output RAW Data Capture Block MSF value when Read	-
[15:8]	R/W	MODE	Set Mod of CDP Sector for Decoding Output RAW Data Capture Block MSF value when Read 00 : MODE0/2 01 : MODE1 10 : MODE2 Form1 11 : MODE2 Form2	-

CDP Target & RAW Sec/Frame Control Register (CDPTRGRAWSECFRAME)

Address : 0xCXXX 0014

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R/W	FRAME	Set Frame Information of CDP Sector for Decoding Output RAW Data Capture Block MSF value when Read	-
[15:8]	R/W	SEC	Set Second of CDP Sector for Decoding Output RAW Data Capture Block MSF value when Read	-

TABLE 29-7. CDP TARGET & RAW SEC/FRAME CONTROL REGISTER (CDPTRGRAWSECFRAME)

CDP ECC&EDC Min/Mode Control Register (CDPECDMODEMIN)

Address : 0xCXXX 0016

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	MIN	Output ECC&EDC Block MSF value when Read	-
[15:8]	R	MODE	Output ECC&EDC Block MSF value when Read	-

TABLE 29-8. CDP ECC&EDC MIN/MODE CONTROL REGISTER (CDPECDMODEMIN)

CDP ECC&EDC Sec/Frame Control Register (CDPECDSECFRAME)

Address : 0xCXXX 0018

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	FRAME	Output ECC&EDC Block MSF value when Read	-
[15:8]	R	SEC	Output ECC&EDC Block MSF value when Read	-

TABLE 29-9. CDP ECC&EDC SEC/FRAME CONTROL REGISTER (CDPECDSECFRAME)

CDP Current Min/Mode Control Register (CDPCURMODEMIN)

Address : 0xCXXX 001A

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	MIN	Output current decoding block MSF when Read	-
[15:8]	R	MODE	Output current decoding block MSF when Read	-

TABLE 29-10. CDP CURRENT MIN/MODE CONTROL REGISTER (CDPCURMODEMIN)

CDP Current Sec/Frame Control Register (CDPCURSECFRAME)

Address : 0xCXXX 001C

Bit	R/W	Symbol	Description	Reset Value
[7:0]	R	FRAME	Output current decoding block MSF when Read	-
[15:8]	R	SEC	Output current decoding block MSF when Read	-

TABLE 29-11. CDP CURRENT SEC/FRAME CONTROL REGISTER (CDPCURSECFRAME)

CDP Interrupt Control Register (CDPINTP)

Address : 0xCXXX 001E

Bit	R/W	Symbol	Description	Reset Value
[0]	R/W	**PENDNOSRCH**	Indicate MSF sector can not be found during Frame defined from TIMEOUT 0 : Disable 1 : Enable	0
[1]	R/W	**PENDSFRAME**	Indicate Frame shorter than 2352 Byte is detected after satisfying MSF. Short Frame value s MSF value+1 0 : Disable 1 : Enable	0
[2]	R/W	**PENDSKIP**	Indicate decoding cannot be performed because of Frame skip after satisfying MSF. Skip Frame value is MSF value 0 : Disable 1 : Enable	0
[3]	R/W	**PENDEOF**	Indicate CPU assigned Decoding is finished after satisfying MSF. 0 : Disable 1 : Enable	0
[4]	R	**EDC Error**	Indicate EDC Error at current decoding sector	
[11:5]	R	**RESERVED**	-	0
[12]	R/W	**ENBNOSRCH**	Generate interrupt when MSF sector can not be found during Frame defined from TIMEOUT 0 : Disable 1 : Enable	0
[13]	R/W	**ENBSFRAME**	Generate interrupt when Frame shorter than 2352 Byte is detected after satisfying MSF. Short Frame value s MSF value+1 0 : Disable 1 : Enable	0
[14]	R/W	**ENBSKIP**	Generate interrupt when decoding cannot be performed because of Frame skip after satisfying MSF. Skip Frame value is MSF value 0 : Disable 1 : Enable	0
[15]	R/W	**ENBEOF**	Generate interrupt when CPU assigned Decoding is finished after satisfying MSF. 0 : Disable 1 : Enable	0

TABLE 29-12. CDP INTERRUPT CONTROL REGISTER (CDPINTP)

CHAPTER 30

1-WIRE MASTER

30. 1-WIRE MASTER

30.1 OVERVIEW

The 1-Wire Master produces all timing signals in order to reduce the standby time of the CPU. In addition, it supports a variable bus clock, from 4 MHz to 120 MHz. The CPU has access to read/write data on the 1-Wire bus in PIO mode.

FEATURES

- Generates all 1-Wire timing and control signals
- Supports variable clock, 4 ~ 120 MHz
- Supports search ROM accelerator
- Supports standard and overdrive communication speeds

30.2 PIN DESCRIPTION

For the connection with an external 1-Wire slave device, one signal pin is used.

Name	Direction	Description
OWDAT	B	1-Wire bus signal

TABLE 30-1. PIN DESCRIPTION

30.3 OPERATION

30.3.1 Initialization

The 1-Wire interface uses the GPIOO[0] pin. This pin is to be configured as GPIO AltFunction1 prior to activating 1-Wire communication.

1) Set GPIO index register (C000 1000h) as Eh (select GPIOO)
2) Set GPIO AltFnSelL register (C000 1002h) as xxxx_xxxx_xxxx_xx10b

30.3.2 Clocks

All 1-Wire timing patterns are generated using a base clock of 1 MHz. The 1-Wire Master will generate this clock frequency internally from peripheral bus clock. [The clock divisor must be configured and the clock enable bit set to 1 before communication on the 1-Wire bus can take place.] The clock divisor can support variable peripheral bus clock up to 100 MHz.

30.3.3 Operation Flow

Any communication with a 1-Wire slave device requires a 1-Wire initialization sequence. A reset pulse followed by a presence pulse indicates the 1-Wire slave is ready to accept a command. The following is the normal 1-Wire communication sequence:

1) Set the clock divisor register with the appropriate value and set the clock enable bit to 1
2) Reset the 1-Wire bus and detect the presence of the 1-Wire device
3) Write command to 1-Wire device by writing OWM_BUF_REG
4) Execute the read/write operation by reading and writing OWM_BUF_REG.
   Repeat steps 2 to 4 if needed.

The 1-Wire Master can generate two special commands besides the read/write operation: the first one is a '1-Wire Reset' command that has to be executed before any other command. The second one is a "Search ROM Accelerator" command.

Note : For the Reset and Search Rom commands, refer to the iButton Standards at (http://www.ibutton.com/iButtons/standard.pdf).

OWM Command Register (OWM_CMD)

Address : C000 4700h

Bit	R/W	Symbol	Description	Reset Value
3	R	**OW_IN**	Current status of 1-Wire bus line.	0b
2	R/W	**FOW**	Forces 1-Wire bus to low. This bit can be used to bypass the 1-Wire Master operations and drive the bus directly if needed. Setting this bit to high will drive the bus low until it is cleared or until the 1-Wire Master is reset. While the 1-Wire bus is held low, no other 1-Wire Master operations will function. By controlling the length of time this bit is set and the point when the line is sampled, any 1-Wire communication can be generated by the host controller. To prevent accidental writes to the bus, the EN_FOW bit in the CONTROL register must be set to a 1 before the FOW bit will function. This bit is cleared to a 0 on power-up or Master reset. 0 = disable forcing 1 = force 1-Wire bus to low	0b
1	R/W	**SRA**	Searches ROM Accelerator enable. When this bit is set, the 1-Wire Master will switch to the Search ROM Accelerator mode. When this bit is set to 0, the Master will function in its normal mode. This bit is cleared to 0 on a power-up or Master reset. 0 = normal mode 1 = search ROM accelerate mode	0b
0	R/W	**1WR**	1-Wire reset. If this bit is set, a reset will be generated on the 1-Wire bus. Setting this bit automatically clears the SRA bit. The 1WR bit will be automatically cleared as soon as the 1-Wire reset completes. The 1-Wire Master will set the Presence Detect interrupt flag (PD) when the reset is complete and sufficient time for a presence detect to occur has passed. The result of the presence detect will be placed in the interrupt register bit PDR. If a presence detection pulse was received, PDR will be cleared; otherwise it will be set. 0 = disable 1 = start 1-Wire reset	0b

TABLE 30-2. OWM COMMAND REGISTER (OWM_CMD)

30.3.4 Timing Diagram

Note : All time units are µs.

30.3.4.1 Reset and Presence Detection Timing

The 1-Wire Master transmits a reset pulse for t_{RSTL}, and then the 1-Wire bus line is pulled high. The slave device transmits a presence pulse for t_{PDL} after detecting a rising edge on the 1-Wire bus line and waiting for tPDH. The Master samples the 1-Wire bus at t_{PDS}.

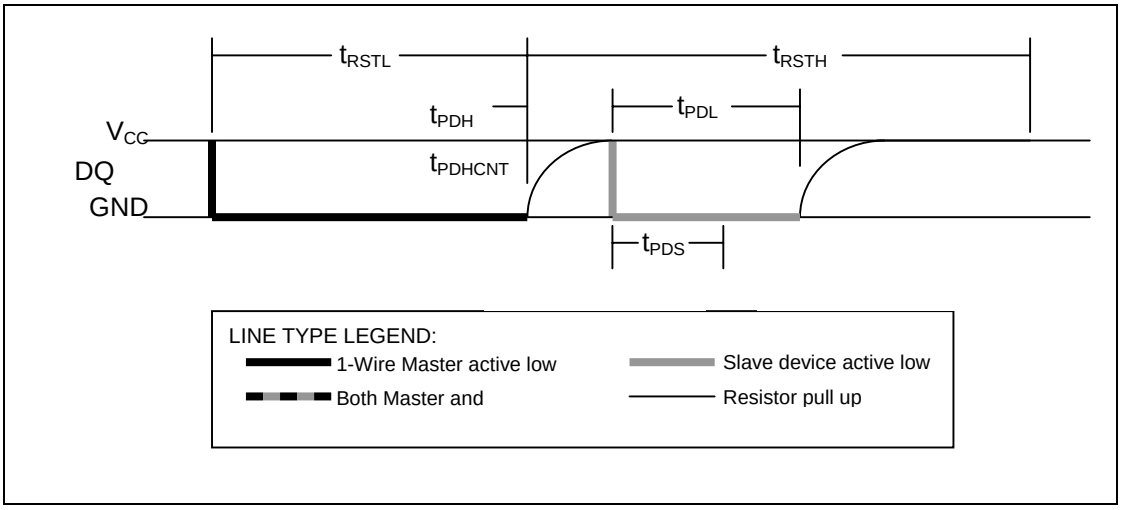


Figure 30-1. Reset and Presence Detection Timing

30.3.4.2 Write 0 and Write 1 Timing

A write time slot is initiated when the Master pulls the 1-Wire bus line from logic high to logic low. The line is held low for t_{LOW0} to write 0 or is released to logic high due to pull up to write 1. The slave will sample the 1-Wire bus line after 15 μs in normal mode.

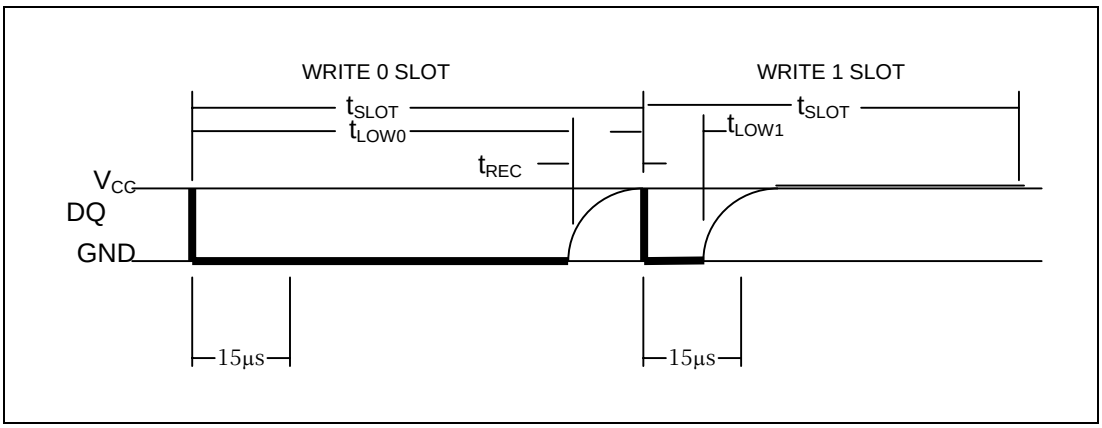


Figure 30-2. Write Time Slot

30.3.4.3 Read 0 and Read 1 Timing

A read time slot is initiated when the Master pulls the bus low for at lease 1 μs and then releases the bus. If the slave is responding with 0, it will continue to hold the bus line low. Otherwise it will release the bus line immediately. The Master will sample the data t_{RDV} from the start of the read time slot.

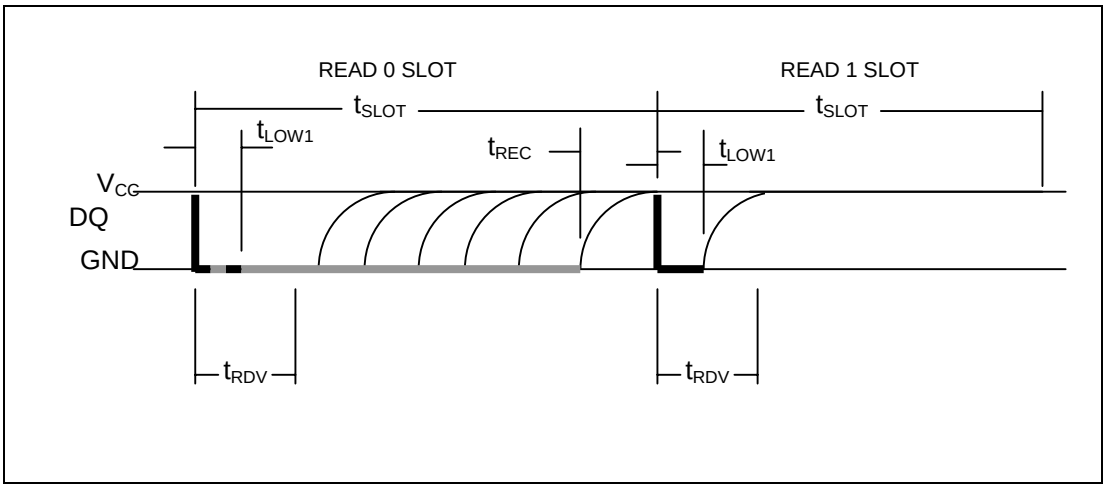


Figure 30-3. Read Time Slot

Symbol	Parameter	Conditions	Min	Max	Units
t_{LOW0}	Write 0 Low Time	Standard	60	120	μs
		Overdrive	6	16	μs
t_{LOW1}	Write 1 Low Time	Standard	1	15	μs
		Overdrive	1	2	μs
t_{PDH}	Presence Detect High	Standard	15	60	μs
		Overdrive	2	6	μs
t_{PDL}	Presence Detect Low	Standard	60	240	μs
		Overdrive	8	24	μs
t_{PDS}	Presence Detect Sample	Standard	24	31	μs
		Overdrive	2.4	4	μs
t_{RDV}	Read Data Value	Standard	12	15	μs
		Overdrive	1.6	2	μs
t_{REC}	Recovery Time	Standard	6.4	8	μs
		Overdrive	4	5	μs

Symbol	Parameter	Conditions	Min	Max	Units
t_{RSTH}	Reset Time High	Standard	508.8	636	µs
		Overdrive	59.2	74	µs
t_{RSTL}	Reset Time Low	Standard	500.8	626	µs
		Overdrive	50.4	63	µs
t_{SLOT}	Time Slot	Standard	68.8	86	µs
		Overdrive	12	15	µs

30.3.5 Read/write a Byte Data

Data sent and received from the 1-Wire Master passes through the transmit/receive buffer location. The 1-Wire Master is actually double-buffered, with separate transmit and receive buffers. Writing to this location connects the Transmit Buffer to the data bus, while reading connects the Receive Buffer to the data bus.

30.3.5.1 Writing a Byte

To send a byte on the 1-Wire bus, the user writes the desired data to the Transmit Buffer. The data is then moved to the Transmit Shift Register, where it is shifted serially onto the bus LSB-first sequence. A new byte of data can then be written to the Transmit Buffer. As soon as the Transmit Shift Register is empty, the data will be transferred from the Transmit Buffer, and the process repeats. Each of these registers has a flag that may be used as an interrupt source. The Transmit Buffer Empty (TBE) flag is set when the Transmit Buffer is empty and ready to accept a new byte. As soon as a byte is written into the Transmit Buffer, TBE is cleared. The Transmit Shift Register Empty (TEMT) flag is set when the shift register has no data in it and is ready to accept a new byte. As soon as a byte of data is transferred from the Transmit Buffer, TEMT is cleared and TBE is set. Remember that proper 1-Wire protocol requires a reset before any bus communication.

30.3.5.2 Reading a Byte

To read data from a slave device, the device must first be ready to transmit data depending on commands already received from the CPU. Data is retrieved from the bus in a similar fashion to a write operation. The host initiates a read by writing to the Transmit Buffer. The data that is then shifted into the Receive Shift Register [is the wired-AND of the written data and the data from the slave device.] Therefore in order to read a byte from a slave device, the host must write 0xFFh. When the Receive Shift Register is full, the data is transferred to the Receive Buffer where it can be accessed by the host. Additional bytes can now be read by sending 0xFFh again. If the slave device is not ready to transmit, the data received will be identical to that which was transmitted. The Receive Buffer Register can also generate interrupts. The Receive Buffer flag (RBF) is set when data is transferred from the Receive Shift Register and cleared when the host reads the register. If RBF is set, no further transmissions should be made on the 1-Wire bus or else data may be lost since the byte in the Receive Buffer will be overwritten by the next received byte. See the timing diagrams for details of the byte reception operation.

Generating a 1-Wire reset on the bus is covered under Command Operations. Interrupt flags are explained in further detail under Interrupt Operations. Write and read operations are detailed in the timing diagrams.

30.3.6 1-Wire Status

Flags from the Current Status, Transmit, Receive, and 1-Wire reset operations are located in the Status Register. The Presence Detect flag (PD), OW_LOW, and OW_SHORT are cleared when the Interrupt Register is read. The other flags are cleared automatically when the Transmit and Receive Buffers are written to or read from. All of these flags can generate an interrupt if the corresponding enable bit is set in the Status Enable Register. To clear the interrupt signal, the Status Register must be read.

OWM Data Buffer Register (OWM_BUF)

Address: C000 4702h

Bit	R/W	Symbol	Description	Reset Value
7:0	R/W	OWM_BUF	1-Wire bus read/write Data Buffer. Serial data in/out is placed in LSB first. - Write If the TBE bit of OWM_STATUS register is 1, the CPU can write data to this register. - Read If the RBF bit of OWM_STATUS register is 1, the CPU can read data from this register.	00h

TABLE 30-3. OWM DATA BUFFER REGISTER (OWM_BUF)

OWM Status Register (OWM_STA)

Address: C000 4704h

Bit	R/W	Symbol	Description	Reset Value
7	R/C	**OW_LOW**	This flag will be set to 1 when the 1-Wire line is low and the Master is in idle signaling that a slave device has issued a presence pulse on the 1-Wire line. A read to the Status Register will clear this bit.	0b
6	R/C	**OW_SHORT**	This flag will be set to a 1 when the 1-Wire line was low before the Master was able to send out the beginning of a reset or a time slot. When this flag is 0, it indicates that the 1-Wire line was high as expected prior to all resets and time slots. A read to the Status Register will clear this bit. 0 = bus ready 1 = bus not ready (bus is already low state)	0b

Bit	R/W	Symbol	Description	Reset Value
5	R	**RSRF**	Receive Shift Register is full. This flag will be set to 1 when there is a byte of data waiting in the Receive Shift Register. When this bit is 0, it indicates that the Receive Shift Register is either empty or currently receiving data. This bit will be cleared when data in the Receive Shift Register is transferred to the Receive Buffer. A read to the Status Register will have no effect on this bit. 0 = not full 1 = full	0b
4	R	**RBF**	Receive Buffer is full. This flag will be set to 1 when there is a byte of data waiting to be read in the Receive Buffer. When this bit is 0, it indicates that the Receive Buffer has no new data to be read. This bit will be cleared when the byte is read from the Receive Buffer. A read to the Interrupt Flag Register will have no effect on this bit. However, following a read of the Interrupt Register, if the ERBF is not cleared and the value is not read from the Receive Buffer, while the Enable Receive Buffer Full status (ERBF) is set to 1,, the interrupt will fire again. 0 = not full 1 = full	0b
3	R	**TEMT**	Transmit Shift Register is empty. This flag will be set to 1 when there is nothing in the Transmit Shift Register and it is ready to receive the next byte of data to be transmitted from the Transmit Buffer. When this bit is 0, it indicates that the Transmit Shift Register is busy sending out data. This bit is cleared when data is transferred from the Transmit Buffer to the Transmit Shift Register. A read to the Status Register will have no effect on this bit. 0 = not empty 1 = empty	0b
2	R	**TBE**	Transmit Buffer empty. This flag will be set to 1 when there is nothing in the Transmit Buffer and it is ready to receive the next byte of data. When it is 0, it indicates that the Transmit Buffer is waiting for the Transmit Shift Register to finish sending its current data before updating it. This bit is cleared when data is written to the Transmit Buffer. A read to the Status Register will have no effect on this bit. 0 = not empty 1 = empty	0b
1	R	**PDR**	Presence detection when PD occurs. When a presence detect interrupt occurs, this bit will reflect the result of the presence detect read – it will be 0 if a slave was found, or 1 if no device was found. A read to the Status Register will have no effect on this bit. 0 = slave found 1 = slave not found	0b

Bit	R/W	Symbol	Description	Reset Value
0	R/C	**PD**	Presence detection check time flag. After a 1-Wire Reset has been issued, this flag will be set to 1 after the appropriate amount of time for a presence detect pulse to have occurred. This flag will be 0 when the Master has not issued a 1-Wire Reset since the previous read of the Interrupt Register. This bit is cleared when the Status Register is read. 0 = not presence detect time 1 = presence detect time	0b

TABLE 30-4. STATUS REGISTER

OWM Status Enable Register (OWM_STA_ENA)

Address: C000 4706h

Bit	R/W	Symbol	Description	Reset Value
7	R/W	**EOWL**	Enable 1-Wire Low Interrupt. Setting this bit to a 1 enables the 1-Wire Low Interrupt. If set, INTR will be established when the OW_LOW flag is set. Clearing this bit disables OW_LOW as an active interrupt source. 0 = disable 1 = enable	0b
6	R/W	**EOWSH**	Enable 1-Wire Short Interrupt. Setting this bit to a 1 enables the 1-Wire Short Interrupt. If set, INTR will be established when the OW_SHORT flag is set. Clearing this bit disables OW_SHORT as an active interrupt source. 0 = disable 1 = enable	0b
5	R/W	**ERSF**	Enable Receive Shift Register Full Interrupt. Setting this bit to a 1 enables the Receive Shift Register Full Interrupt. If set, INTR will be established when the RSRF flag is set. Clearing this bit disables RSRF as an active interrupt source. 0 = disable 1 = enable	0b
4	R/W	**ERBF**	Enable Receive Buffer Full Interrupt. Setting this bit to a 1 enables the Receive Buffer Full Interrupt. If set, INTR will be established when the RBF flag is set. Clearing this bit disables RBF as an active interrupt source. 0 = disable 1 = enable	0b
3	R/W	**ETMT**	Enable Transmit Shift Register Empty Interrupt. Setting this bit to a 1 enables the Transmit Shift Register Empty Interrupt. If set, INTR will be established when the TEMT flag is set. Clearing this bit disables TEMT as an active interrupt source. 0 = disable 1 = enable	0b

Bit	R/W	Symbol	Description	Reset Value
2	R/W	**ETBE**	Enable Transmit Buffer Empty Interrupt. Setting this bit to a 1 enables the Transmit Buffer Empty Interrupt. If set, INTR will be asserted when the TBE flag is set. Clearing this bit disables TBE as an active interrupt source. 0 = disable, 1 = enable	0b
1	R/W	**Reserved**	-	-
0	R/W	**EPD**	Enable Presence Detect Interrupt. Setting this bit to a 1 enables the Presence Detect Interrupt. If set, INTR will be established when the PD flag is set. Clearing this bit disables PD as an active interrupt source. 0 = disable 1 = enable	0b

TABLE 30-5. OWM STATUS REGISTER (OWM_STA)

OWM Clock Divisor Register (OWM_CLK_DIVISOR)

Address: C000 4708h

Bit	R/W	Symbol	Description	Reset Value
7	R/W	**CLK_EN**	Clock Enable 0 = disable clock 1 = enable clock	0b
6:5	R/W	**Reserved**	-	-
4:0	R/W	**PRESCALE[?]**	Clock prescale[?] value. Refer to prescale[?] value table below.	0h

Min CLK Frequency (MHz)	Max CLK Frequency (MHz)	PreScale[?] value
4.0	< 5.0	08h
5.0	< 6.0	02h
6.0	< 7.0	05h
7.0	< 8.0	03h
8.0	< 10.0	0eh
10.0	< 12.0	06h
12.0	< 14.0	09h
14.0	< 16.0	07h
16.0	< 20.0	10h
20.0	< 24.0	0ah
24.0	< 28.0	0dh
28.0	< 32.0	0bh
32.0	< 40.0	14h

Min CLK Frequency (MHz)	Max CLK Frequency (MHz)	PreScale[?] value
40.0	< 48.0	0eh
48.0	< 56.0	11h
56.0	< 64.0	0fh
64.0	< 80.0	18h
80.0	< 96.0	12h
96.0	< 100.0	15h

TABLE 30-6. CLOCK DIVISOR REGISTER

OMW Control Register (OWM_CTRL)

Address: C000 470Ah

Bit	R/W	Symbol	Description	Reset Value
6	R/W	**OD**	Overdrive mode enable. Setting this bit to a 1 will place the Master into Overdrive mode which effectively changes the Master's 1-Wire timings to match those outlined for Overdrive in the **Book of iButton Standards**. Clearing this bit to a 0 leaves the Master operating in standard mode speed. 0 = normal mode 1 = overdrive mode	0
5:3	R/W	**Reserved**	-	-
2	R/W	**EN_FOW**	Enable Force 1-Wire. Setting this bit to a 1 will enable the functionality of the Force 1-Wire (FOW) register bit in the Command Register. Clearing this bit will disable the functionality of the FOW bit. 0 = disable force 1 = enable force	0
1:0	R/W	**Reserved**	-	-

TABLE 30-7. OWM CLOCK DIVISOR REGISTER (OWM_CLK_DIVISOR)

OWM IRQ Register (OWM_IRQ)

Address: C000 470Ch

Bit	R/W	Symbol	Description	Reset Value
0	R	**IRQ_OCCUR**	OWM IRQ status occurred flag. 0 = IRQ status did not occur 1 = IRQ status occurred	0

TABLE 30-8. IRQ REGISTER

30.4 REGISTER MAP LIST

OWM Command Register (OWM_CMD)

Address: C000 4700h

Bit	R/W	Symbol	Description	Reset Value
OWM Command Register (OWM_CMD) ***Address : C000 4700h***				
3	R	**OW_IN**	Current state of 1-Wire bus line	0b
2	R/W	**FOW**	Force 1-Wire bus to low	0b
1	R/W	**SRA**	Search ROM accelerator enable	0b
0	R/W	**1WR**	1-Wire reset	0b
OWM Data Buffer Register (OWM_BUF) ***Address : C000 4702h***				
7:0	R/W	**OWM_BUF**	1-Wire bus read/write data buffer	00h
OWM Status Register (OWM_STA) ***Address : C000 4704h***				
7	R/C	**OW_LOW**	1-Wire line is low	0b
6	R/C	**OW_SHORT**	1-Wire line was low before Master was able to send out a reset or a time slot	0b
5	R	**RSRF**	Receive shift register is full	0b
4	R	**RBF**	Receive buffer is full	0b
3	R	**TEMT**	Transmit shift register is empty	0b
2	R	**TBE**	Transmit buffer is empty	0b
1	R	**PDR**	Presence detection when PD occurs	0b
0	R/C	**PD**	Presence detection check time flag	0b
OWM Status Enable Register (OWM_STA_ENA) ***Address : C000 4706h***				
7	R/W	**EOWL**	Enable 1-Wire Low Interrupt	0b
6	R/W	**EOWSH**	Enable 1-Wire Short Interrupt	0b
5	R/W	**ERSF**	Enable Receive Shift Register Full Interrupt	0b
4	R/W	**ERBF**	Enable Receive Buffer Full Interrupt	0b
3	R/W	**ETMT**	Enable Transmit Shift Register Empty Interrupt	0b
2	R/W	**ETBE**	Enable Transmit Buffer Empty Interrupt	0b

Bit	R/W	Symbol	Description	Reset Value
1	R/W	**Reserved**	Reserved	0b
0	R/W	**EPD**	Enable Presence Detect Interrupt	0b
OWM Clock Diviso[?] Register (OWM_CLK_DIVISOR) ***Address : C000 4708h***				
7	R/W	**CLK_EN**	Clock Enable	0b
6:5	R/W	**Reserved**	-	-
4:0	R/W	**PRESCALE[?]**	Clock prescale[?] value	0h
OMW Control Register (OWM_CTRL) ***Address : C000 470Ah***				
6	R/W	**OD**	Overdrive mode enable	0
5:3	R/W	**Reserved**	-	-
2	R/W	**EN_FOW**	Enable Force 1-Wire	0
1:0	R/W	**Reserved**	-	-
OWM IRQ Register (OWM_IRQ) ***Address : C000 470Ch***				
0	R	**IRQ_OCCUR**	OWM IRQ status occurred flag	0

TABLE 30-9. COMMAND REGISTER (OWM_CMD)

CHAPTER 31

DECSS

31. DECSS

31.1 OVERVIEW

The DECSS block has the decoding function for the MPEG Decoding of the DVD Streams encoded by the CSS Algorithm.

Programmers can transfer encoded Data to the DECSS Block and able to read the decoded Data by means of the DMA or PIO.

FEATURES

- Hardwired Descramble Logic
- Supports DMA or PIO data transfer mode
- 4 Byte Input & Output FIFO

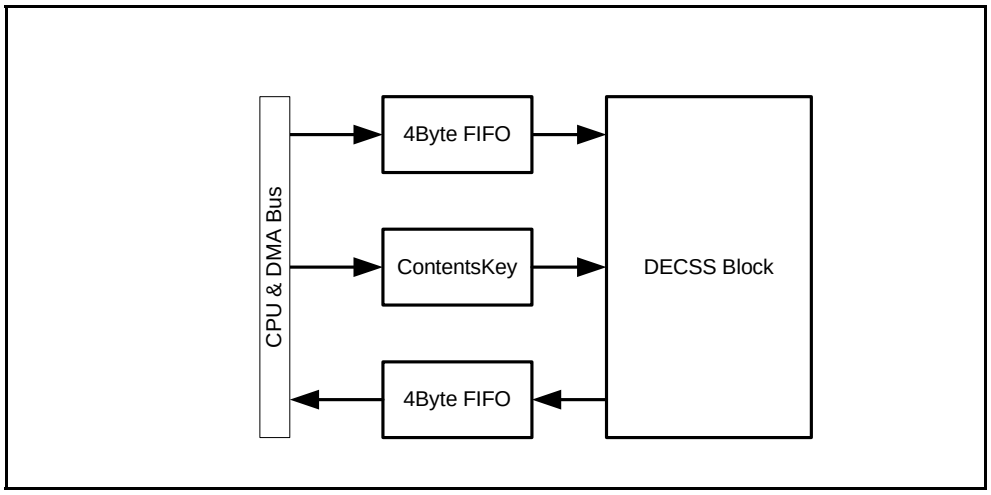


Figure 31-1. DECSS Block Diagram

31.2 OPERATION

To store the decoded contents into the Output FIFO by means of DMA or PIO transfer mode in the DECSS Block, it is required to store the DVD contents key first. After ward, load the encoded data into INPUT FIFO by DMA or PIO mode to descrable the data.

Before the initial transmission is started, the DECSS Block must have been initialized with the CSSRSTENB bit.

The DMAWENB Bit and the DMARENB Bit determine the transmission into the Input FIFO or the Output FIFO via the CPU or the DMA.

Before the transmission of Data, the Contents Key is set. Then the REQINIT Bit will be set, and the internal DECSS Block will be initialized according to the entered Contents Key.

After initialization, the CPU will check the status of the FIFO in PIO Mode, and the Data will be transmitted into the FIFO. In DMA Mode, the DMA Transform will be automatically carried out according to the status of the FIFO.

The DECSSNUM Register shows the number of the Data transmitted into the Main Memory via the DMA in the DECSS Block. With this number, the transmission completed point can be confirmed on the DMA transmission.

31.3 DECSS CONTROL REGISTERS LIST

Bit	R/W	Symbol	Description	Reset Value
DECSS Control Register (DECSSCTRL) ***Address : 0xC000 1700h***				
[0]	R/W	**REQINIT**	Perform Initialization with Content Key 0 : Default 1: Initialization After finishing Initialization, automatically goes to '0'.	0
[1]	R/W	**DMAWENB**	DMA Write Mode 0 : Disable 1 : Enable	0
[2]	R/W	**DMARENB**	DMA Read Mode 0 : Disable 1 : Enable	0
[3]	R/W	**CSSRSTENB**	Software Reset Perform Software Reset, Must be set to '0' after resetting. 0 : Default 1 : Reset	0
[13:4]	R	**Reserved**	-	-
[14]	R/W	**RFFEMPTY**	Read FIFO Empty Flag 0 : Valid Data 1 : Empty	0
[15]	R/W	**WFFFULL**	Write FIFO Full Flag 0 : Default 1 : Full	0
DECSS Content Key #0 Register (DECSSKEY0) ***Address : 0xC000 1702h***				
[15:0]	R/W	**DECSSKEY0**	Content Key 0	0
DECSS Content Key #1 Register (DECSSKEY1) ***Address : 0xC000 1704h***				
[15:0]	R/W	**DECSSKEY1**	Content Key 1	0
DECSS Content Key #2 Register (DECSSKEY2) ***Address : 0xC000 1706h***				
[15:0]	R/W	**DECSSKEY2**	Content Key 2	0
DECSS Data Register (DECSSDATA) ***Address : 0xC000 1708h***				
[7:0]	R/W	**DECSSDATA**	Write : CSS Data Read : DECSS Data	0
[15:8]	R	**-**	Reserved	-
DECSS Number Register (DECSSNUM) ***Address : 0xC000 170Ah***				
[7:0]	R/W	**DECSSNUM**	Holds the current number of transmitled halfword data into the Main Memory via the DMA.	0
[15:8]	R	**-**	Reserved	-